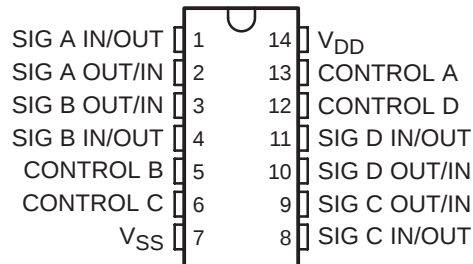


- 15-V Digital or ± 7.5 -V Peak-to-Peak Switching
- 125- Ω Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output-Voltage Ratio: 80 dB Typical at $f_{IS} = 10$ kHz, $R_L = 1$ k Ω
- High Degree of Linearity: <0.5% Distortion Typical at $f_{IS} = 1$ kHz, $V_{IS} = 5$ V p-p, $V_{DD} - V_{SS} \geq 10$ V, $R_L = 10$ k Ω
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS} = 10$ V, $T_A = 25^\circ\text{C}$
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical
- Low Crosstalk Between Switches: -50 dB Typical at $f_{IS} = 8$ MHz, $R_L = 1$ k Ω
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20 V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices*
- Applications:
 - Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch
 - Digital Signal Switching/Multiplexing
 - Transmission-Gate Logic Implementation
 - Analog-to-Digital and Digital-to-Analog Conversion
 - Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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CD4066B
CMOS QUAD BILATERAL SWITCH

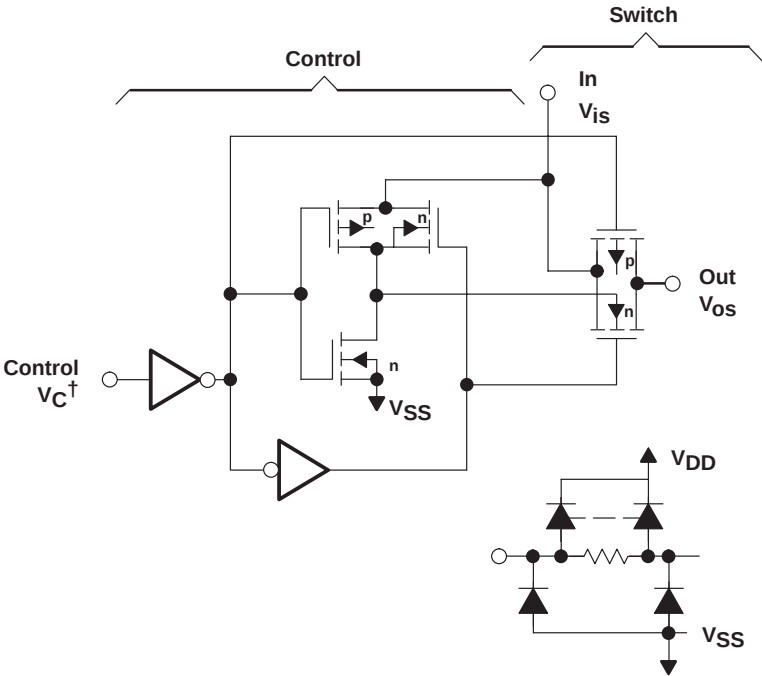
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description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube of 25	CD4066BE	CD4066BE
	SOIC – M	Tube of 50	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP – NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP – PW	Tube of 90	CD4066BPW	CM066B
		Reel of 2000	CD4066BPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



- † All control inputs are protected by the CMOS protection network.
- NOTES: A. All p substrates are connected to V_{DD} .
B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $V_{SS} \leq V_{IS} \leq V_{DD}$

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Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal)	–0.5 V to 20 V
Input voltage range, V_{IS} (all inputs)	–0.5 V to $V_{DD} + 0.5$ V
DC input current, I_{IN} (any one input)	±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package	80°C/W
M package	86°C/W
NS package	76°C/W
PW package	113°C/W
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	265°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
V_{DD} Supply voltage	3	18	V
T_A Operating free-air temperature	–55	125	°C

CD4066B

CMOS QUAD BILATERAL SWITCH

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electrical characteristics

PARAMETER	TEST CONDITIONS	LIMITS AT INDICATED TEMPERATURES								UNIT
		VIN (V)	VDD (V)	–55°C	–40°C	85°C	125°C	25°C		
								TYP	MAX	
IDD Quiescent device current		0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0, 10	10	0.5	0.5	15	15	0.01	0.5	
		0, 15	15	1	1	30	30	0.01	1	
		0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (VIS) and Outputs (VOS)										
ron On-state resistance (max)	VC = VDD, RL = 10 kΩ returned to $\frac{(V_{DD} - V_{SS})}{2}$, VIS = VSS to VDD	5	800	850	1200	1300	470	1050	Ω	
		10	310	330	500	550	180	400		
		15	200	210	300	320	125	240		
Δron On-state resistance difference between any two switches	RL = 10 kΩ, VC = VDD	5					15	Ω		
		10					10			
		15					5			
THD Total harmonic distortion	VC = VDD = 5 V, VSS = –5 V, VIS(p-p) = 5 V (sine wave centered on 0 V), RL = 10 kΩ, fIS = 1-kHz sine wave						0.4	%		
–3-dB cutoff frequency (switch on)	VC = VDD = 5 V, VSS = –5 V, VIS(p-p) = 5 V (sine wave centered on 0 V), RL = 1 kΩ						40	MHz		
–50-dB feedthrough frequency (switch off)	VC = VSS = –5 V, VIS(p-p) = 5 V (sine wave centered on 0 V), RL = 1 kΩ						1	MHz		
IIS Input/output leakage current (switch off) (max)	VC = 0 V, VIS = 18 V, VOS = 0 V; and VC = 0 V, VIS = 0 V, VOS = 18 V	18	±0.1	±0.1	±1	±1	±10–5	±0.1	μA	
–50-dB crosstalk frequency	VC(A) = VDD = 5 V, VC(B) = VSS = –5 V, VIS(A) = 5 Vp-p, 50-Ω source, RL = 1 kΩ						8	MHz		
tpd Propagation delay (signal input to signal output)	RL = 200 kΩ, VC = VDD, VSS = GND, CL = 50 pF, VIS = 10 V (square wave centered on 5 V), tr, tf = 20 ns	5					20	40	ns	
		10					10	20		
		15					7	15		
CIS Input capacitance	VDD = 5 V, VC = VSS = –5 V						8	pF		
COS Output capacitance	VDD = 5 V, VC = VSS = –5 V						8	pF		
CIOS Feedthrough	VDD = 5 V, VC = VSS = –5 V						0.5	pF		

electrical characteristics (continued)

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
			−55°C	−40°C	85°C	125°C	25°C		
							TYP	MAX	
Control (V _C)									
V _{ILC} Control input, low voltage (max)	I _{IS} < 10 μA, V _{IS} = V _{SS} , V _{OS} = V _{DD} , and V _{IS} = V _{DD} , V _{OS} = V _{SS}	5	1	1	1	1	1		V
		10	2	2	2	2	2		
		15	2	2	2	2	2		
V _{IHC} Control input, high voltage	See Figure 6	5	3.5 (MIN)						V
		10	7 (MIN)						
		15	11 (MIN)						
I _{IN} Input current (max)	V _{IS} ≤ V _{DD} , V _{DD} − V _{SS} = 18 V, V _{CC} ≤ V _{DD} − V _{SS}	18	±0.1	±0.1	±1	±1	±10 ^{−5}	±0.1	μA
Crosstalk (control input to signal output)	V _C = 10 V (square wave), t _r , t _f = 20 ns, R _L = 10 kΩ	10					50		mV
Turn-on and turn-off propagation delay	V _{IN} = V _{DD} , t _r , t _f = 20 ns, C _L = 50 pF, R _L = 1 kΩ	5					35	70	ns
		10					20	40	
		15					15	30	
Maximum control input repetition rate	V _{IS} = V _{DD} , V _{SS} = GND, R _L = 1 kΩ to GND, C _L = 50 pF, V _C = 10 V (square wave centered on 5 V), t _r , t _f = 20 ns, V _{OS} = 1/2 V _{OS} at 1 kHz	5					6		MHz
		10					9		
		15					9.5		
C _I Input capacitance							5	7.5	pF

switching characteristics

V _{DD} (V)	SWITCH INPUT						SWITCH OUTPUT, V _{OS} (V)	
	V _{IS} (V)	I _{IS} (mA)					MIN	MAX
		-55°C	-40°C	25°C	85°C	125°C		
5	0	0.64	0.61	0.51	0.42	0.36		0.4
5	5	-0.64	-0.61	-0.51	-0.42	-0.36	4.6	
10	0	1.6	1.5	1.3	1.1	0.9		0.5
10	10	-1.6	-1.5	-1.3	-1.1	-0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4		1.5
15	15	-4.2	-4	-3.4	-2.8	-2.4	13.5	

CD4066B CMOS QUAD BILATERAL SWITCH

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TYPICAL CHARACTERISTICS

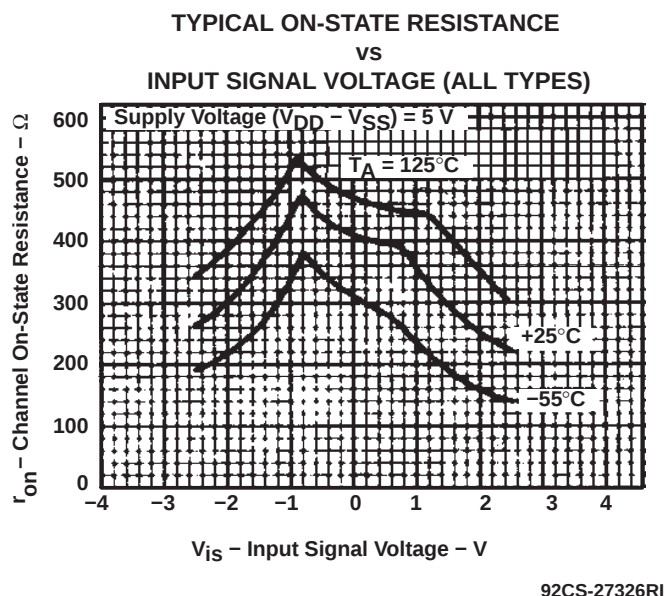


Figure 2

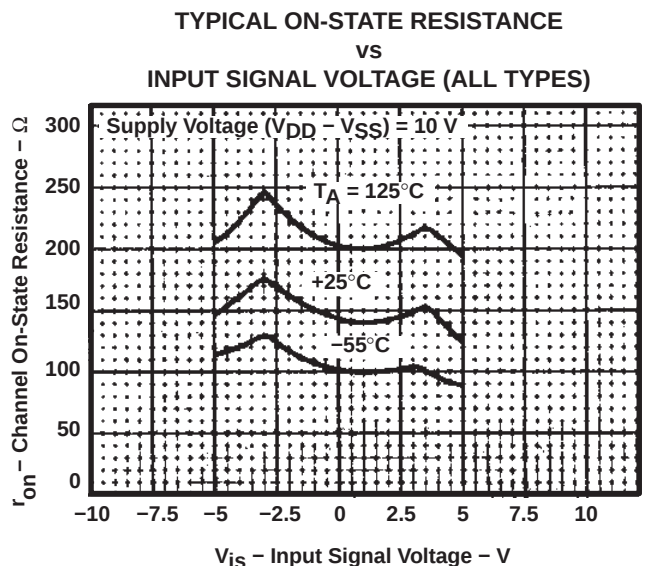


Figure 3

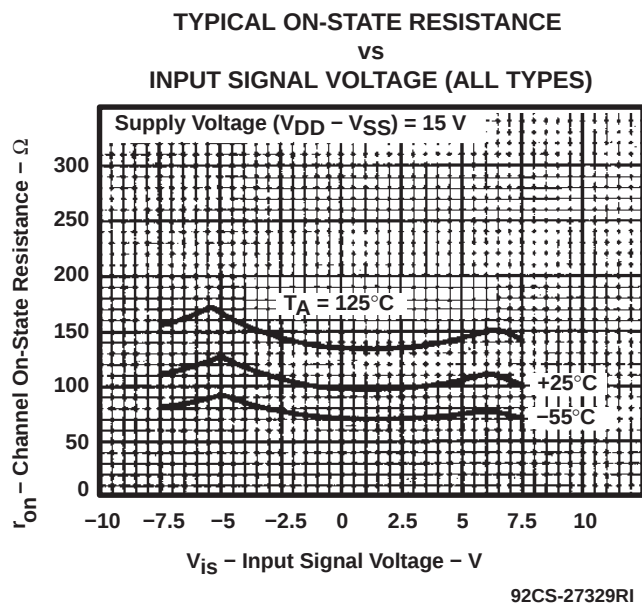


Figure 4

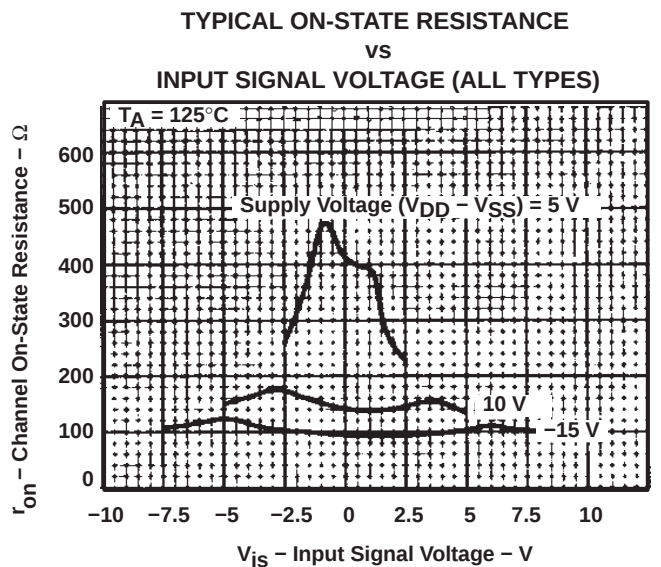
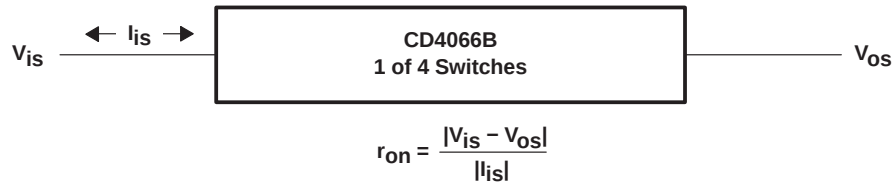


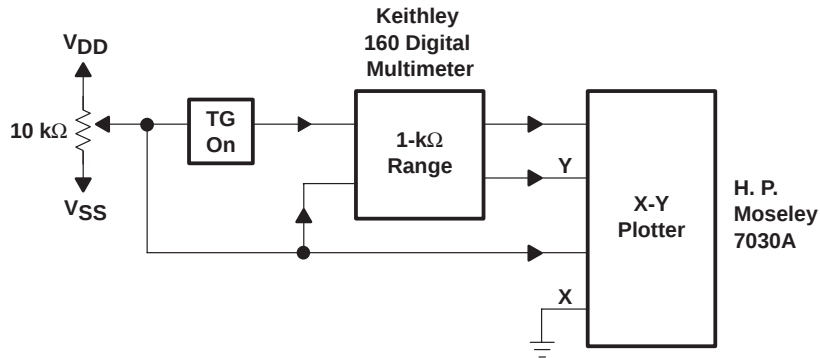
Figure 5

TYPICAL CHARACTERISTICS



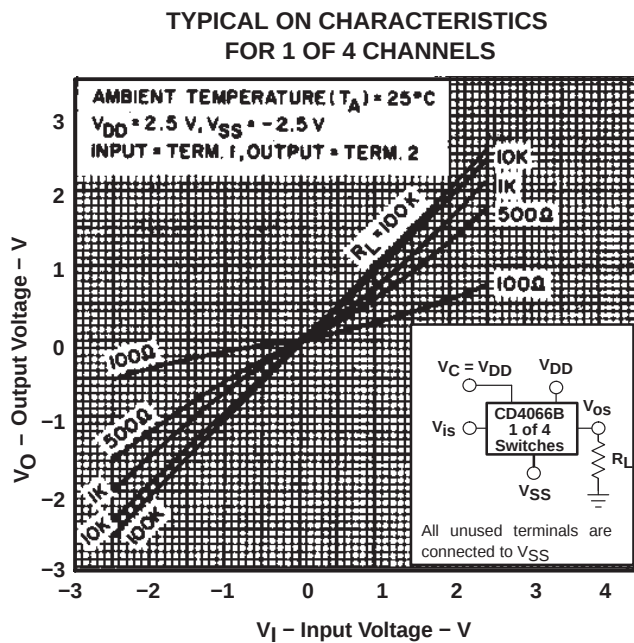
92CS-30966

Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification



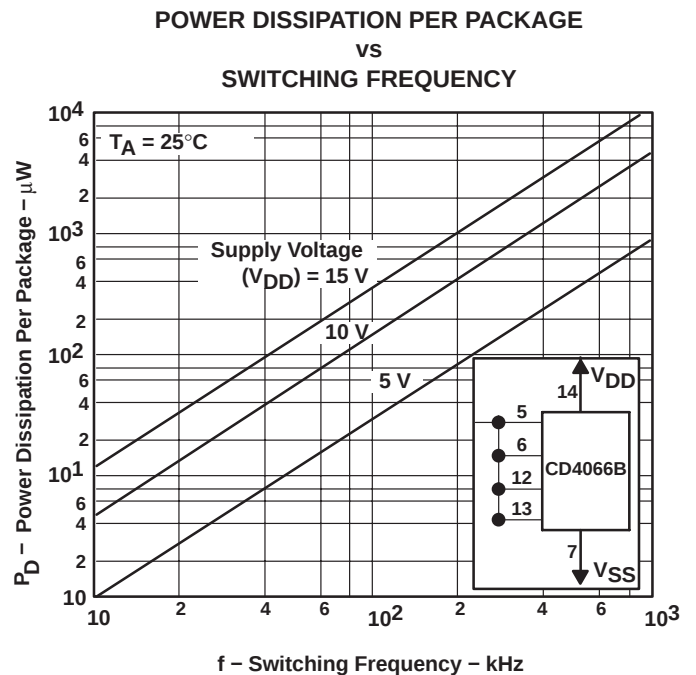
92CS-22716

Figure 7. Channel On-State Resistance Measurement Circuit



92CS-30919

Figure 8



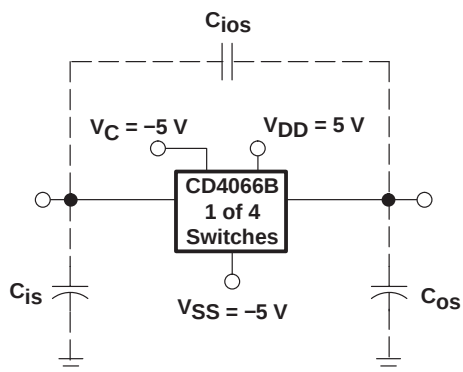
92C-30920

Figure 9

CD4066B CMOS QUAD BILATERAL SWITCH

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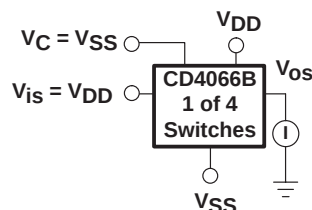
TYPICAL CHARACTERISTICS



92CS-30921

Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

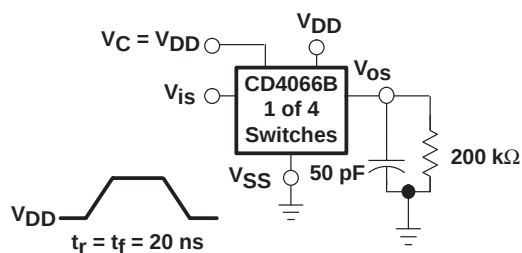
Figure 10. Typical On Characteristics for One of Four Channels



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All unused terminals are connected to V_{SS} .

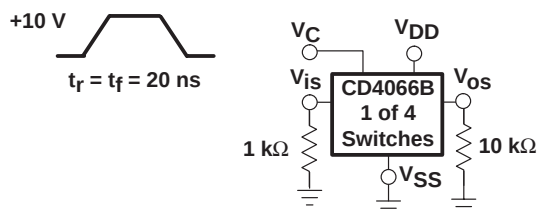
Figure 11. Off-Switch Input or Output Leakage



92CS-30923

All unused terminals are connected to V_{SS} .

Figure 12. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})

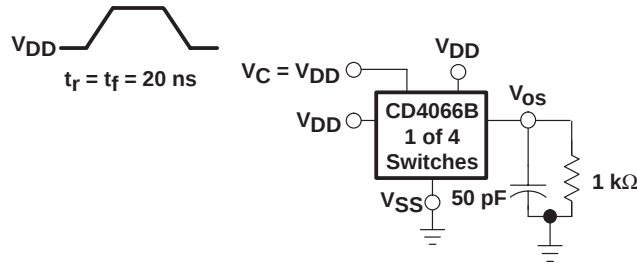


92CS-30924

All unused terminals are connected to V_{SS} .

Figure 13. Crosstalk-Control Input to Signal Output

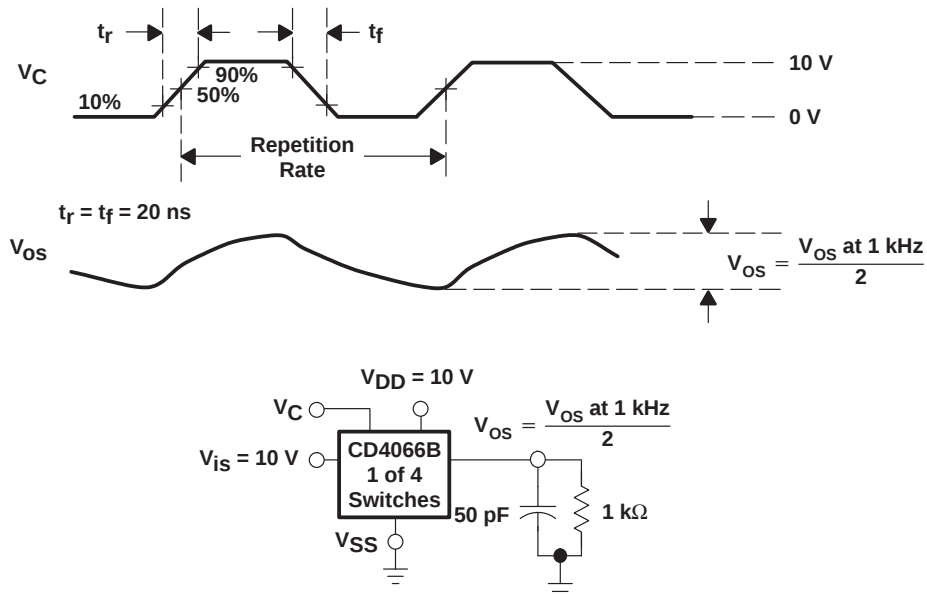
TYPICAL CHARACTERISTICS



NOTES: A. All unused terminals are connected to V_{SS} .
 B. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

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Figure 14. Propagation Delay, t_{PLH} , t_{PHL} Control-Signal Output



All unused terminals are connected to V_{SS} .

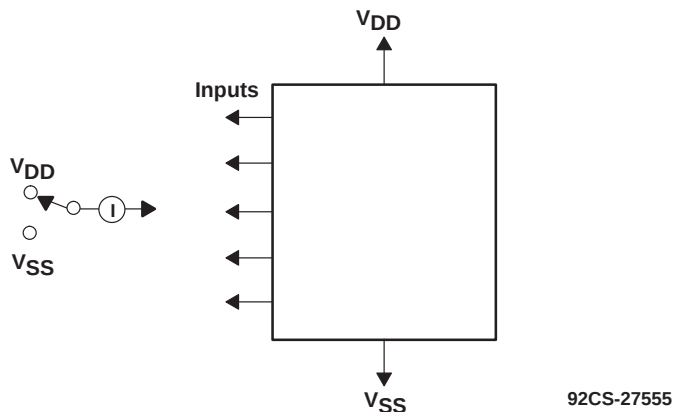
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Figure 15. Maximum Allowable Control-Input Repetition Rate

CD4066B CMOS QUAD BILATERAL SWITCH

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TYPICAL CHARACTERISTICS



Measure inputs sequentially to both V_{DD} and V_{SS} . Connect all unused inputs to either V_{DD} or V_{SS} . Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

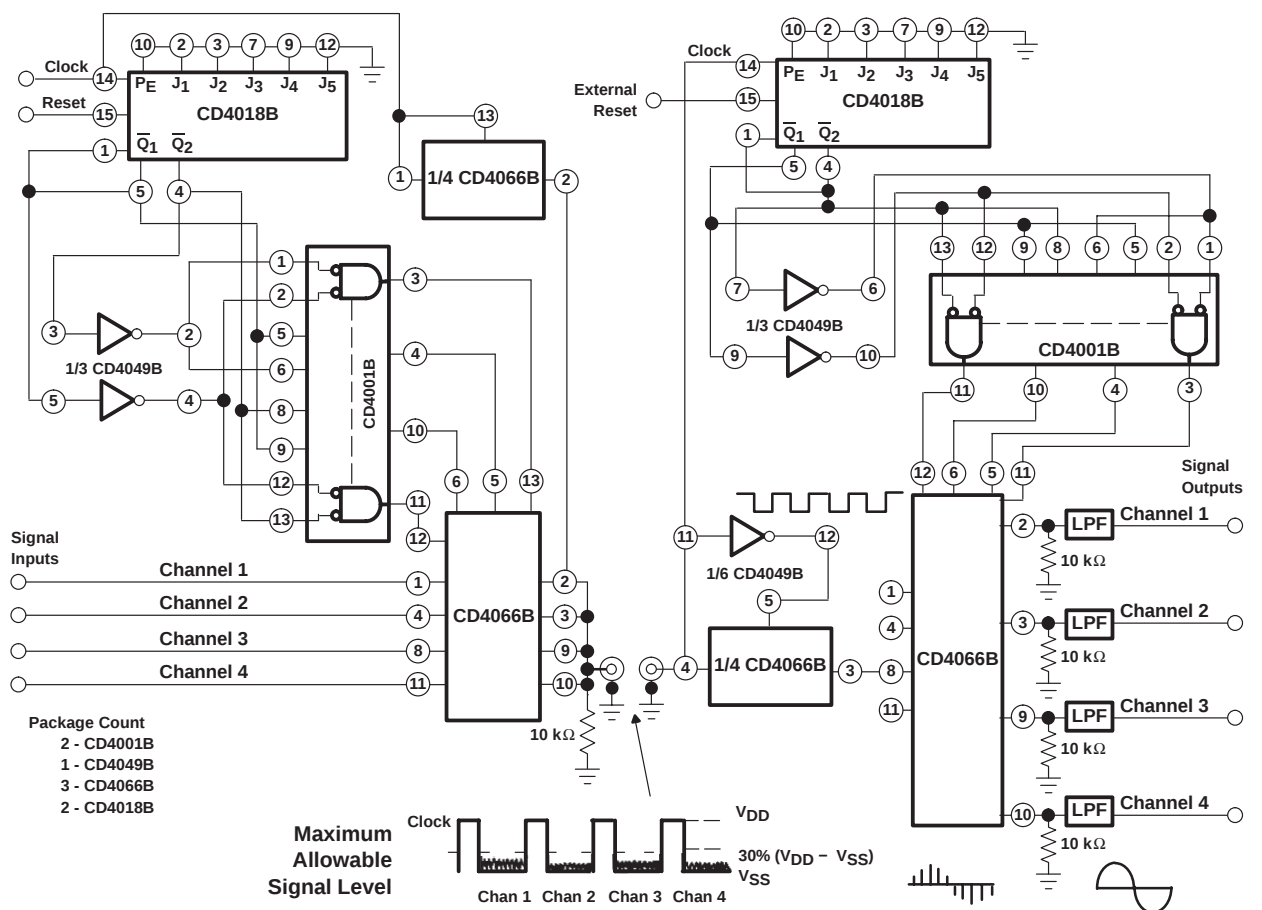
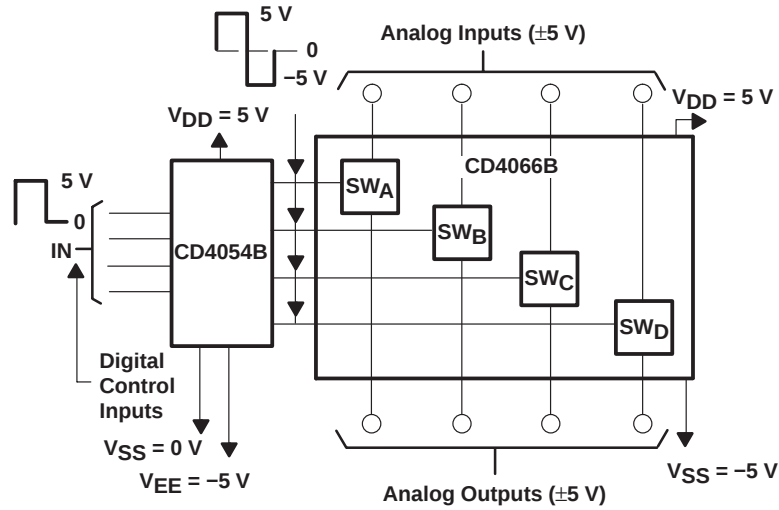


Figure 17. Four-Channel PAM Multiplex System Diagram

TYPICAL CHARACTERISTICS



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Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

CD4066B

CMOS QUAD BILATERAL SWITCH

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APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4066BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4066BF	Samples
CD4066BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4066BF3A	Samples
CD4066BF3AS2283	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI			
CD4066BF3AS2534	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI			
CD4066BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066B	Samples
CD4066BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples
M38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4066B, CD4066B-MIL :

- Catalog: [CD4066B](#)
- Automotive: [CD4066B-Q1](#), [CD4066B-Q1](#)
- Military: [CD4066B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4066BM96	SOIC	D	14	2500	333.2	345.9	28.6
CD4066BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4066BM96	SOIC	D	14	2500	364.0	364.0	27.0
CD4066BM96G4	SOIC	D	14	2500	367.0	367.0	38.0
CD4066BM96G4	SOIC	D	14	2500	333.2	345.9	28.6
CD4066BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4066BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4066BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

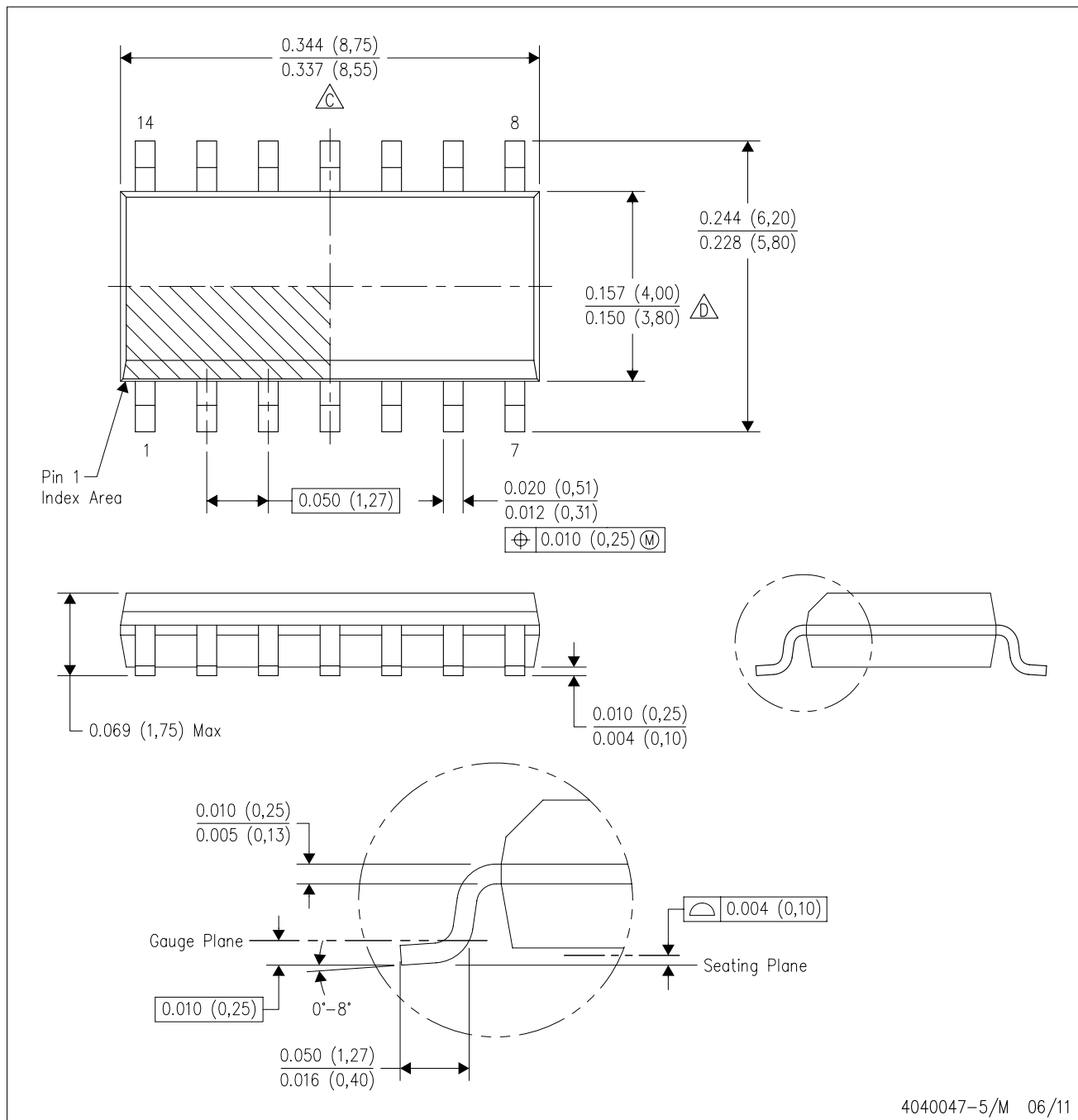


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

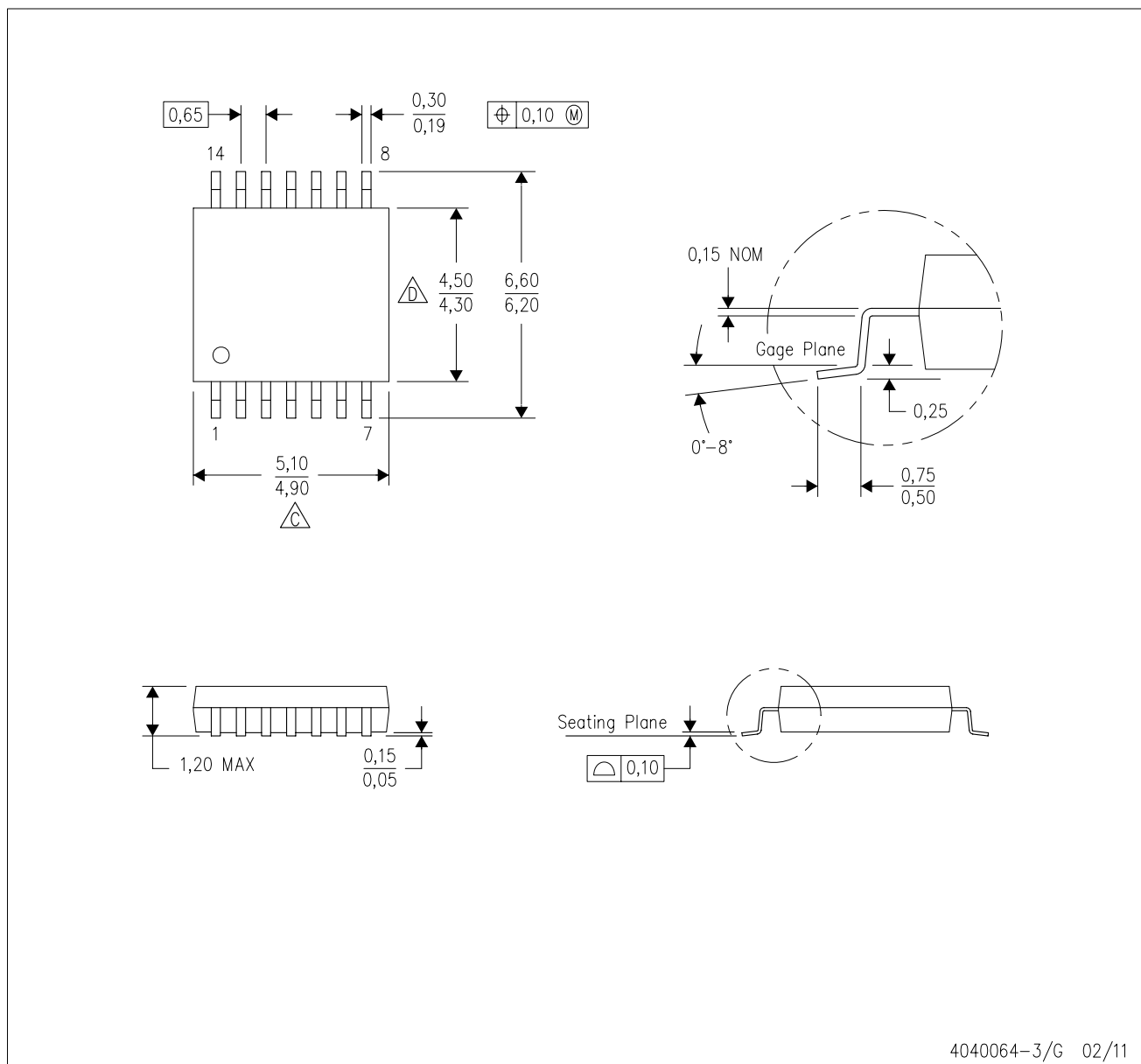
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

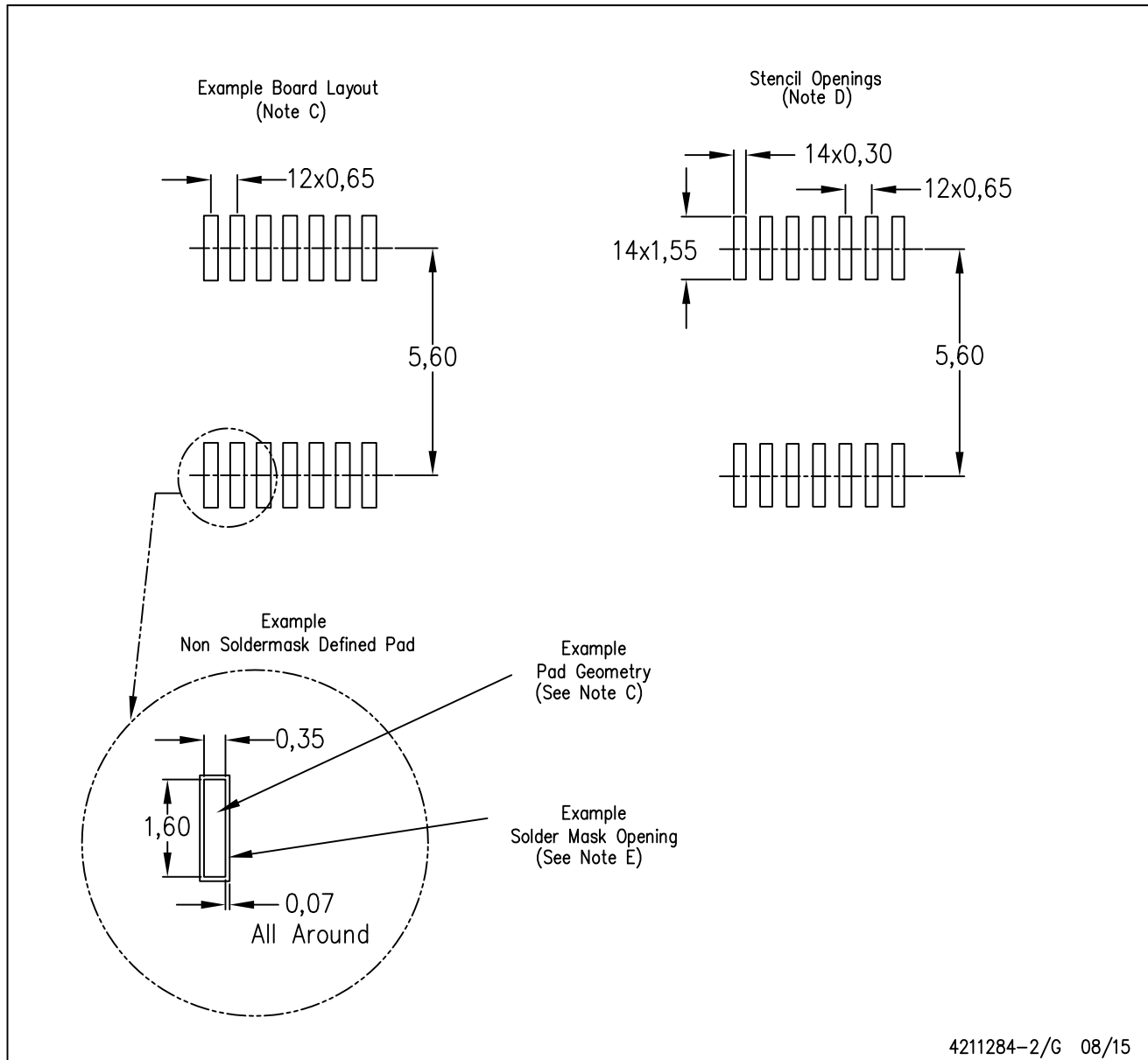
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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