

## High performance, Current Source

### For Parallel White-LED Driver

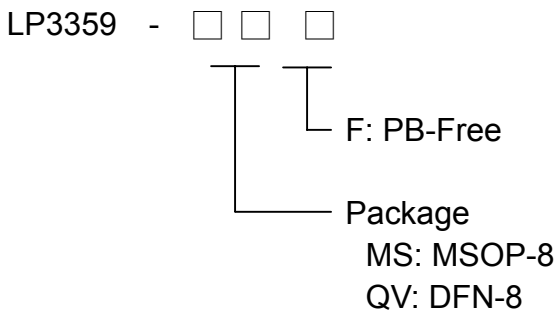
### General Description

The LP3359 is a parallel white-LED driver with four matched current outputs. It can supply a total output current of 100mA over an input voltage range of 3.0V to 5.5V. The amount of constant current sourced to the outputs is user selectable using one external sense resistor. LP3359 typically draws 0.01 $\mu$ A when placed in shutdown, and 180 $\mu$ A when operating in the no-load condition. If any of the outputs are not used, leave the pin(s) unconnected.

Brightness can be controlled by PWM techniques or by adding a DC voltage. A PWM signal can be applied to the EN/PWM pin to vary the perceived brightness of the LED.

The LP3359 uses an active-high enable level. The LP3359 is available in DFN-8 and TSSOP-8 package.

### Ordering Information



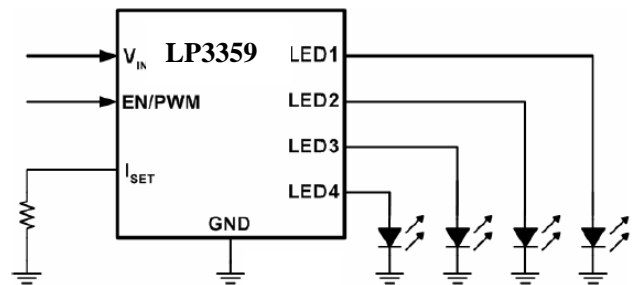
### Features

- ◆ Regulated IOUT With  $\pm 0.3\%$  Matching Between Constant Current Outputs
- ◆ Drives One, Two, Three or Four White LED's with No Ballast Resistors
- ◆ 3.0V to 5.5V Input Voltage
- ◆ Up to 100mA Output Current
- ◆ Active-High Enable
- ◆ Very Small Solution Size
- ◆ Very Low Shutdown Current (0.01 $\mu$ A typical)
- ◆ Available in DFN-8 ,TSSOP-8 Package
- ◆ RoHS Compliant and 100% Lead(Pb)-Free

### Applications

- ✧ Cellular and Smart mobile phone
- ✧ PDA/DSC
- ✧ LCD Display

### Typical Application Circuit



### Pin Configurations

Part Number	Pin Configurations	Part Number	Pin Configurations
DFN-8	<p>(Top View)</p>	TSSOP-8	<p>(Top View)</p>

## Functional Pin Description

Pin Number	Pin Name	Pin Function
1	V <sub>in</sub>	Input Voltage
2	GND	Power Ground.
3	EN/PWM	Active-High Enable Input – There is no internal pull-down resistor.
4	I <sub>set</sub>	Current Set Input-The resistor value tied between this pin and ground sets the output current.
5-8	LEDx	Current Source Outputs 1- 4 - Connect directly to LED's

## Function Block Diagram

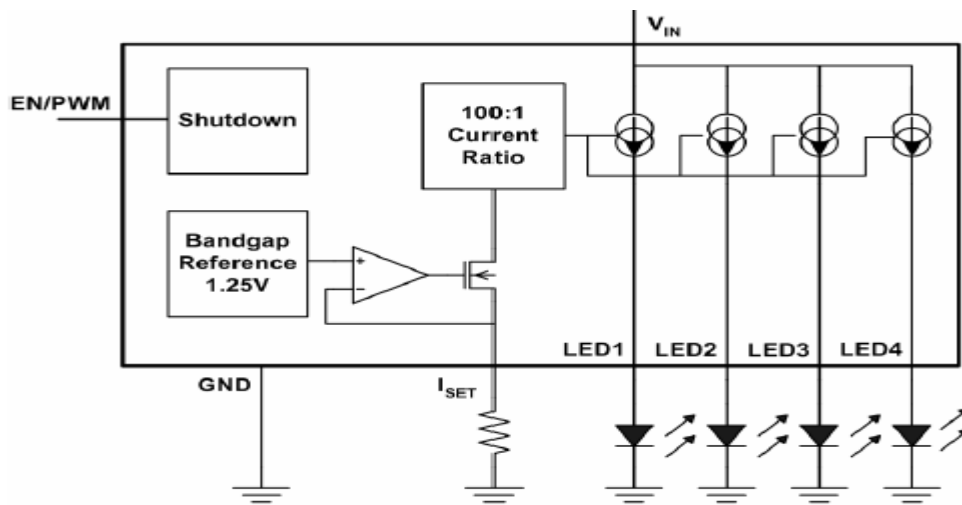


Fig1. LP3359 Block Diagram

## Absolute Maximum Ratings

V <sub>IN</sub> .....	0.3V to 6V max
EN/PWM.....	-0.3V to (V <sub>IN</sub> +0.3V) w/ 6 max
Continuous Power Dissipation .....	Internally Limited
DFN-8L , 3 × 3, θ <sub>JA</sub> .....	50°C/W
TSSOP-8L , θ <sub>JA</sub> .....	70°C/W
Junction Temperature (T <sub>J</sub> ) .....	150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temp (Soldering, 5sec) .....	260°C
ESD Rating Human Body Model .....	-2kV

## Operating Conditions

Input Voltage (V <sub>IN</sub> ) .....	3V to 5.5V
Ambient Temperature (T <sub>A</sub> ) .....	-40°C to 85°C

## Electrical Characteristics

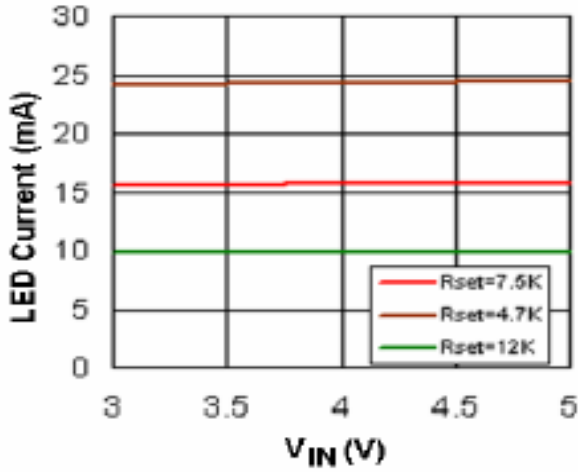
(Limits in standard typeface and typical values apply for TA=25°C. Limits in **boldface** type apply over the operating junction temperature range (-40°C~+85°C). Unless otherwise specified: VIN=5V, VLEDX=3.6V, RSET=7.5k, V(EN/PWM)=VIN.)

Symbol	Description	Conditions	Min	Typ	Max	Units
ILEDx	LED Current	$3.0V \leq V_{IN} \leq 5.5V$ $2.0V \leq V_{LEDX} \leq (V_{IN}-0.4V)$ RSET=7.5k	14.3	15.8	17.3	mA
ILEDX-MATCH	Current Matching Between Any Two Outputs			±0.3	±1	%
VSET	ISET Pin Voltage		1.06 (-8%)	1.18	1.3 (+8%)	V
ILEDX/ISET	Output Current to Current Set Ratio			100		
VHR	Current Source Headroom Voltage	ILED=95% × ILED(nom), RSET= 4.7K (ILED(nom) approx. 25mA) ILED=95% × ILED(nom), RSET= 12K (ILED(nom) approx. 10mA)		320 130	440 220	mV
Iq	Quiescent Supply Current	ILED=0mA, RSET=Open ILED=0mA, RSET=7.5k		175 325	285	uA
ISHUT-DOWN	Shutdown Supply Current	EN/PWM=0		0.01	1	V

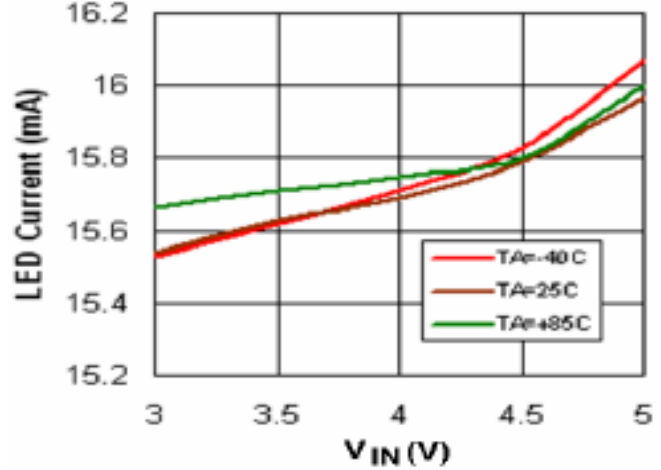
**Typical Operating Characteristics**

Typical Operating Characteristics

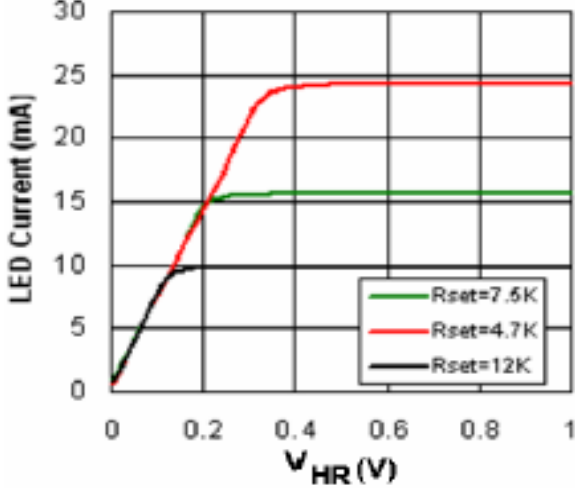
LED Current vs Power Supply



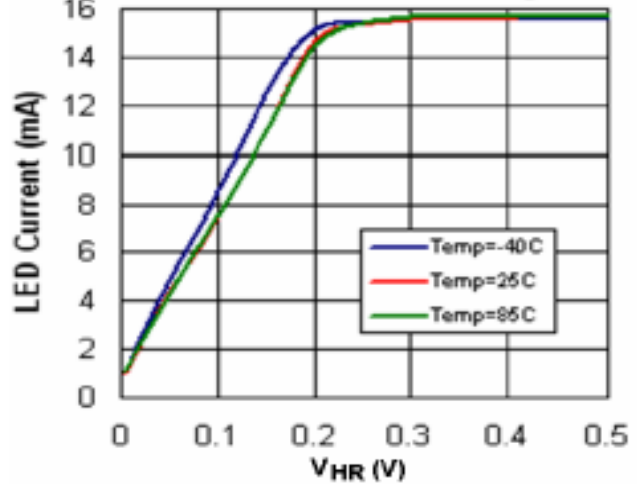
LED Current vs Power Supply



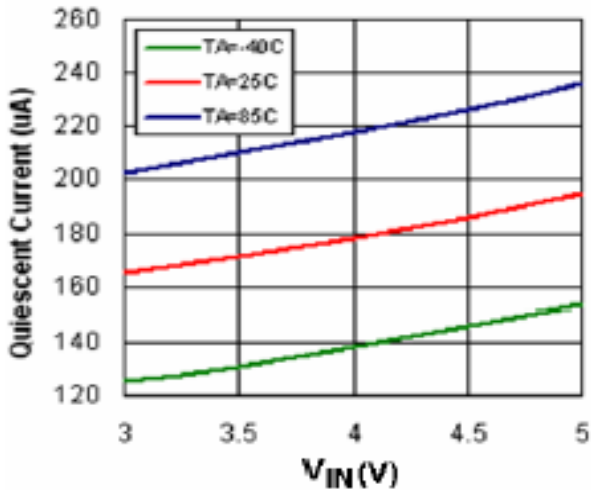
I<sub>led</sub> vs Headroom Voltage



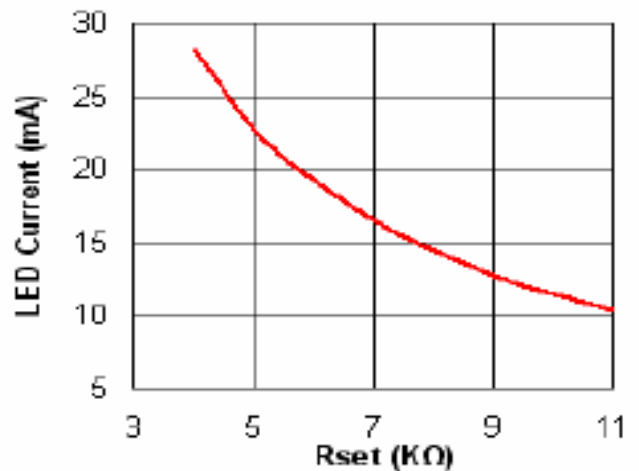
I<sub>led</sub> vs Headroom Voltage



Quiescent Current vs Power Supply



LED Current vs Set Resistor



## Applications Information

### Enable/Shutdown

When the voltage on the active-high-logic enable pin is low, the LP3359 will be in shutdown. While disabled, the LP3359 typically draws 0.01µA. There is no internal pull-up or pull-down on the PWM pin of the LP3359, Do not let PWM pin floating.

### Output Current Capability

The LP3359 is capable of providing up to 25mA of current to each of the four outputs given an input voltage of 3.0V to 5.5V. The outputs have a typical current matching of ± 0.3% between adjacent sources. An external resistor can be used to set the output current, as approximated with the following the equation:

$$R_{SET} = 100 \times (1.18V / I_{LEDX})$$

In order for the output currents to be regulated properly, sufficient headroom voltage (VHR) must be present. The headroom voltage refers to the minimum amount of voltage that must be present across the current source in order to ensure the desired current is realizable. To ensure the desired current is obtained, apply the following equations to find the minimum input voltage required:

$$V_{IN} - V_{LEDX} \geq V_{HR}$$

VLEDX is the diode forward voltage, and VHR is defined by the following equation:

$$V_{HR} = K_{HR} \times (0.95 \times I_{LEDX})$$

ILEDX is the desired diode current, and kHR, typically 15mV/mA in the LP3359, is a proportionality constant that represents the ON-resistance of the internal current mirror transistors. For worst-case design calculations, using a kHR of 20mV/mA is recommended. (Worst-case recommendation accounts for parameter shifts from part-to-part variation and applies over the full operating temperature range). Changes in headroom voltage from one output to the next, possible with LED forward voltage mismatch, will result in different output currents and LED brightness mismatch. Thus, operating the LP3359 with insufficient headroom voltage across all current sources

should be avoided.

**Table 1. ILEDX, RSET and VHR-MIN  
kHR= 20 mV/mA (worst-case)**

I <sub>OUT</sub>	R <sub>SET</sub>	V <sub>HEADROOM</sub>
10mA	12kΩ	200mV
15mA	7.5kΩ	300mV
25mA	4.7kΩ	500mV

### Brightness Control

#### (1)Using a PWM Signal to EN/PWM Pin

Brightness control can be implemented by pulsing a signal at the PWM pin. The RSET value should be selected using the RSET equation. LED brightness is proportional to the duty cycle (D) of the PWM signal. For linear brightness control over the full duty cycle adjustment range, the PWM frequency (f) should be limited to accommodate the turn-on time (TON = 20µs) of the de- vice.

$$D \cdot (1/f) > T_{ON}$$

$$f_{MAX} = D_{MIN} / T_{ON}$$

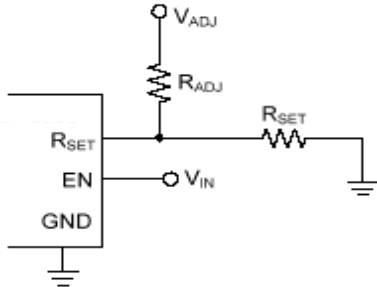
If the PWM frequency is much less than 100Hz, flicker may be seen in the LEDs. For the LP3359, zero duty cycle will turn off the LEDs and a 50% duty cycle will result in an average ILED being half of the programmed LED current. For example, if RSET is set to program 15mA, a 50% duty cycle will result in an average ILED of 7.5mA, LED being half the programmed LED current. RSET should be chosen not to exceed the maximum current delivery capability of the device.

#### (2)Using a DC Voltage Added to RSET

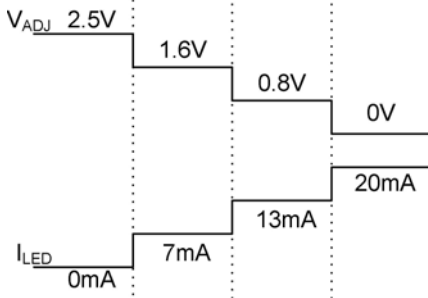
Using an analog input voltage VADJ via a resistor RADJ connects to the RSET pin can also be used to achieve setting LED current. Figure 3 shows this application circuit. For this application the LED's current can be derived from the following Equation. Figure 4 and table 2 shows the relation between VADJ and ILED of a typical application example, where the VADJ from 0 to 2.5V, RSET equals 11.5kΩ and RADJ

equals 12.5kΩ.

$$I_{LED} = 100 \times \left[ 1.18 \times \left( \frac{1}{R_{SET}} + \frac{1}{R_{ADJ}} \right) - \frac{V_{ADJ}}{R_{ADJ}} \right]$$



**Figure3. The Application Circuit of Brightness which Uses a DC Voltage Into R<sub>SET</sub>**



**Figure4. LED current setting example which using a DC voltage to Rset**

**Table 2. The LED Current vs V<sub>ADJ</sub> With R<sub>ADJ</sub>=12.5KΩ and R<sub>SET</sub>=11.5KΩ**

V <sub>ADJ</sub> (V)	0	0.2	0.4	0.6	0.8	1	1.2
I <sub>LED</sub> (mA)	19.7	18.1	16.5	14.9	13.3	11.7	10.1
V <sub>ADJ</sub> (V)	1.4	1.6	1.8	2	2.2	2.4	2.5
I <sub>LED</sub> (mA)	8.5	6.9	5.3	3.7	2.1	0.5	0

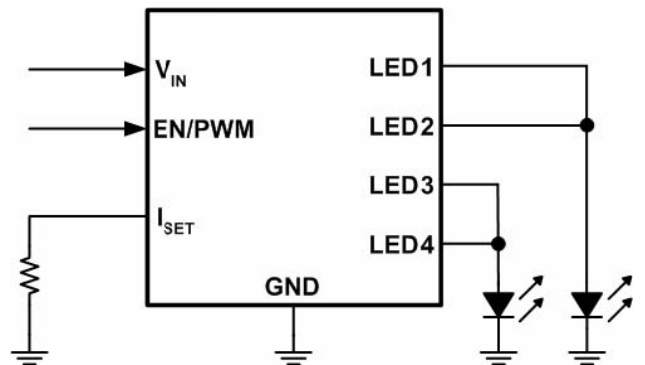
**LED Selection**

The LP3359 is designed to drive white-LEDs with a typical forward voltage of 3.0V to 4.0V. The maximum LED forward voltage that the LP3359 can accommodate is highly dependant upon V<sub>IN</sub> and I<sub>LEDX</sub> (See the section on Output Current Capability for more information on finding maximum V<sub>LEDX</sub>.) For applications that demand color and brightness matching, care must be taken to select LEDs from the same chromaticity group. Forward current matching is assured over

the LED process variations due to the constant current outputs of the LP3359.

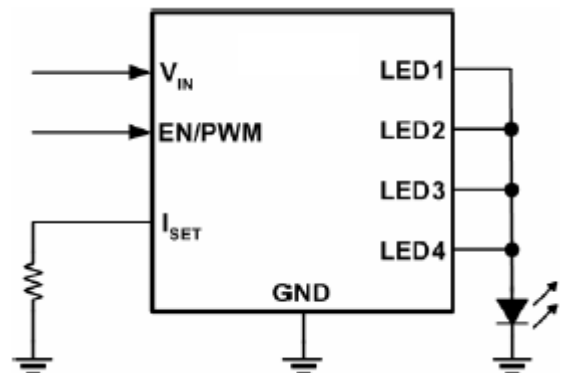
**Parallel LEDx Outputs for Increased Current Driver**

Outputs LED1 through LED4 may be connected together in any combination to drive higher currents through fewer LEDs. For example in Figure 5, outputs LED1 and LED2 are connected together to drive one LED while LED3 and LED4 are connected together to drive a second LED.



**Figure 5. Two Parallel Connected LEDs**

With this configuration, two parallel current sources of equal value provide current to each LED. R<sub>SET</sub> should therefore be chosen so that the current through each output is programmed to 50% of the desired current through the parallel connected LEDs. For example, if 30mA is the desired drive current for 2 parallel connected LEDs, R<sub>SET</sub> should be selected so that the current through each of the outputs is 15mA. Other combinations of parallel outputs may be implemented in similar fashions, such as in Figure 6.



**Figure 6. One Parallel Connected LED**

Connecting outputs in parallel does not affect internal operation of the LP3359 and has no impact on the Electrical Characteristics and limits previously presented. The available diode output current, maximum diode voltage, and all other specifications provided in the Electrical Characteristics table apply to parallel output configurations, just as they do to the standard 4-LED application circuit.

**Power Consumption**

It is recommended that power consumed by the circuit ( $V_{IN} \times I_{IN}$ ) be evaluated rather than power efficiency. Figure 7 shows the power consumption of the LP3359 Typical Application Circuit.

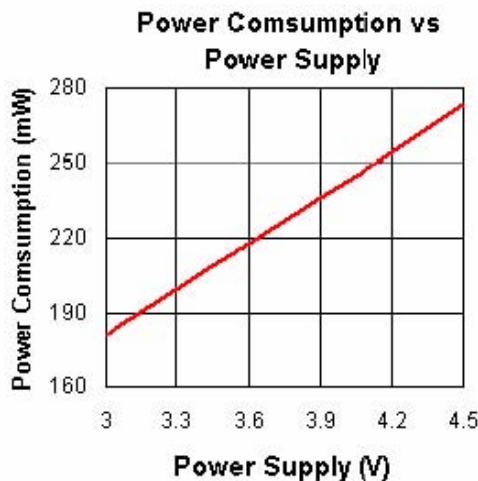


Figure 7. 4LEDs, LED VF=2.7V, ILED=15mA Power Dissipation  
 The maximum allowable power dissipation that this package is capable of handling can be determined as follows:

$$P_{DMax} = (T_{JMax} - T_A) / \theta_{JA}$$

Where T is the maximum junction temperature, T is the ambient temperature, and  $\theta_{JA}$  is the junction -to-ambient thermal resistance of the specified package. The LP3359 come in the DFN-8 package that has a junction-to-ambient thermal resistance ( $\theta_{JA}$ ) equal to 50°C/W. This value of  $\theta_{JA}$  is highly dependant upon the layout of the PC board. The actual power dissipated by the LP3359 follows the equation:

$$P_{DISS} = (V_{IN} \times I_{IN}) - N(V_{LEDX} \times I_{LEDX})$$

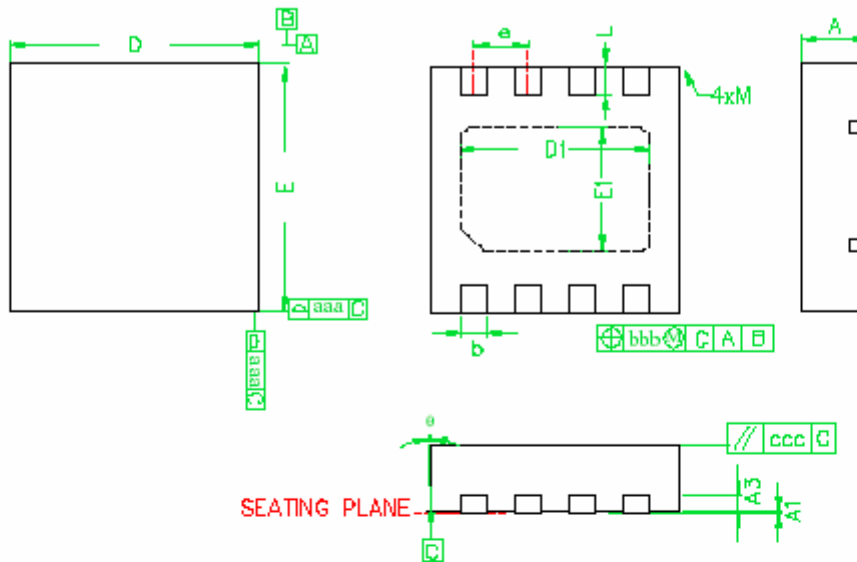
Where N equals the number of active outputs,  $V_{LEDX}$  is the LEDX LED forward voltage, and  $I_{LEDX}$  is the current supplied to the LEDX diode by the LP3359. Power dissipation must be less than that allowed by the package. Please refer to the Absolute Maximum Rating of the LP3359.

**Input Capacitor Selection**

The LP3359 is designed to run off of a fixed input voltage. Depending on the stability and condition of this voltage rail, it may be necessary to add a small input capacitor to help filter out any noise that may be present on the line. In the event that filtering is needed, surface mount multi-layer ceramic capacitors are recommended. These capacitors are small and inexpensive. A capacitance of 0.1µF is typically sufficient.

Applications Information

DFN-8

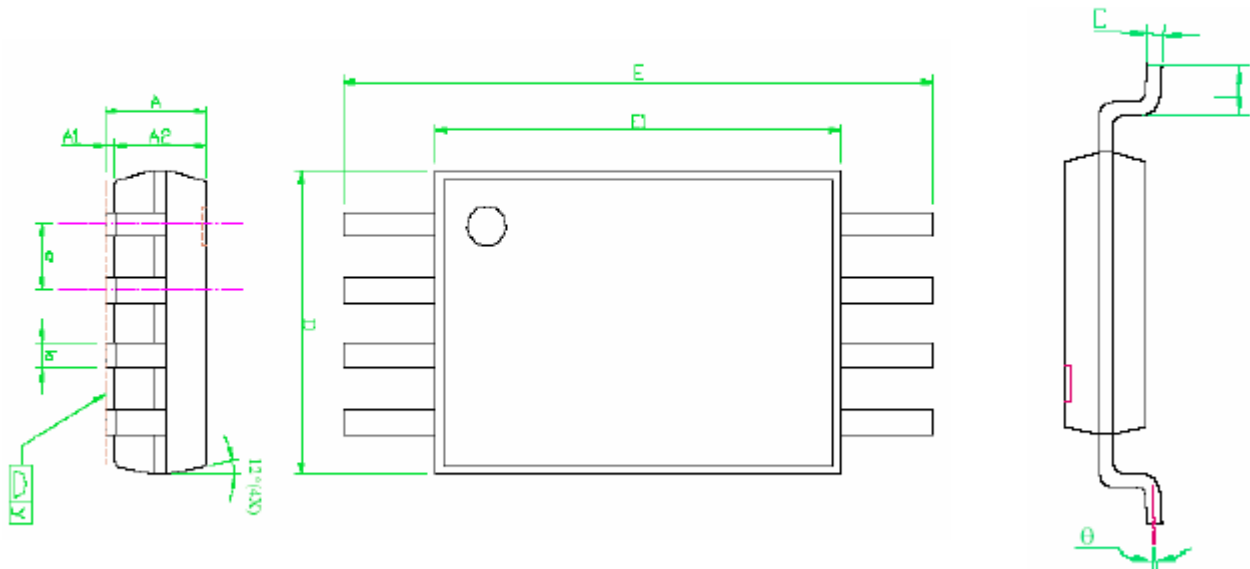


NOTE

1. All dimensions are in millimeters,  $\theta$  is in degrees
2. M: The maximum allowable corner on the molded plastic body corner
3. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side
4. Dimension E does not include interterminal mold protrusions or terminal protrusions. Interterminal mold protrusions and/or terminal protrusions shall not exceed 0.20mm per side
5. Dimension b applies to plated terminals. Dimension A1 is primarily Y terminal plating, but may or may not include a small protrusion of terminal below the bottom surface of the package
6. Burr shall not exceed 0.060mm
7. JEDEC MO-229

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.81	0.9	1.00
A1	0	0.015	0.03
A3	-----	0.20 REF	-----
B	0.25	0.30	0.37
D	2.85	3.00 BSC	3.15
D1	-----	2.3 BSC	-----
E	2.85	3.00 BSC	3.15
E1	-----	1.5 BSC	-----
e	-----	0.65 BSC	-----
L	0.25	0.35	0.45
aaa	-----	0.25	-----
bbb	-----	0.10	-----
ccc	-----	0.10	-----
M	-----	-----	0.05
$\theta$	-12	-----	0



**8-Pin TSSOP**

**NOTE**

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance  $\pm 0.10\text{mm}$  unless otherwise specified
3. Coplanarity: 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Followed from JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.20	-----	-----	0.048
A1	0.05	-----	0.15	0.002	-----	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
$\theta$	0	-----	8	0	-----	8