V53C516400A
4M x 4 FAST PAGE MODE CMOS DYNAMIC RAM

V53C516400A	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	25 ns	30 ns
Min. Page Mode Cycle Time, (t_{PC})	35 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	84 ns	104 ns

Features

- 4M x 4-bit organization
- Fast Page Mode for a sustained data rate of 50 MHz
- $\overline{RAS}$ access time: 50, 60 ns
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 24/26-pin 300 mil SOJ, and 24/26-pin 300 mil TSOP-II
- Single +5V ±10% Power Supply
- TTL Interface

Description

The V53C516400A is a 4,194,304 x 4 bit high-performance CMOS dynamic random access memory. The V53C516400A offers Page mode operation. The V53C516400A has asymmetric address, 12-bit row and 10-bit column.

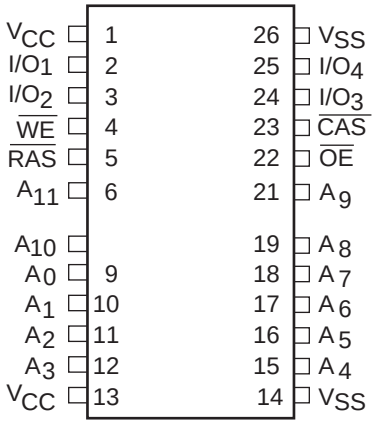
All inputs are TTL compatible. Fast Page Mode operation allows random access up to 1024 x 4 bits, within a page, with cycle times as short as 35ns.

These features make the V53C516400A ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	K	T	50	60	Std.	
0°C to 70°C	•	•	•	•	•	Blank

24/26-Pin Plastic SOJ/TSOP-II PIN CONFIGURATION Top View



311640002-02

Pin Names

A_0–A_{11}	Row, Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{CC}	5V Supply
V_{SS}	0V Supply
NC	No Connect

Description	Pkg.	Pin Count
SOJ	K	26/24
TSOP-II	T	26/24

Absolute Maximum Ratings*

Operating temperature range .....0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Input/output voltage .... -0.5 to min (V_{CC}+0.5, 4.6) V
Power supply voltage .....-1.0 to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

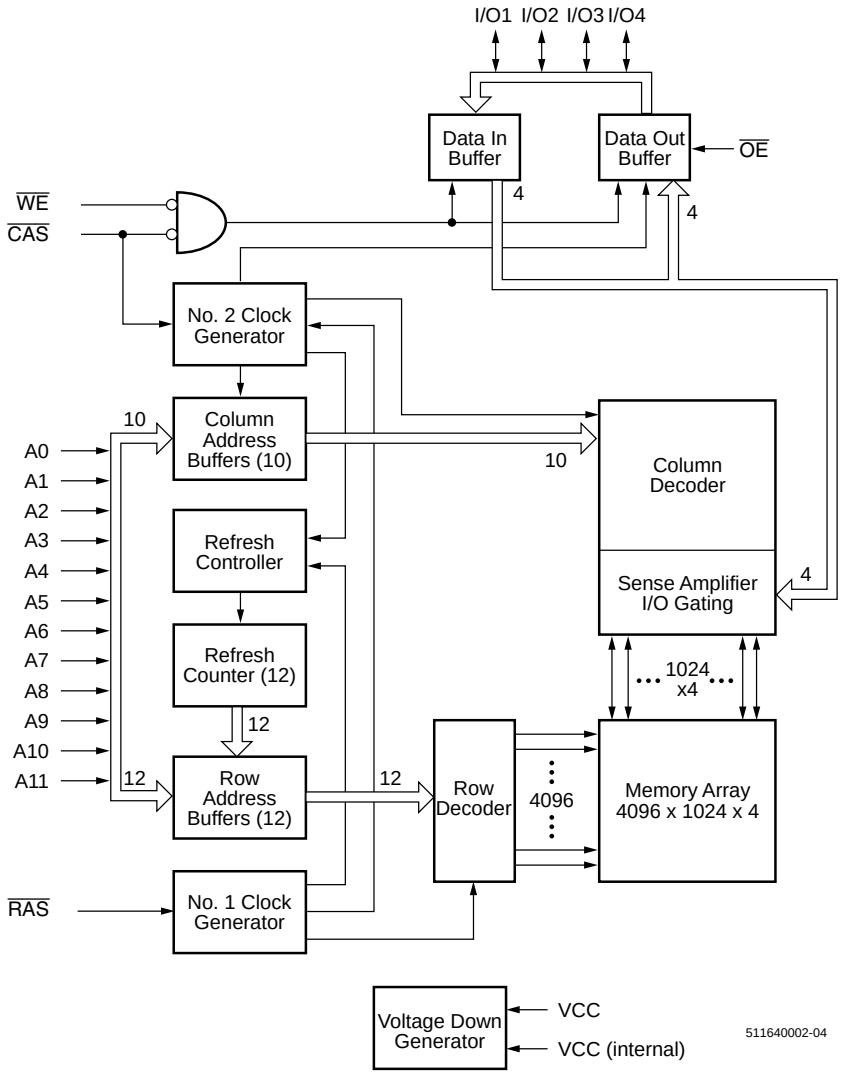
T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

***Note:** Capacitance is sampled and not 100% tested.

Block Diagram

4096 x 4



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C516400A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	µA	$V_{SS} \le V_{IN} \le V_{CC}$	1
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	1
I_{CC1}	V_{CC} Supply Current, Operating	50			50	mA	$t_{RC} = t_{RC}$ (min.)	2, 3, 4
		60			40			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	50			50	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60			40			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	50			25	mA	Minimum Cycle	2, 3, 4
		60			20			
I_{CC5}	V_{CC} Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh	50			50	mA		2, 4
		60			40			
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1.0	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V other input ≥ V_{SS}	1
V_{CC}	Power Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		–0.5		0.8	V		1
V_{IH}	Input High Voltage		2.4		V_{CC} + 0.5	V		1
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 4.2 mA	1
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –5 mA	1

AC Characteristics[5,6]

T_A = 0 to 70 ˚C,V_{CC} = 5V ±10%, t_T = 2 ns

#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Common Parameters								
1	t_{RC}	Random read or write cycle time	90	–	110	–	ns	
2	t_{RP}	$\overline{RAS}$ precharge time	30	–	40	–	ns	
3	t_{RAS}	$\overline{RAS}$ pulse width	50	10k	60	10k	ns	
4	t_{CAS}	$\overline{CAS}$ pulse width	13	10k	15	10k	ns	
5	t_{ASR}	Row address setup time	0	–	0	–	ns	
6	t_{RAH}	Row address hold time	8	–	10	–	ns	
7	t_{ASC}	Column address setup time	0	–	0	–	ns	
8	t_{CAH}	Column address hold time	10	–	15	–	ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	18	37	20	45	ns	
10	t_{RAD}	$\overline{RAS}$ to column address delay	13	25	15	30	ns	
11	t_{RSH}	$\overline{RAS}$ hold time	13		15	–	ns	
12	t_{CSH}	$\overline{CAS}$ hold time	50		60	–	ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	ns	
14	t_T	Transition time (rise and fall)	3	50	3	50	ns	7
15	t_{REF}	Refresh period	–	64	–	64	ms	
Read Cycle								
16	t_{RAC}	Access time from $\overline{RAS}$	–	50	–	60	ns	8, 9
17	t_{CAC}	Access time from $\overline{CAS}$	–	13	–	15	ns	8, 9
18	t_{CAA}	Access time from column address	–	25	–	30	ns	8,10
19	t_{OEA}	$\overline{OE}$ access time	–	13	–	15	ns	
20	t_{RAL}	Column address to $\overline{RAS}$ lead time	25	–	30	–	ns	
21	t_{RCS}	Read command setup time	0	–	0	–	ns	
22	t_{RCH}	Read command hold time	0	–	0	–	ns	11
23	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0	–	0	–	ns	11
24	t_{CLZ}	$\overline{CAS}$ to output in low-Z	0	–	0	–	ns	8
25	t_{OFF}	Output buffer turn-off delay	0	13	0	15	ns	12
26	t_{OEZ}	Output turn-off delay from $\overline{OE}$	0	13	0	15	ns	12
27	t_{DZC}	Data to $\overline{CAS}$ low delay	0	–	0	–	ns	13
28	t_{DZO}	Data to $\overline{OE}$ low delay	0	–	0	–	ns	13
29	t_{CDD}	$\overline{CAS}$ high to data delay	13	–	15	–	ns	14
30	t_{ODD}	$\overline{OE}$ high to data delay	13	–	15	–	ns	14

AC Characteristics[5,6]

T_A = 0 to 70 ˚C,V_{CC} = 5V ±10%, t_T = 2 ns

#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Write Cycle								
31	t_{WCH}	Write command hold time	8	–	10	–	ns	
32	t_{WP}	Write command pulse width	8	–	10	–	ns	
33	t_{WCS}	Write command setup time	0	–	0	–	ns	15
34	t_{RWL}	Write command to $\overline{RAS}$ lead time	13	–	15	–	ns	
35	t_{CWL}	Write command to $\overline{CAS}$ lead time	13	–	15	–	ns	
36	t_{DS}	Data setup time	0	–	0	–	ns	16
37	t_{DH}	Data hold time	8	–	10	–	ns	16
Read-modify-Write Cycle								
38	t_{RWC}	Read-write cycle time	126	–	150	–	ns	
39	t_{RWD}	$\overline{RAS}$ to WE delay time	68	–	80	–	ns	15
40	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	31	–	35	–	ns	15
41	t_{AWD}	Column address to $\overline{WE}$ delay time	43	–	50	–	ns	15
42	t_{OEH}	$\overline{OE}$ command hold time	13	–	15	–	ns	
Fast Page Mode Cycle								
43	t_{PC}	Fast Page mode cycle time	35	–	40	–	ns	
44	t_{CP}	$\overline{CAS}$ precharge time	10	–	10	–	ns	
45	t_{CPA}	Access time from $\overline{CAS}$ precharge	–	30	–	35	ns	7
46	t_{RASP}	$\overline{RAS}$ pulse width in Fast mode	50	200k	60	200k	ns	
47	t_{RHPC}	$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	30	–	35	–	ns	
Fast Page Mode Read-modify-Write Cycle								
48	t_{PRWC}	Fast Page mode read-write cycle time	71	–	80	–	ns	
49	t_{CPWD}	$\overline{CAS}$ precharge to $\overline{WE}$	48	–	55	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle								
50	t_{CSR}	$\overline{CAS}$ setup time	10	–	10	–	ns	
51	t_{CHR}	$\overline{CAS}$ hold time	10	–	10	–	ns	
52	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	5	–	5	–	ns	
53	t_{WRP}	Write to $\overline{RAS}$ precharge time	10	–	10	–	ns	
54	t_{WRH}	Write hold time referenced to $\overline{RAS}$	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle								
55	t_{CPT}	$\overline{CAS}$ precharge time	35	–	40	–	ns	

AC Characteristics[5,6]

T_A = 0 to 70 ˚C,V_{CC} = 5V ±10%, t_T = 2 ns

#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Test Mode								
56	t_{WTS}	Write command setup time	10	–	10	–	ns	
57	t_{WTH}	Write command hold time	10	–	10	–	ns	
58	t_{CHRT}	$\overline{CAS}$ hold time	30	–	30	–	ns	
59	t_{RAHT}	$\overline{RAS}$ hold time in test mode	30	–	30	–	ns	

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In case of I_{CC4} it can be changed once or less during a Fast Page mode cycle

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume t_T = 2 ns.

7) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

8) Measured with the specified current load and 100 pF at V_{OL} = 0.8 V and V_{OH} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CAA},t_{CPA}, t_{OEA} . t_{CAC} is measured from tristate.

9) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

10) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{CAA}.

11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12) $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

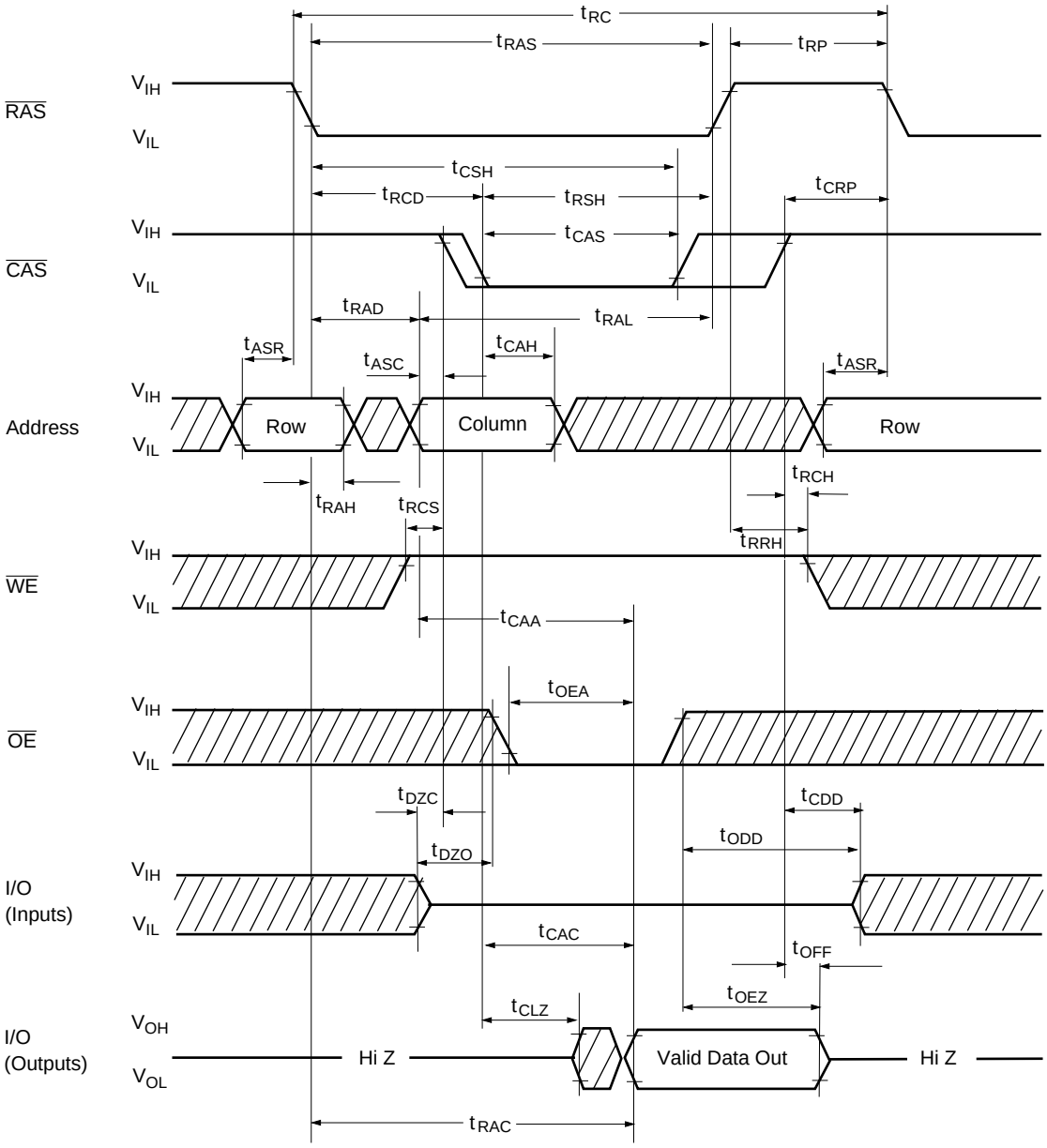
13) Either t_{DZC} or t_{DZO} must be satisfied.

14) Either t_{CDD} or t_{ODD} must be satisfied.

15) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

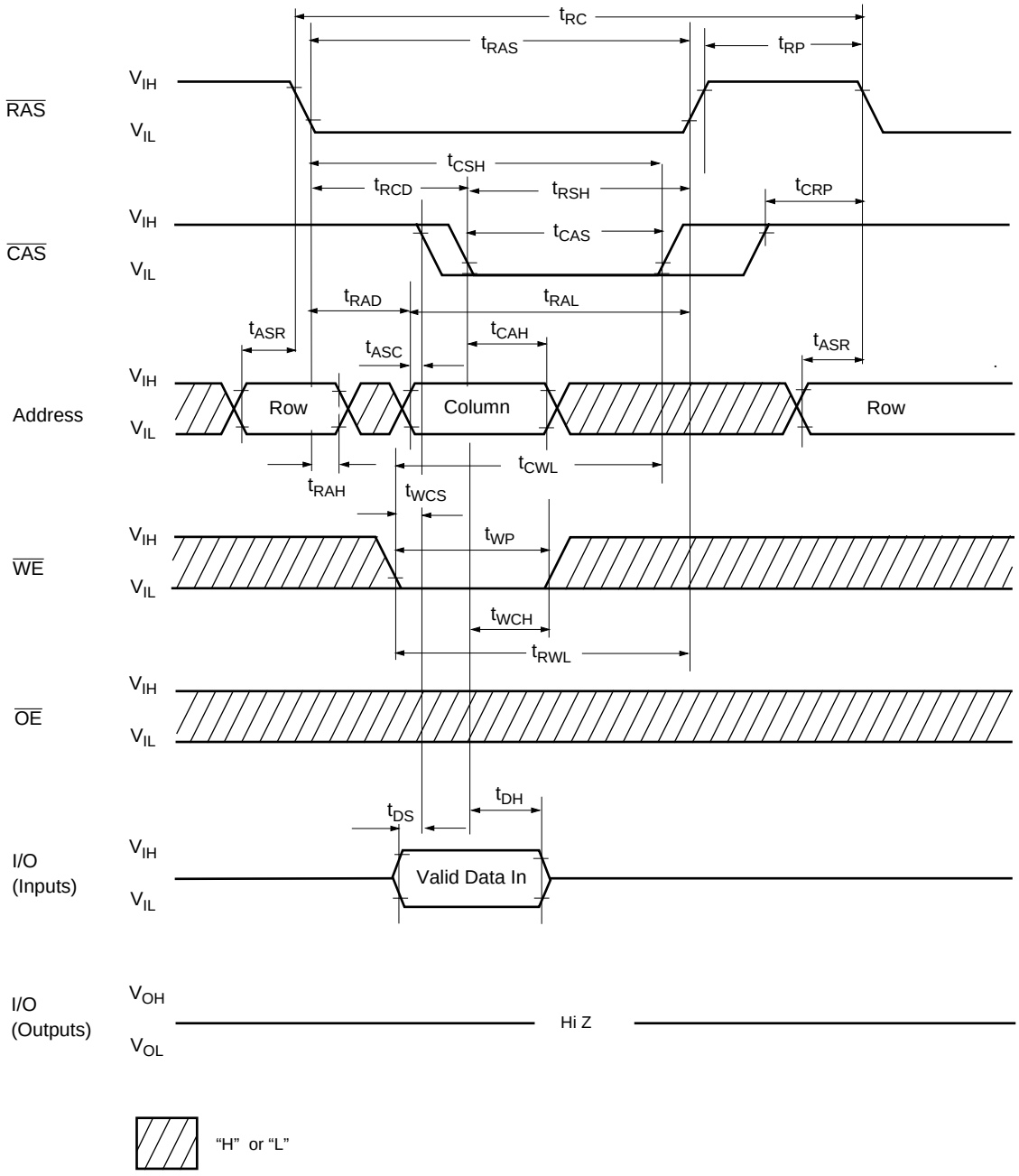
16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

Waveforms of Read Cycle



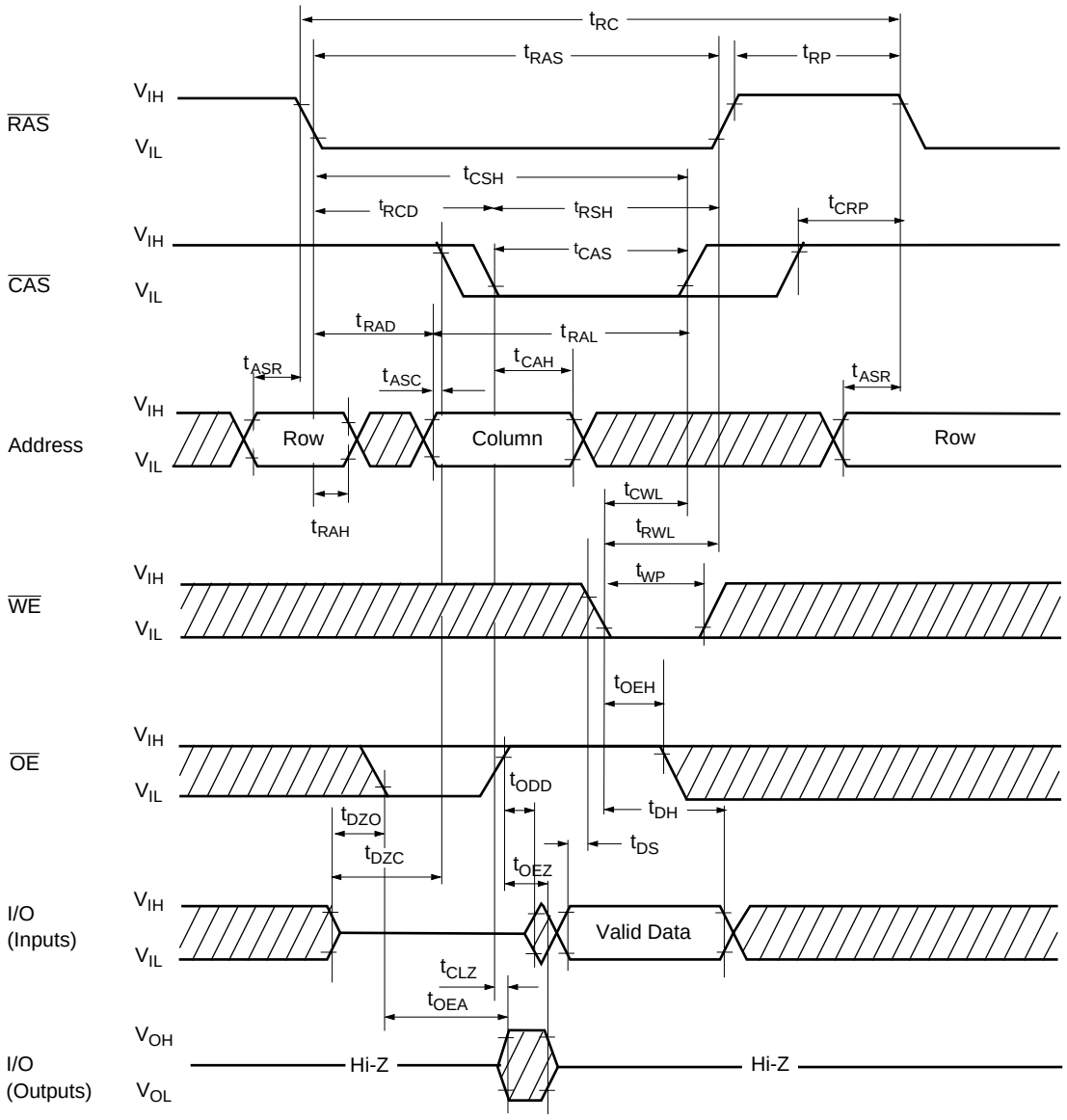
WL1

Waveforms of Write Cycle (Early Write)

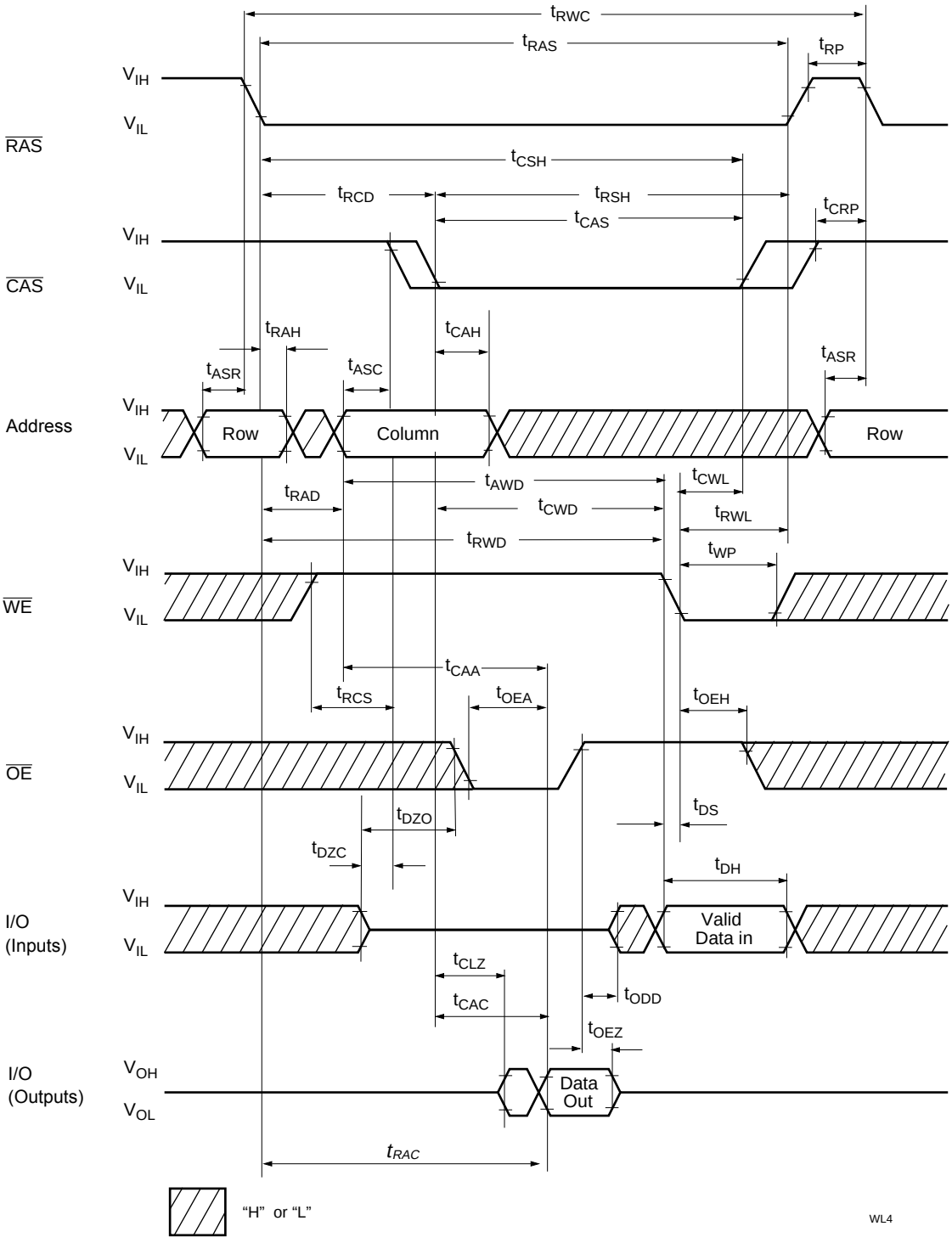


WL2

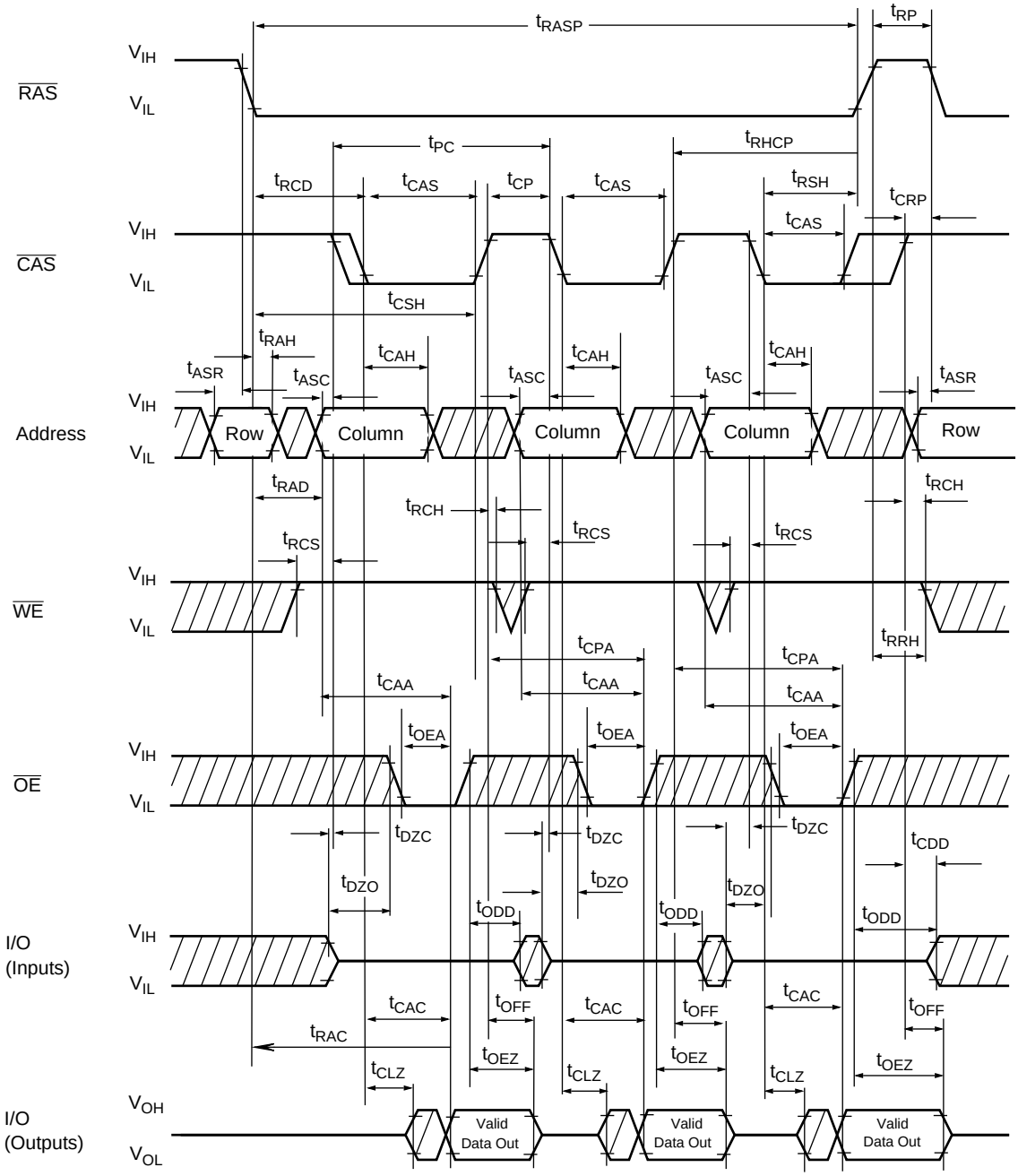
Waveforms of Write Cycle ($\overline{OE}$ Controlled Write)



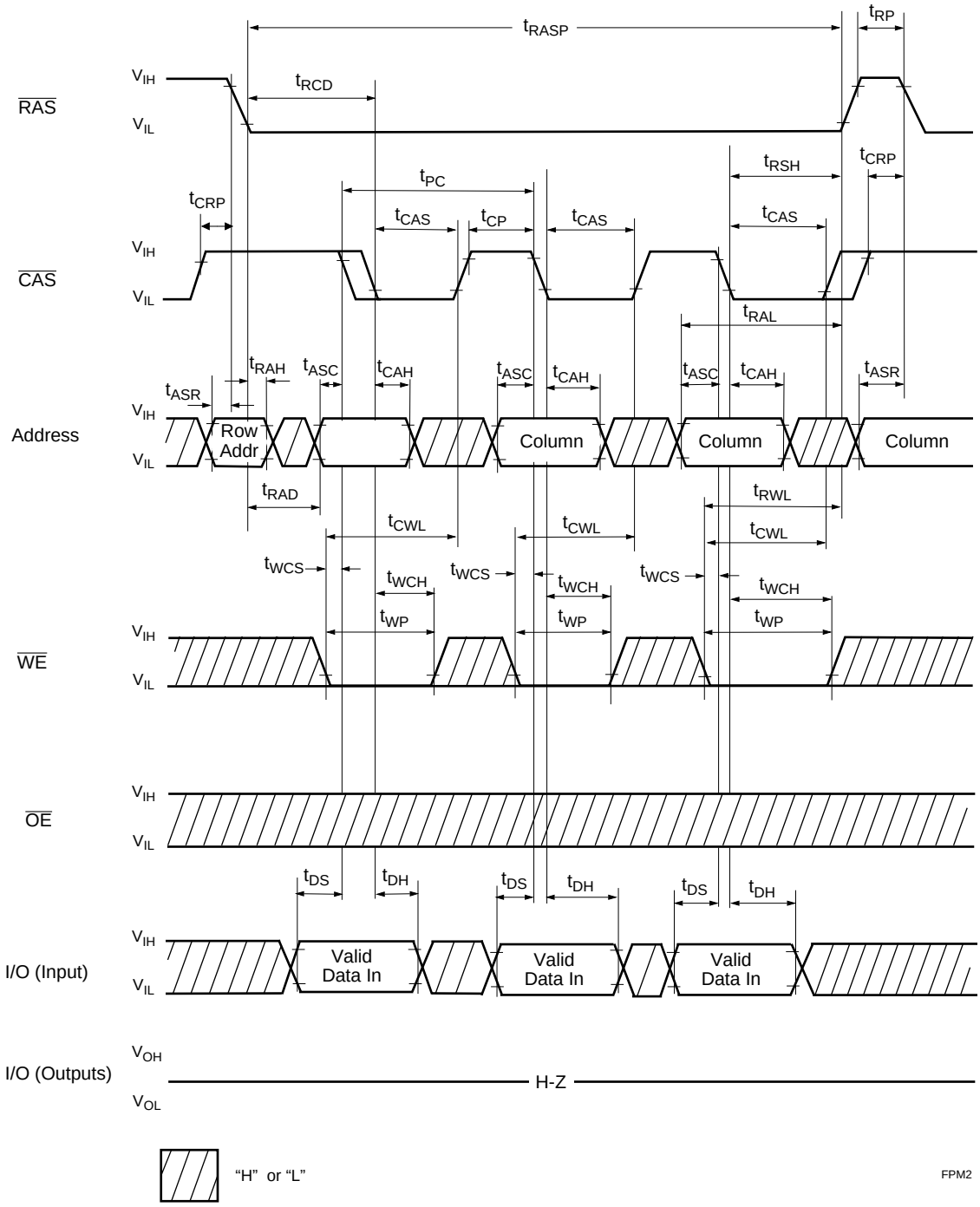
Waveforms of Read-Write (Read-Modify-Write) Cycle



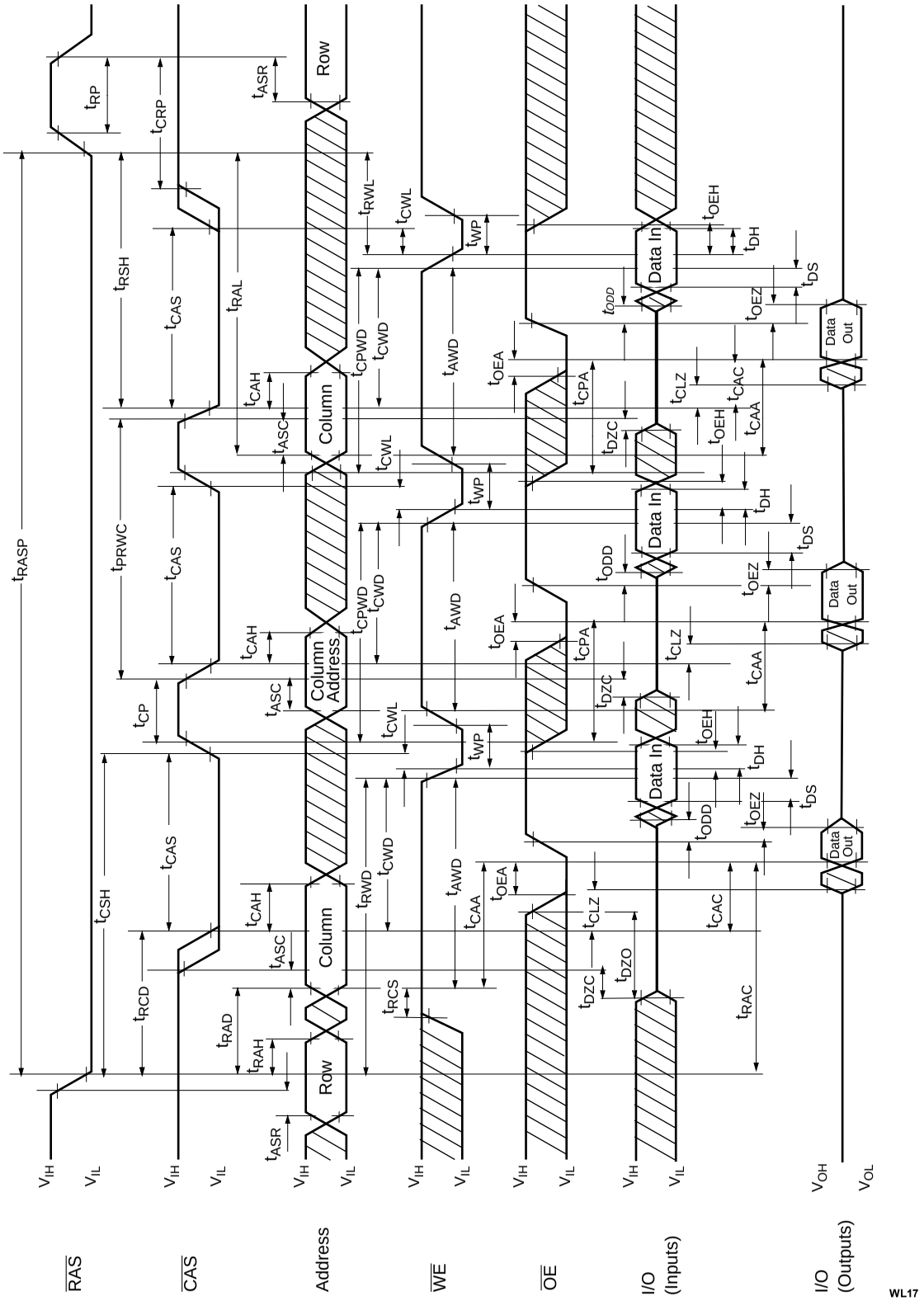
Waveforms of Fast Page Mode Read Cycle



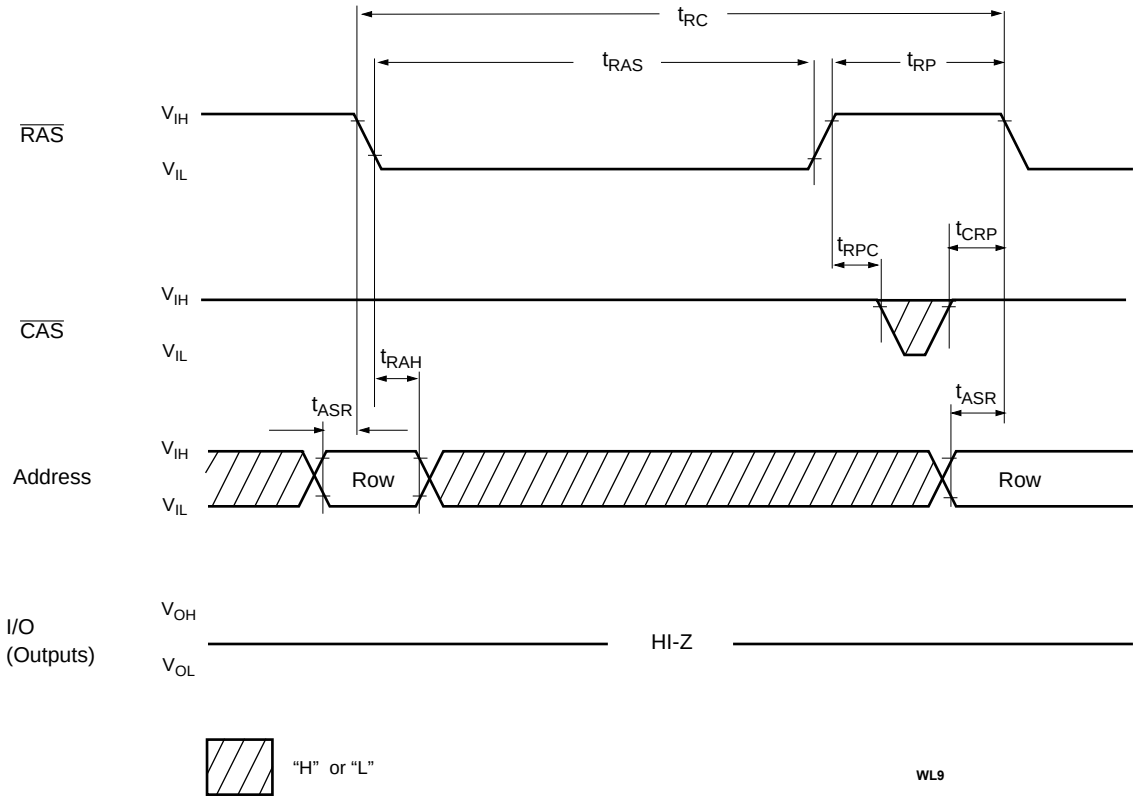
Waveforms of Fast Page Mode Early Write Cycle



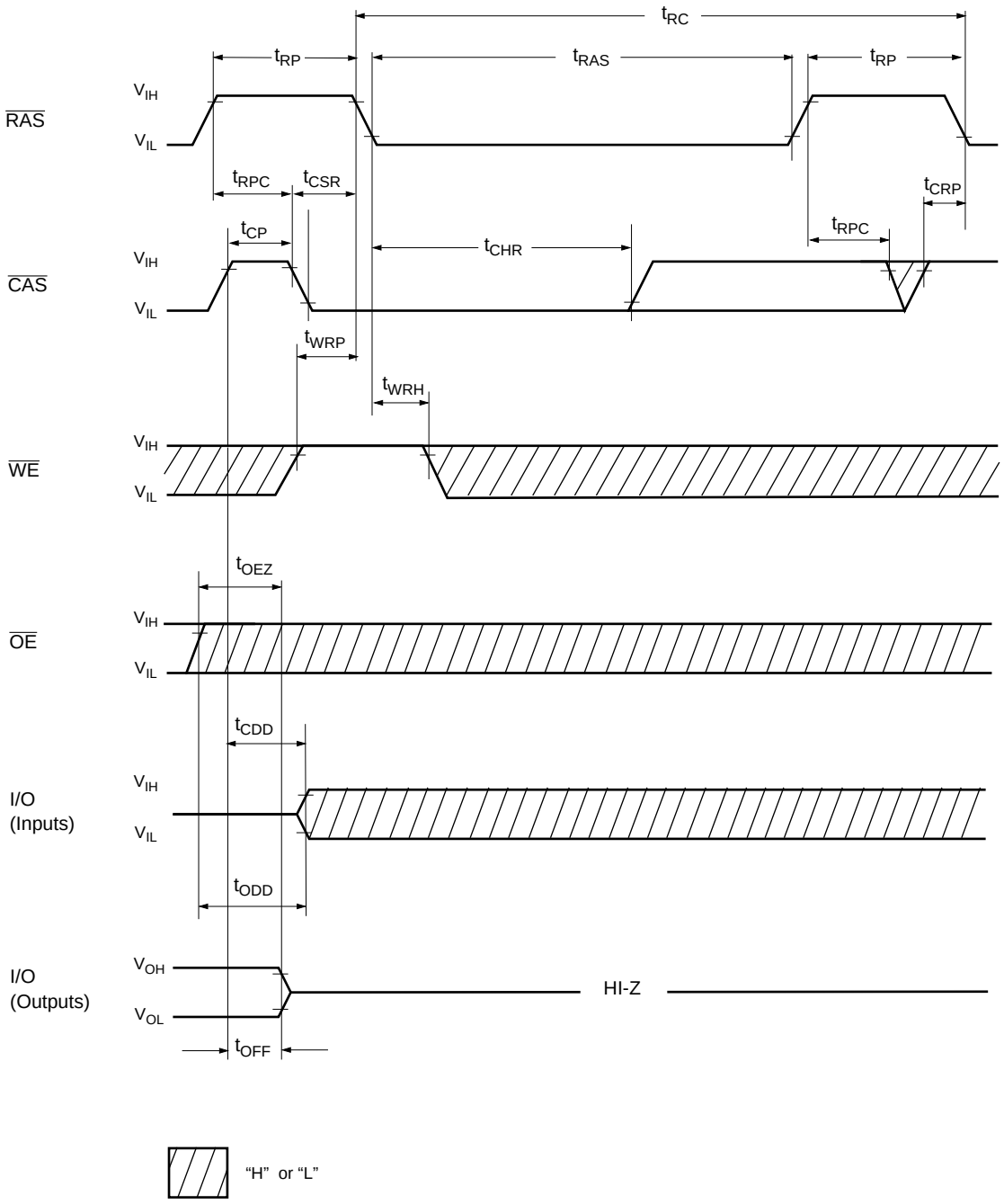
Waveforms of Fast Page Mode Late Write and Read-Modify-Write Cycle



Waveforms of $\overline{RAS}$ Only Refresh Cycle

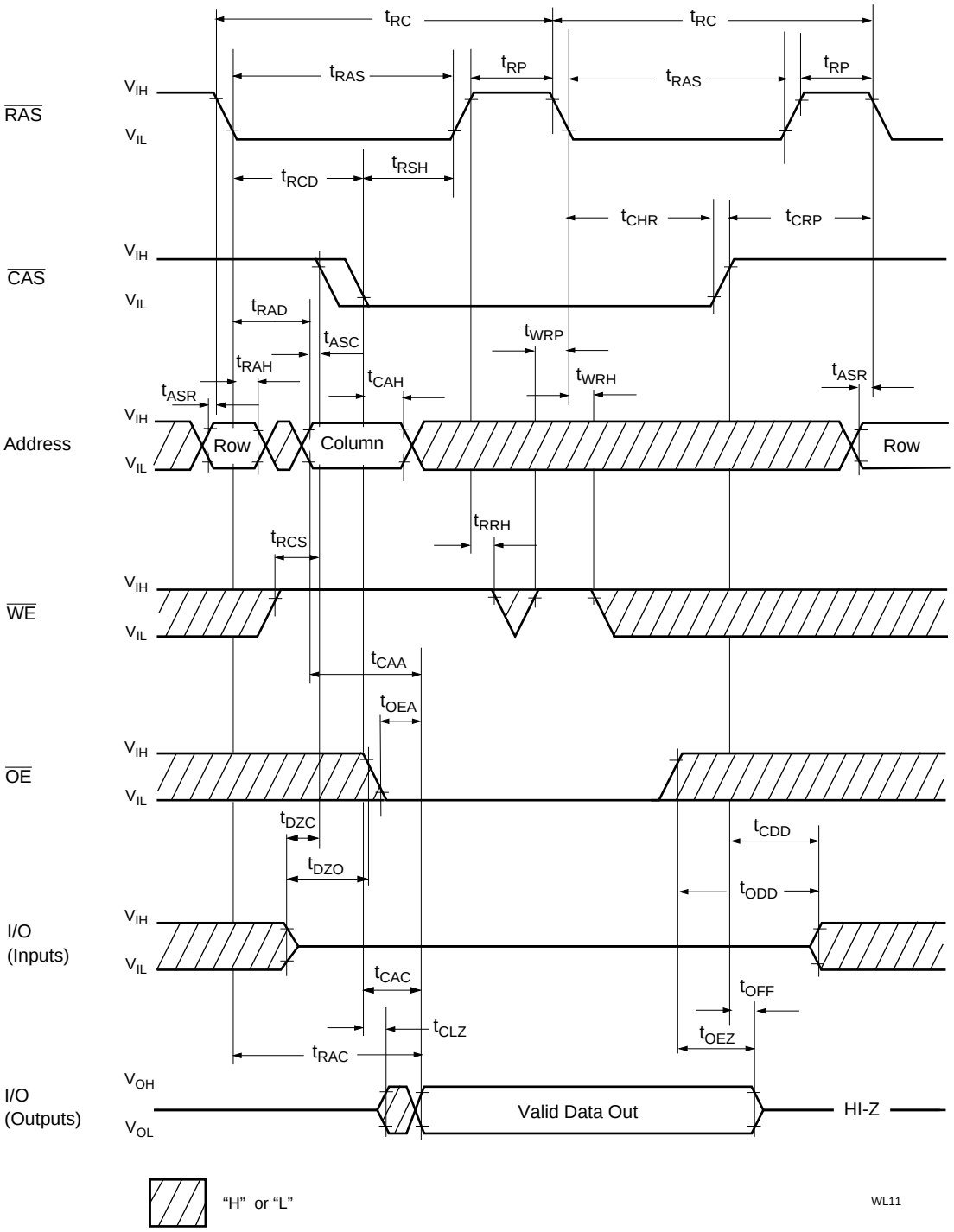


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

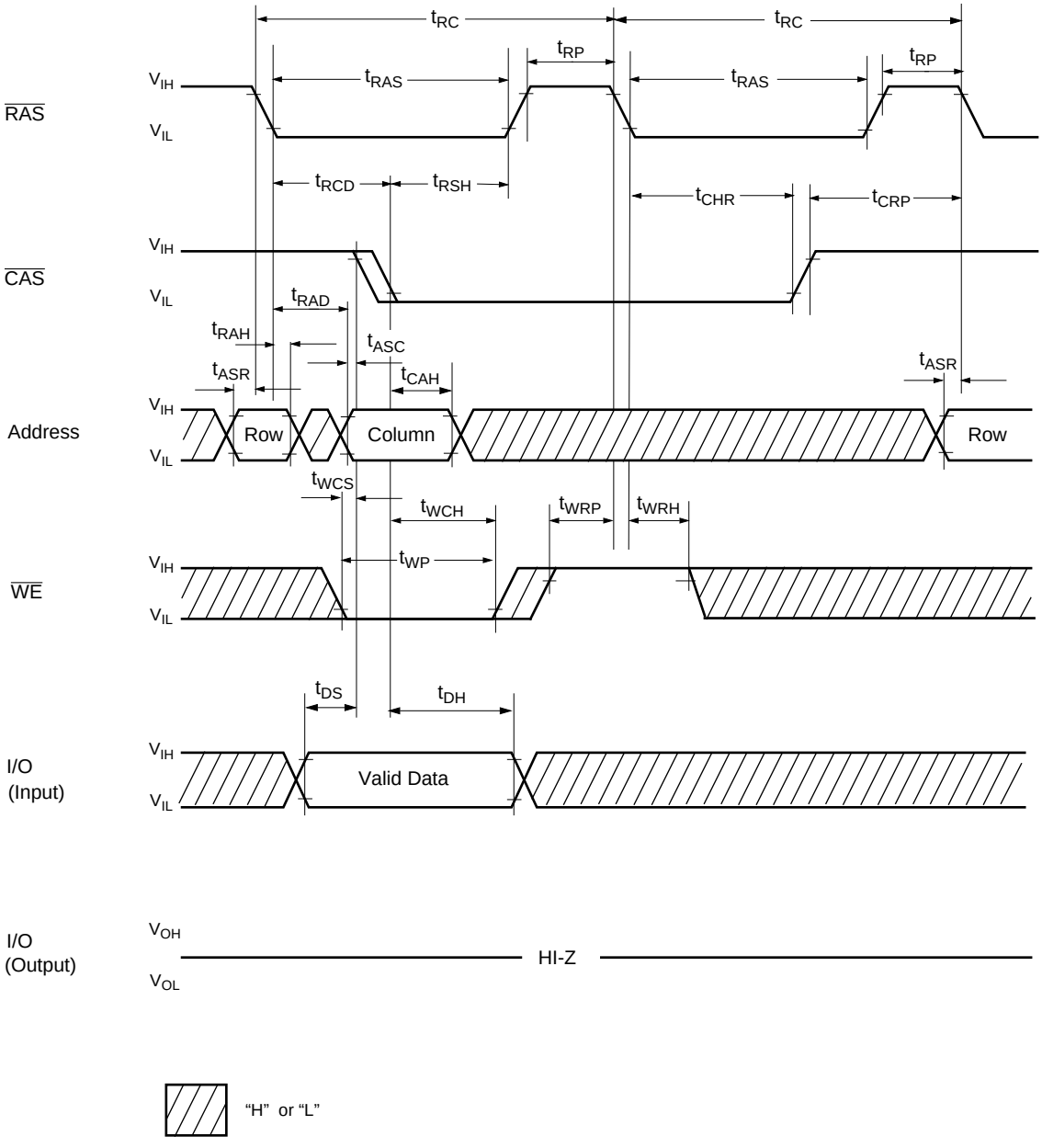


WL10

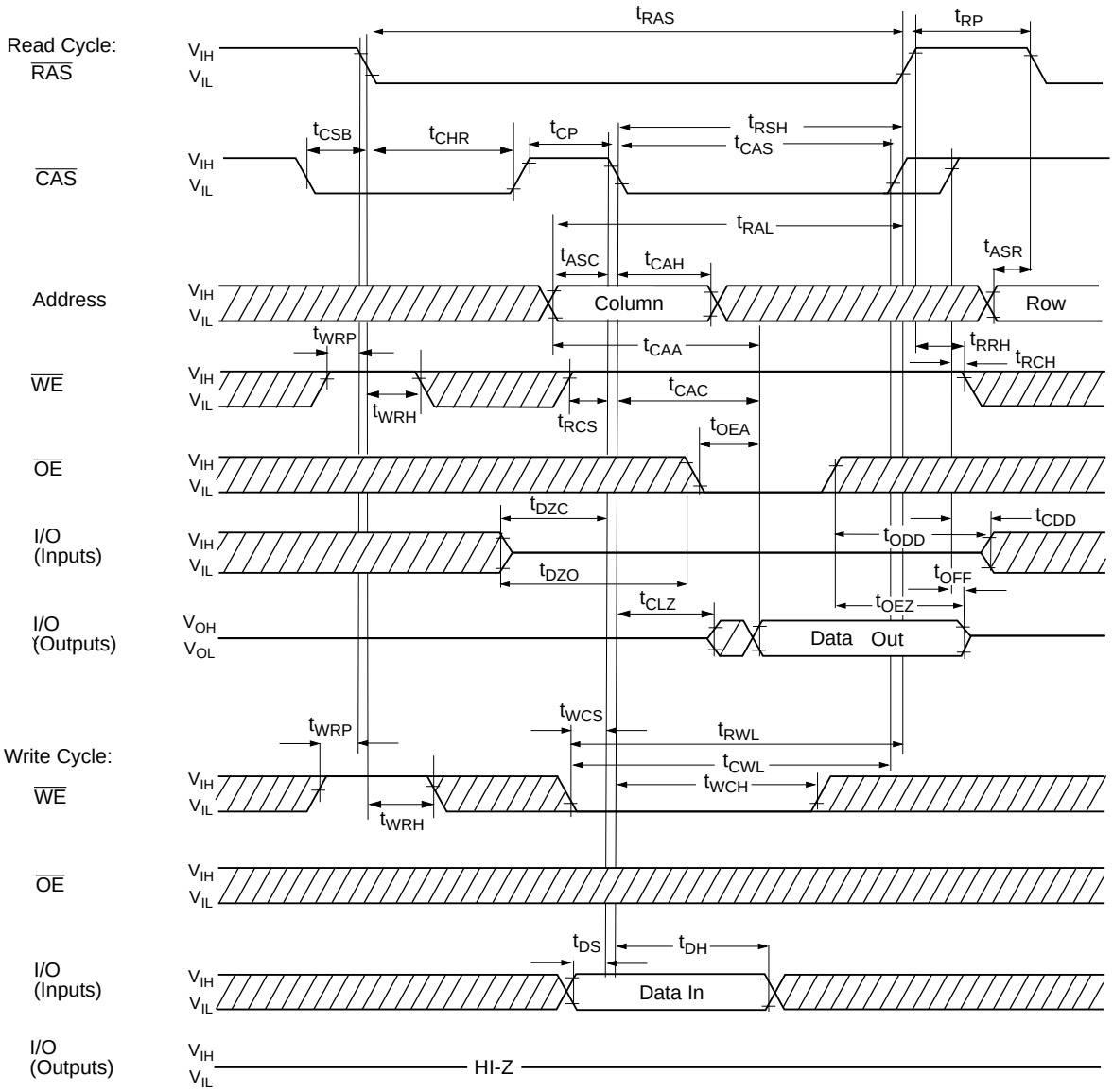
Waveforms of Hidden Refresh Read Cycle



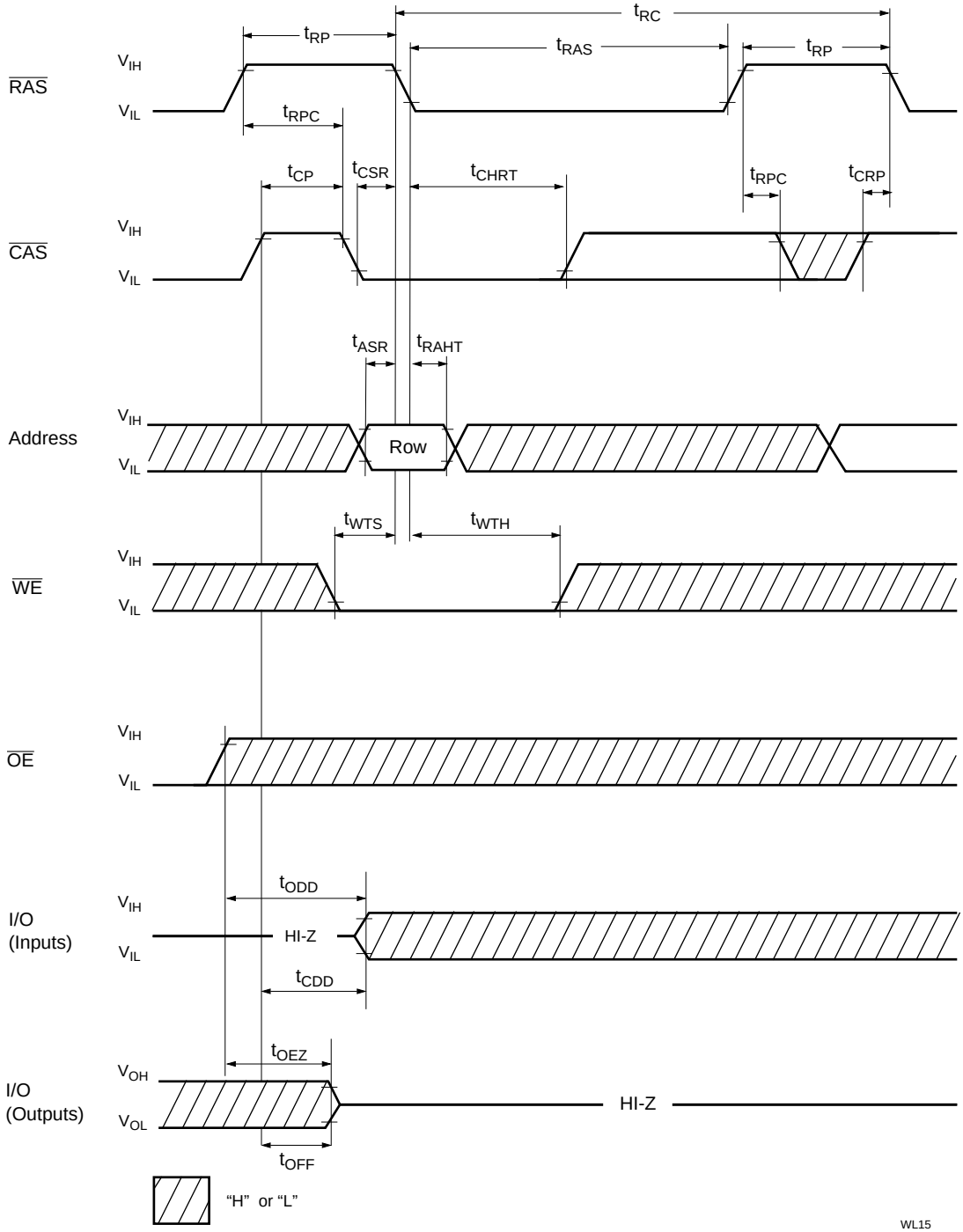
Waveforms of Hidden Refresh Early Write Cycle



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Waveforms of Test Mode Entry



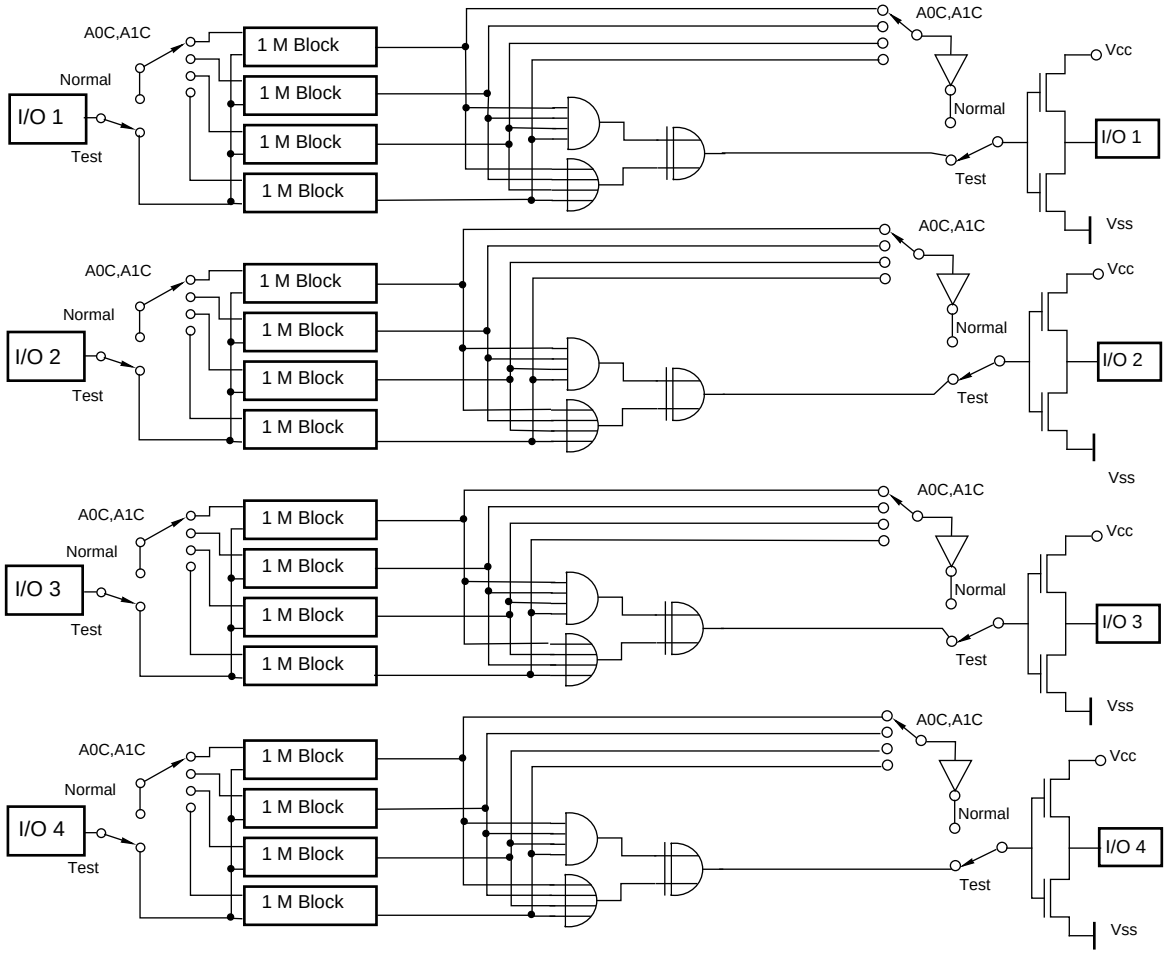
Test Mode

As the V53C516400A is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode “write” the data from each I/O pin is written into four 1M blocks simultaneously (all “1” s or all “0” s). In test mode “read” each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a “1”. If they were not equal, the I/O would indicate a “0”. The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a “$\overline{CAS}$ before $\overline{RAS}$ refresh”, “$\overline{RAS}$ only refresh” or “Hidden refresh” can be used.Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

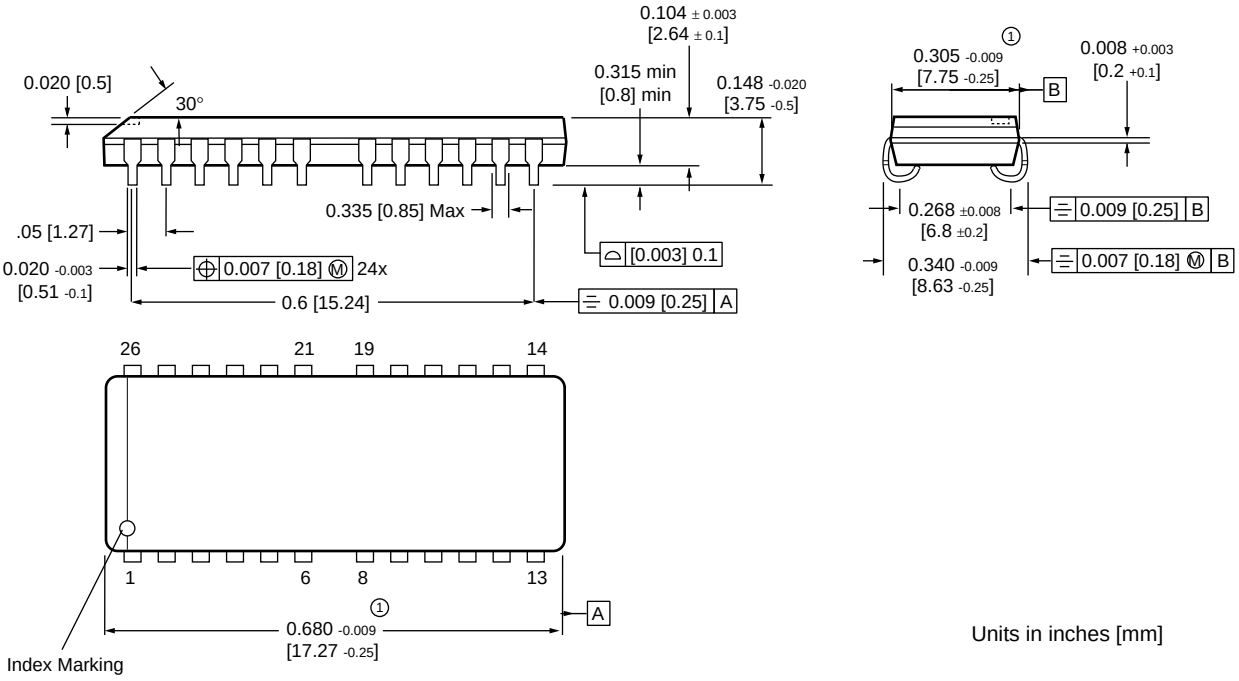
Row addresses A0 through A9 have to kept high to perform a testmode entry cycle. All other addresses are don’t care.

Block Diagram in Test Mode



Package Diagrams

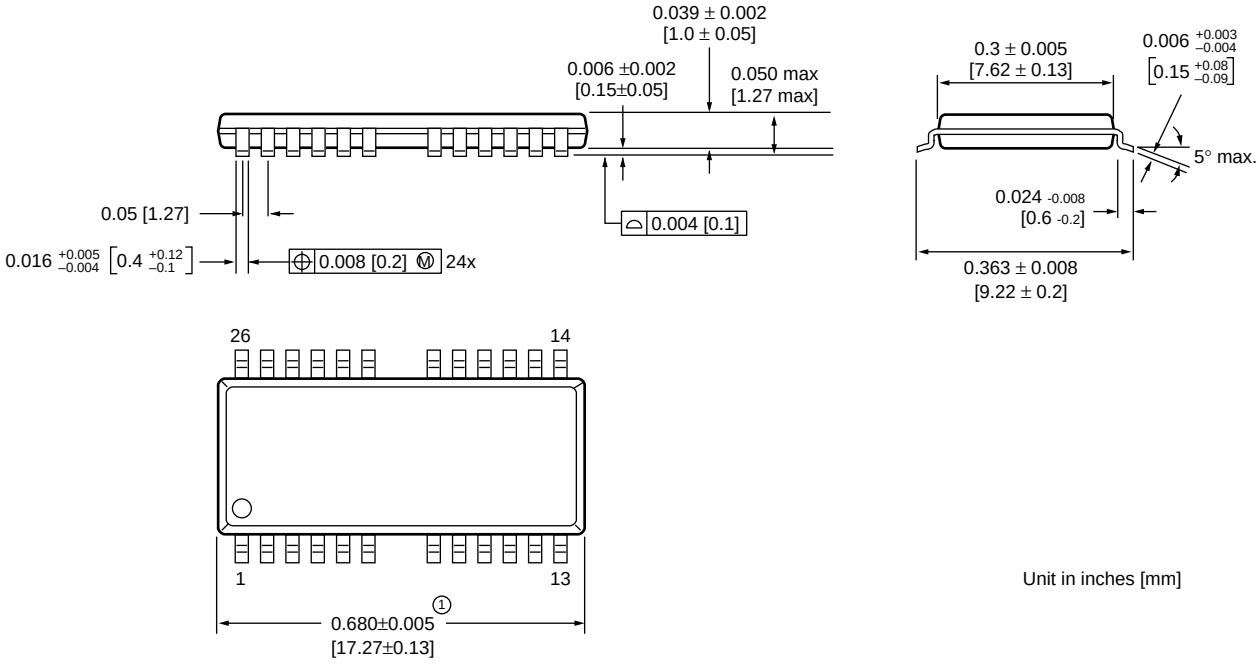
24/26-pin 300 mil SOJ



Units in inches [mm]

① Does not include plastic or metal protrusion of 0.15 max. per side

24/26-pin 300 mil TSOP-II



Unit in inches [mm]

① Does not include plastic or metal protrusion of 0.15 max. per side

U.S.A.
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

HONG KONG
19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 852-2665-4883
FAX: 852-2664-7535

TAIWAN
7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

1 CREATION ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-578-3344
FAX: 886-3-579-2838

JAPAN
WBG MARINE WEST 25F
6, NAKASE 2-CHOME
MIHAMA-KU, CHIBA-SHI
CHIBA 261-71
PHONE: 81-43-299-6000
FAX: 81-43-299-6555

IRELAND & UK
BLOCK A UNIT 2
BROOMFIELD BUSINESS PARK
MALAHIDE
CO. DUBLIN, IRELAND
PHONE: +353 1 8038020
FAX: +353 1 8038049

GERMANY (CONTINENTAL EUROPE & ISRAEL)
71083 HERRENBERG
BENZSTR. 32
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES

NORTHWESTERN
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

NORTHEASTERN
SUITE 436
20 TRAFALGAR SQUARE
NASHUA, NH 03063
PHONE: 603-889-4393
FAX: 603-889-9347

SOUTHWESTERN
SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 562-498-3314
FAX: 562-597-2174

CENTRAL & SOUTHEASTERN
604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 972-690-1402
FAX: 972-690-0341

© Copyright 1998, MOSEL VITELIC Inc.

3/98
Printed in U.S.A.

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.