UM10444

90 W notebook adapter with TEA1753, TEA1703 and TEA1791

Rev. 1 — 4 April 2011 **User manual**

Document information

Info	Content
Keywords	GreenChip III, TEA1753, GreenChip control IC, TEA1703, GreenChip SR, TEA1791, PFC, flyback, synchronous rectification, high efficiency, Power-down functionality for very low standby power, adapter, notebook, PC power
Abstract	This manual provides the specification, performance, schematics, bill of materials and PCB layout of a 90 W notebook adapter using the TEA1753, TEA1703 and TEA1791. Please refer to the relevant application notes for design details on the TEA1753, TEA1703 and TEA1791.

Revision history

Rev	Date	Description
v.1	20110404	first draft

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

1. Introduction

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This manual describes a universal input, 19.5 V, 4.62 A single output power supply using TEA1753 with the TEA1703 and TEA1791 devices from the GreenChip III and GreenChip SR family of NXP Semiconductors. It contains the specification of the power supply, circuit diagram, the component list to build the supply, the PCB layout and component positions, documentation of the PFC choke and transformer, along with test data and oscilloscope pictures of the most important waveforms.

The GreenChip III combines the control and drive for both the PFC and the flyback stages into a single device. The TEA1753 provides complete SMPS control functionality to comply with the IEC61000-3-2 harmonic current emission requirements, obtain a significant reduction of components, save PCB space and give a cost benefit. It also offers extremely low power consumption in no-load mode, which makes it suitable for the low-power consumer markets. The built-in green functions ensure high efficiency at all power levels, which results in a design that can easily meet all existing and proposed energy efficiency standards such as: CoC (Europe), ENERGY STAR (US), CEC (California), MEPS (Australian and New Zealand), and CECP (China).

The TEA1703 in combination with the TEA1753 provide a very low power requirement in Standby mode.

The GreenChip SR is a synchronous rectification control IC that needs no external components to tune the timing. Used in notebook adapter designs, the GreenChip SR offers a wide VCC operating range between 8.5 V and 38 V, minimizing the number of external components required and enabling simpler designs. In addition, the high driver output voltage (10 V) makes the GreenChip SR compatible with all brands of MOSFETs.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



019aab482

Fig 1. 90 W TEA1753 and TEA1791 demo board

2. Specification

- Mains input voltage: 90 V to 264 V; 47 Hz to 63 Hz
- DC output: 19.5 V; ±2 %
- Maximum continuous output current: 4.62 A
- Peak output current: ≥ 5.7 A
- Efficiency: > 88.5 % at maximum load
- ENERGY STAR active mode efficiency: > 89.5 %
- No load power consumption: ≤ 33 mW
- Dynamic load response (peak-to-peak): 700 mV
- Output ripple and noise (peak-to-peak): 100 mV
- CISPR22 class B conducted EMI (−15 dB margin)
- EN61000-4-2 immunity against ESD (≥ ±12 kV air discharge)
- EN61000-3-2 A14 (harmonics) compliance
- Short Circuit Protection (SCP); input power < 1.2 W during SCP test
- OverCurrent Protection (OCP); input power < 2.2 W during OCP test
- Latched output OverVoltage Protection (OVP): < 24 V
- Latched OverTemperature Protection (OTP); ≤ 120 °C
- Fast Latch Reset (FLR): < 2 s

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

3. Performance data

3.1 Test setup

3.1.1 Test equipment

- AC source: Agilent 6812B
- Power meter: Yokogawa WT210 with Harmonics option
- DC electronic load: Chroma, Model 63103
- Digital oscilloscope: Yokogawa DL1640L
- Current probe Yokogawa 701933 30 A; 50 MHz
- 100 MHz, high voltage differential probe: Yokogawa 700924
- 500 MHz, low voltage differential probe: Yokogawa 701920
- Multimeter: Keithley 2000
- EMC receiver: Rohde & Schwarz ESPI-3 + LISN ENV216

3.1.2 Test conditions

- Adapter on the lab-table with the heat sinks downwards
- The adapter has no casing
- Ambient temperature between 20 °C and 25 °C
- Measurements were made after stabilization of temperature according to "test method for calculating the efficiency of single-voltage external AC-DC and AC-AC power supplies" of ENERGY STAR

3.2 Efficiency

3.2.1 ENERGY STAR efficiency

To market adapters as ENERGY STAR efficient they have to pass the active mode and no-load criteria as stated in the ENERGY STAR standard for External Power Supplies; EPS2.0. The minimum active-mode efficiency is defined as the arithmetic average efficiency at 25 %, 50 %, 75 % and 100 % of the rated output power as printed on the nameplate of the adapter.

3.2.1.1 Active mode efficiency

Test Conditions:

The adapter is set to maximum load and well pre-heated until temperature stabilization is achieved. Temperature stabilization is established for every load step before recording any measurements.

Remark: The output voltage is measured at the end of the output cable (2×20 mΩ).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Criteria to pass:

To comply with ENERGY STAR EPS2.0, the arithmetic average of the four efficiency measurements must be greater than, or equal to, 87 %. Universal mains adapters have to pass the criteria at both 115 V; 60 Hz and 230 V; 50 Hz. To meet this criteria, the PFC must be off at 25 % load and preferably on at 50 % load.

Table 1. Active mode efficiency at 115 V; 60 Hz

Load (%)	I_O (A)	V_O (V)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
100	4.628	19.173	88.72	98.94	89.67	0.986
75	3.472	19.246	66.81	73.74	90.61	0.979
50	2.315	19.318	44.73	49.33	90.67	0.965
25	1.160	19.383	22.49	24.69	91.08	0.450
Average	-	-	-	-	90.51	-

Table 2. Active mode efficiency at 230 V; 50 Hz

Load (%)	I_O (A)	V_O (V)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
100	4.628	19.175	88.73	98.41	90.17	0.945
75	3.472	19.247	66.82	74.31	89.92	0.921
50	2.316	19.319	44.73	50.49	88.60	0.878
25	1.160	19.385	22.49	24.75	90.87	0.378
Average	-	-	-	-	89.89	-

Table 3. PFC on and off level as a function of the mains input voltage

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
Output current (A) (PFC on)	1.75	1.83	1.88	1.91	1.86
Output current (A) (PFC off)	1.35	1.36	1.34	1.35	1.31

3.2.1.2 No-load input power

Test Conditions:

The adapter is set to maximum load and pre-heated. After 5 minutes the load is removed. The no-load input power measurements were recorded after stabilization of the input power reading.

The combination of the TEA1733 with the TEA1703 results in a standby power consumption far below the requirements of ENERGY STAR EPS2.0. It reflects the standby power loss requirements of our customers.

Table 4. No-load input power

No-load input power as a function of the mains input voltage.

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
Input power P_I (mW)	10.0	10.8	12.5	32.1	39.5

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

3.2.1.3 Full load efficiency PFC plus flyback stage

Test conditions:

Before any measurements were recorded, the adapter is set to maximum load and is preheated till the readings were stabilized.

Remark: The output voltage is measured at the end of the output cable. (2×20 mΩ)

Criteria to pass:

The efficiency (η) must be > 88 % at the maximum continuous output load.

Table 5. PFC plus flyback stage

Total converter efficiency (at full load) as a function of the mains input

Mains supply	I_I RMS (A)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
90 V/60 Hz	1.130	88.74	100.24	88.53	0.989
100 V/50 Hz	1.013	88.76	99.58	89.14	0.987
115 V/60 Hz	0.877	88.72	98.94	89.67	0.986
230 V/50 Hz	0.456	88.73	98.41	90.17	0.945
264 V/50Hz	0.402	88.66	98.26	90.24	0.929

3.3 Timing and protection

3.3.1 Switch-on delay and output rise time

Test conditions:

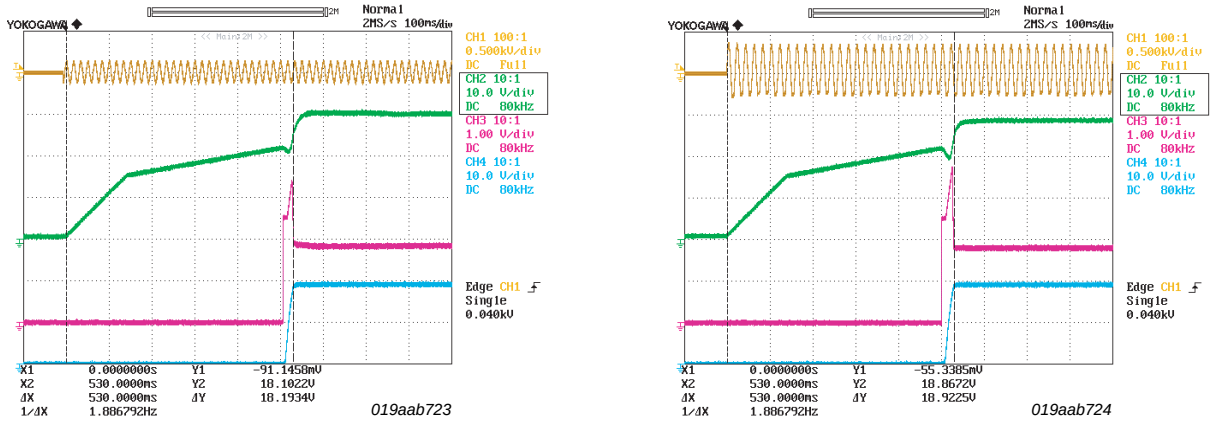
The electronic load is set to Constant Current (CC) mode and V_{on} = 0 V. The electronic load is set to the maximum continuous output current.

Criteria to pass:

- Switch-on delay: two seconds maximum after the AC mains voltage is applied to the time when the output is within regulation
- Output rise time: The output voltage must rise from 10 % of the maximum to the regulation limit within 30 ms. There must be a smooth and continuous ramp-up of the output voltage. No voltage with a negative polarity must be present at the output during start-up
- No output bounce or hiccup is allowed during switch-on.
- There be must be sufficient margin between the FBCTRL signal and the 4.5 V time-out trigger level to avoid false triggering of the time-out protection due to component tolerances

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

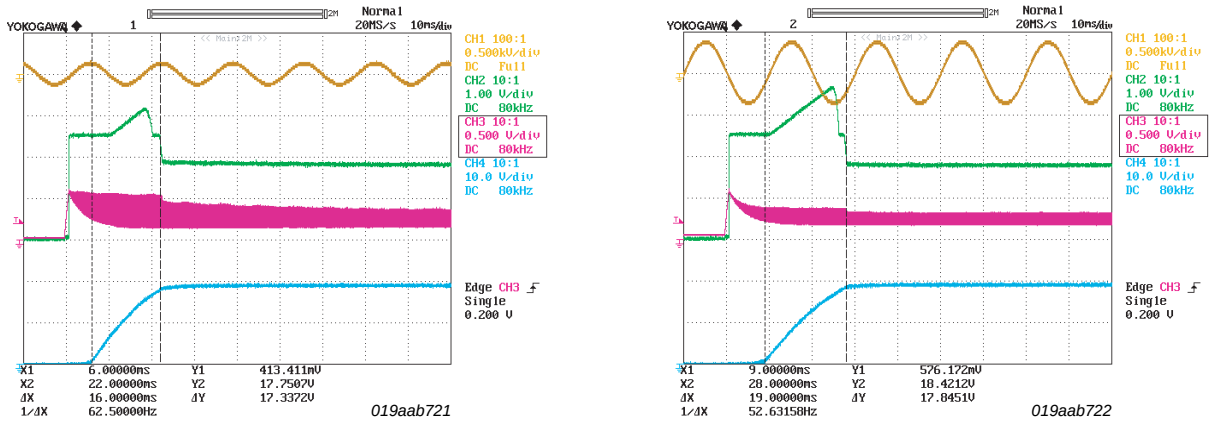


a. Mains input 90 V; 60 Hz; delay time 484 ms

b. Mains input 264 V; 50 Hz; delay time 484 ms

Load = 4.62 A; CH1 (brown): mains input; CH2 (green): VCC pin TEA1753; CH3 (magenta): FBCTRL pin TEA1753; CH4 (cyan): output voltage

Fig 2. Delay between switch-on and output in regulation



a. Mains input 90 V; 60 Hz; output rise time 12.64 ms

Load = 4.63 A

CH1 (brown): mains input

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): FBSENSE pin TEA1753 (soft-start)

CH4 (cyan): output voltage

b. Mains input 264 V; 50 Hz; output rise time 12.24 ms

Load = 4.63 A

CH1 (brown): mains input

CH2 (green): VCC pin TEA1751

CH3 (magenta): FBSENSE pin TEA1751 (soft-start)

CH4 (cyan): output voltage

Fig 3. Output rise time at full load start-up

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

3.3.2 Brownout and brownout recovery

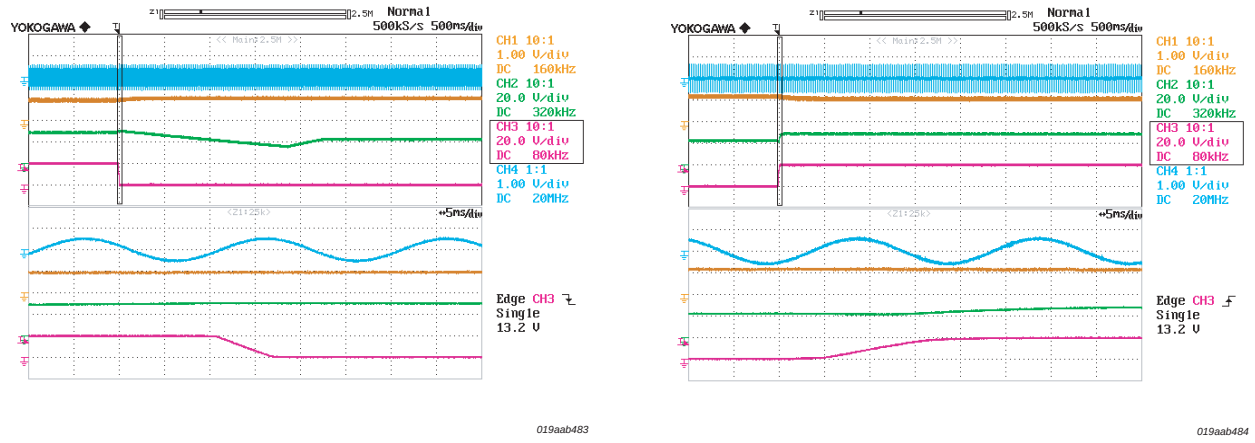
The voltage on the VINSENSE pin is monitored continuously to prevent the PFC from operating at very low mains input voltages.

Test Conditions:

The mains input voltage is decreased from 90 V down to 0 V and then increased from 0 V to 90 V. The electronic load is set to Constant Current (CC) mode and V_{on} = 0 V. The electronic load is set to the maximum continuous output current.

Criteria to pass:

- The adapter must survive the test without damage and excessive heating of component
- The output voltage must remain within the specified regulation limits or switch-off
- No output bounce or hiccup is allowed during switch-on or switch-off
- The adapter must power-up before the AC line input voltage reaches 85 V (maximum)



a. AC mains input from 90 V to 0 V

Brownout voltage = $105/(\sqrt{2}) = 74$ V

Load = 4.62 A

CH1 (brown): VINSENSE pin TEA1753

CH2 (green): VCC pin TEA1753

CH3 (magenta): output voltage

CH4 (cyan): mains input 200 V per division

b. AC mains input from 0 V to 90 V

Brownout recovery voltage = $121/(\sqrt{2}) = 83$ V)

Load = 4.62 A

CH1 (brown): VINSENSE pin TEA1753

CH2 (green): VCC pin TEA1753

CH3 (magenta): output voltage

CH4 (cyan): mains input 200 V per division

Fig 4. Brownout and brownout recovery

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

3.3.3 Output short circuit protection

To protect the adapter and application against an output short circuit or a single fault open (flyback) feedback loop situations, time-out protection is implemented. When the voltage on FBCTRL pin rises above 4.5 V (typical), a fault is assumed and switching is blocked.

The time-out protection must not trigger during a normal start-up with the maximum continuous output current.

Test Conditions:

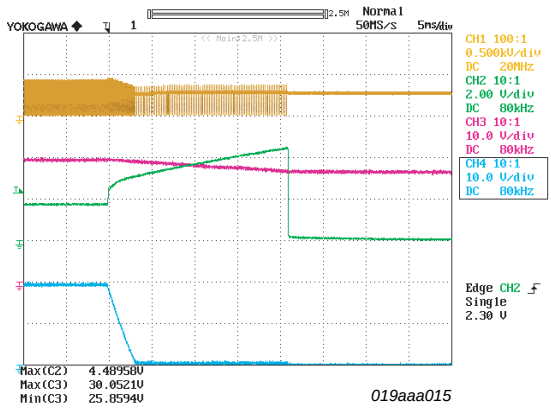
There are two test conditions:

1. The adapter is switched on with 4.62 A output load. After startup a short circuit is applied manually at the end of the output cable
2. Before the adapter is switched on a short circuit is applied to at the end of the output cable

Remark: An output short-circuit is defined as an output impedance of less than 0.1 ohm.

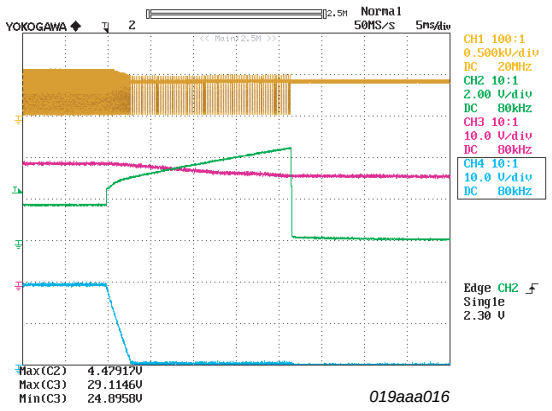
Criteria to pass:

- The adapter must be capable of withstanding a continuous short-circuit at the output without damaging or overstressing the adapter under any input conditions
- The average input power must be less than 3 W during the short-circuit test
- After removal of the short circuit, the adapter must recover automatically



a. Mains input 90 V; 60 Hz

Load before short circuit = 4.62 A
CH1 (brown): drain flyback MOSFET
CH2 (green): FBCTRL pin TEA1753
CH3 (magenta): VCC pin TEA1753
CH4 (cyan): output voltage



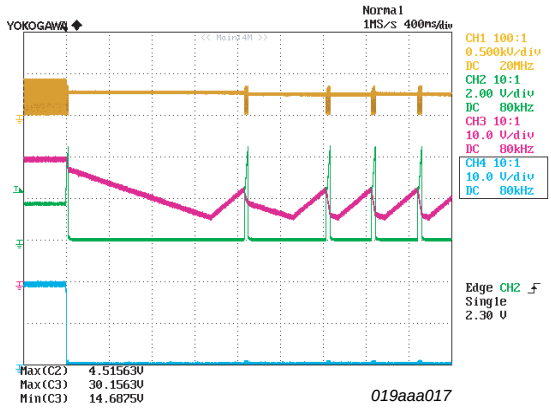
b. Mains input 264 V; 50 Hz

Load before short circuit = 4.62 A
CH1 (brown): drain flyback MOSFET
CH2 (green): FBCTRL pin TEA1753
CH3 (magenta): FBDRIVER pin TEA1753
CH4 (cyan): output voltage

Fig 5. Output short-circuit, triggering of the time-out protection

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



a. Output short-circuit during normal operation

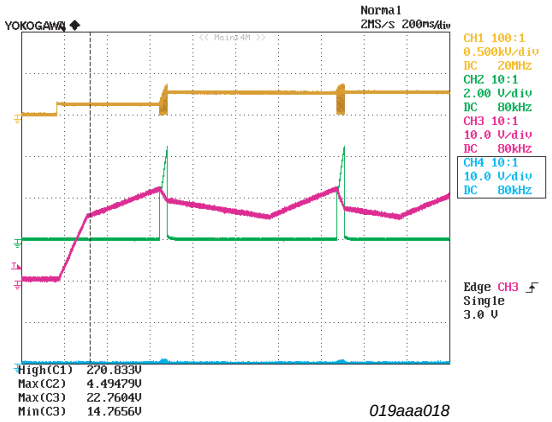
Load before short circuit= 4.62 A

CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): VCC pin TEA1753

CH4 (cyan): output voltage



b. Output short-circuit applied before start-up

Load = short circuit

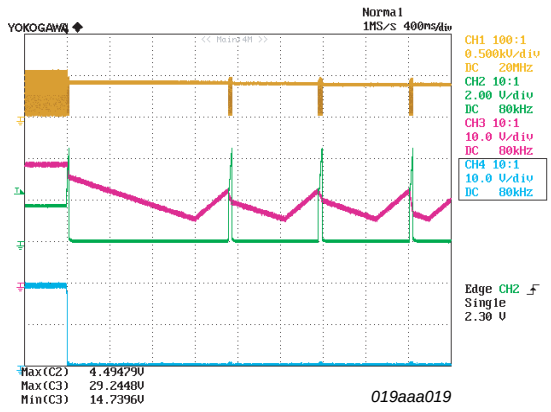
CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): VCC pin TEA1753

CH4 (cyan): output voltage

Fig 6. Output short-circuit at 90 V; 60 Hz



a. Output short-circuit during normal operation

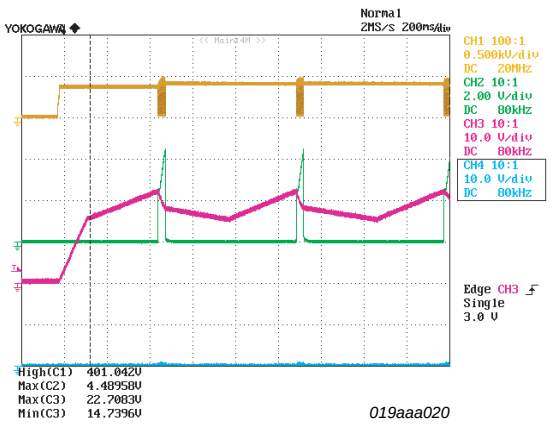
Load before short circuit = 4.62 A

CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): VCC pin TEA1753

CH4 (cyan): output voltage



b. Output short-circuit applied before start-up

Load = short circuit

CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta: VCC pin TEA1753

CH4 (cyan): output voltage

Fig 7. Output short-circuit at 264 V; 50 Hz

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 6. Output short circuit input power

Output short circuit input power as a function of the mains input voltage

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
Input power P_I (mW)	0.63	0.61	0.63	0.86	0.65

3.3.4 Output OverCurrent Protection (OCP)

Test Conditions:

- The electronic load is set in Constant Current (CC) mode
- The load is increased from the maximum continuous value in small steps until the overcurrent protection is triggered. The input power is measured after triggering the overcurrent protection without changing the load setting

Criteria to pass:

- The output power must be limited to less than 150 W, just before the triggering of the overcurrent protection
- The average input power must be less than 3 W once the overcurrent protection has been triggered

Table 7. Output overcurrent protection and input power as a function of the mains input voltage.

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
OCP trigger level (A)	6.16	6.16	6.15	5.78	5.77
Input power P_I (W)	135.2	134	132.2	122.5	122.5

3.3.5 Output OverVoltage Protection (OVP)

Test Conditions:

- The adapter is switched on without a load at the output
- An output over-voltage is created by applying a short circuit across the OPTO-LED of U2-1 (see Figure 14).

Criteria to pass:

- The output voltage must not exceed 25 V or stabilize between 25 V and the rated output voltage
- The voltage on the TEA1753 VCC pin must not exceed the absolute maximum rating of 38 V
- When OVP is triggered, the primary side controller must shut down and stay in a latched mode
- A single point fault must not cause a sustained overvoltage condition at the output

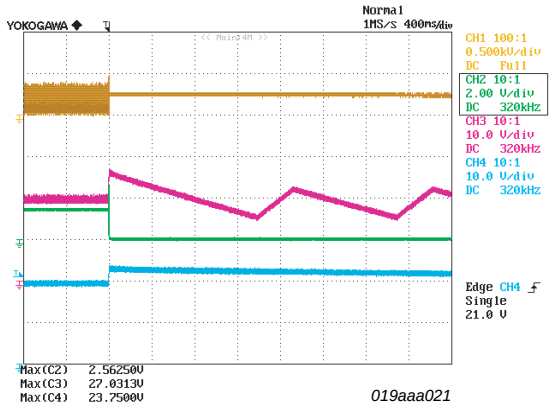
Table 8. Output over-voltage protection

Output over-voltage at no-load as a function of the mains input voltage with protection mode latched

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
Output OVP trip point (V)	23.8	23.8	23.7	23.8	23.7
VCC maximum during OVP (V)	27.5	27.5	27.5	27.1	27.0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



a. Mains input 90 V; 60 Hz

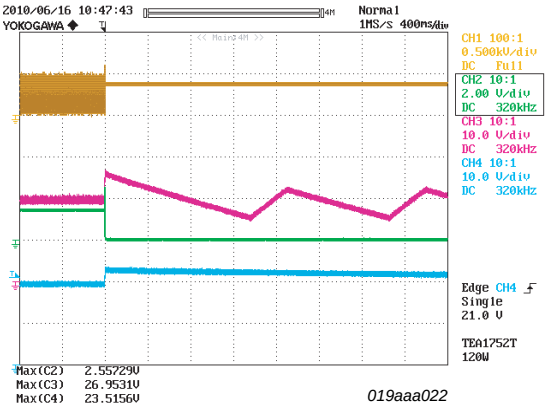
Output current before short-circuit of the optocoupler = 0.015 A

CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): VCC pin TEA1753

CH4 (cyan): output voltage



b. Mains input 264 V; 50 Hz

Output current before short-circuit of the optocoupler = 0.015 A

CH1 (brown): drain flyback MOSFET

CH2 (green): FBCTRL pin TEA1753

CH3 (magenta): VCC pin TEA1753

CH4 (cyan): output voltage

Fig 8. Output overvoltage protection

3.3.6 OverTemperature Protection (OTP)

An accurate external over temperature protection (TEA1753's LATCH pin, RT2, R26 and C19) is provided on the demo board to protect the flyback transformer against overheating (see Figure 14). Normally, the flyback transformer is the most heat sensitive component.

Test Conditions:

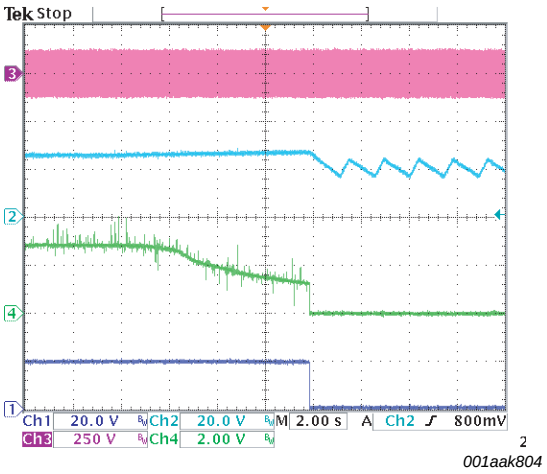
The NTC temperature sensor, glued to the transformer, is heated using a heat gun.

Criteria to pass:

The IC must latch off the output at a VLATCH trip level of 1.25 V. No output bounce or hiccup is allowed

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



OTP trigger temperature 108 °C

Output current 4.62 A before OTP is triggered

CH1 (blue): V_{out}

CH2 (cyan): TEA1753 VCC pin

CH3 (magenta): Mains input voltage

CH4 (green): TEA1753 LATCH pin

Fig 9. External OverTemperature Protection (OTP)

3.3.7 Fast latch reset

A Fast Latch Reset function (FLR) enables latched protection to be reset without discharging the bulk elcap. The latch protection is reset as soon as the voltage on VINSENSE pin drops below 0.75 V and is then raised to 0.87 V.

Test conditions:

- The output is loaded (I_{out} = 50 mA)
- The test sequence is as follows:
  - The latch protection is triggered by an OVP caused by a short-circuit across the OPTO-led
  - The mains input is switched off and the voltage on pin VINSENSE dropped below 0.75 V
  - The mains input is switched on and, as soon as the voltage on pin VINSENSE rises above 0.87 V, the latch is reset

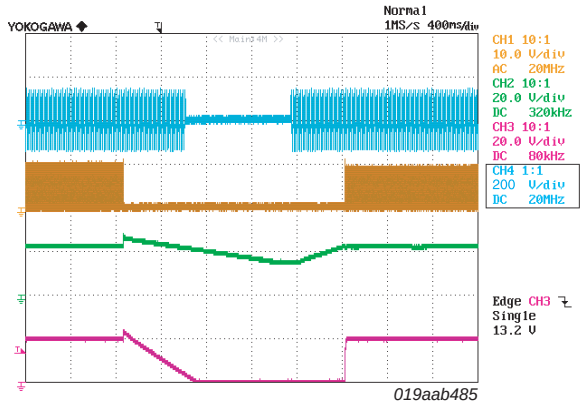
Remark: Both live and neutral must be switched.

Criteria to pass:

The latch must be reset within 3 seconds after switching off and switching on, the mains input voltage.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



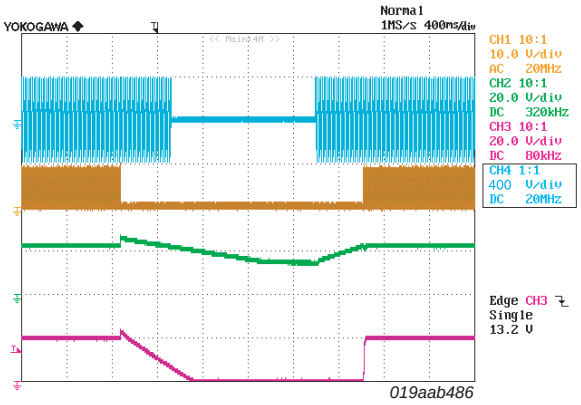
a. Mains input 90 V; 60 Hz; FLR = 1.2 s

CH1 (brown): FBDRIVER

CH2 (green): VCC pin TEA1753

CH3 (magenta): output voltage 20 V per division (I_O = 50 mA)

CH4 (cyan): AC mains input voltage 200 V per division



b. Mains input 264 V; 50 Hz; FLR = 1.3 s

CH1 (brown): FBDRIVER

CH2 (green): VCC pin TEA1753

CH3 (magenta): output voltage 20 V per division (I_O = 50 mA)

CH4 (cyan): AC mains input voltage 400 V per division

Fig 10. Fast Latch Reset (FLR)

3.4 Output regulation and characterization

3.4.1 Load regulation

Test conditions:

- The output voltage deviation is measured while the load current on the output is increased from 15 mA to 4.62 A
- The measurement is repeated for different mains input voltages

Remark: The output voltage is measured at the end of the output cable, the minimum current of 15 mA prevents switching to Standby mode.

Criteria to pass:

The output load regulation must remain within 2 %.

The load regulation is calculated using Equation 1.

$$\frac{V_{O(max)} - V_{O(min)}}{V_{O(nom)}} \times 100\ \% \quad (1)$$

where $V_{O(nom)}$ = 19.5 V.

Table 9. Load regulation

Output voltage as a function of the output load and the mains input voltage

Mains supply	90 V/60 Hz		264 V/50 Hz	
V_O (V)	19.558	19.325	19.559	19.324
I_O (A)	0.015	4.62	0.015	4.62

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Load regulation at 90 V; 60 Hz is calculated as follows:

$$\frac{19.558V - 19.325V}{19.5V} \times 100\ \% = 1.19\ \% \quad (2)$$

Load regulation at 264 V; 50 Hz is calculated as follows:

$$\frac{19.559V - 19.324V}{19.5V} \times 100\ \% = 1.21\ \% \quad (3)$$

3.4.2 Line regulation

Test conditions:

- The output voltage deviation is measured while the mains voltage on the input is increased from 90 V to 264 V
- The measurement is repeated for different mains input voltages

Remark: The output voltage is measured at the end of the output cable. The load current is 4.62 A.

The line regulation is calculated using the following equation:

$$\frac{V_{O(max)} - V_{O(min)}}{V_{O(nom)}} \times 100\ \% \quad (4)$$

Criteria to pass:

The output voltage deviation must remain within 0.05 %.

Table 10. Line regulation

Output voltage (at full load) as a function of the mains input voltage

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
V_O (V)	19.325	19.325	19.325	19.324	19.324

Load regulation at 90 V; 60 Hz is calculated using the following equation:

$$\frac{19.325V - 19.324V}{19.5V} \times 100\ \% = 0.005\ \% \quad (5)$$

3.4.3 Ripple and noise PARD (Periodic And Random Deviation)

Ripple and noise are defined as the periodic or random signals over a frequency band of 10 Hz to 20 MHz.

Test Conditions:

- The measurement is made with an oscilloscope set to bandwidth of 20 MHz
- The output is shunted at the end of the output cable, by a 0.1 μF ceramic disk capacitor and a 22 μF electrolytic capacitor, to simulate loading

Criteria to pass:

The output ripple and noise must remain within the specified limits 100 mV (peak-to-peak) at a maximum load current of 4.62 A.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 11. Ripple and noise PARD

Ripple and noise (at maximum load) as a function of the mains input voltage.

Mains supply	90 V/60 Hz	100 V/50 Hz	115 V/60 Hz	230 V/50 Hz	264 V/50 Hz
PARD (mV)	94	94	94	83	83

3.4.4 Dynamic load response

Test Conditions:

- The adapter is subjected to a load change from 0.33 % to 100 % at a slew rate of 1 A / ms
- The frequency of change is set to give the best readability of the deviation and setting time

Remark: The voltage is measured at the end of the output cable, the minimum output current of 15 mA prevents switching in to Standby mode.

Criteria to pass:

The output is not allowed to have an overshoot or undershoot beyond the specified limits (+1 V to 0.5 V) after a load change.

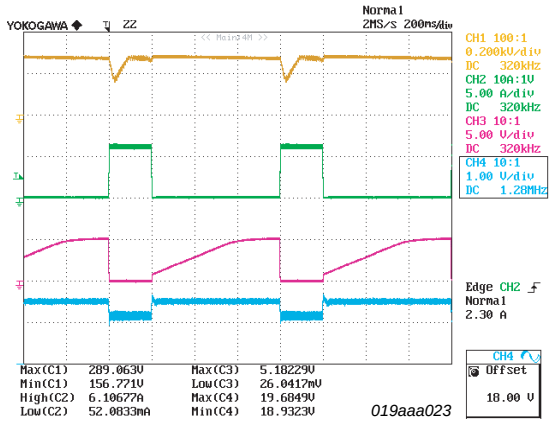
Table 12. Dynamic load response

Deviation of the output voltage at a load step from 4.62 A to 0.015 A and from 0.015 A to 4.62 A

Mains supply	90 V/60 Hz	230 V/50 Hz
Deviation (mV_{p-p})	700	700

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



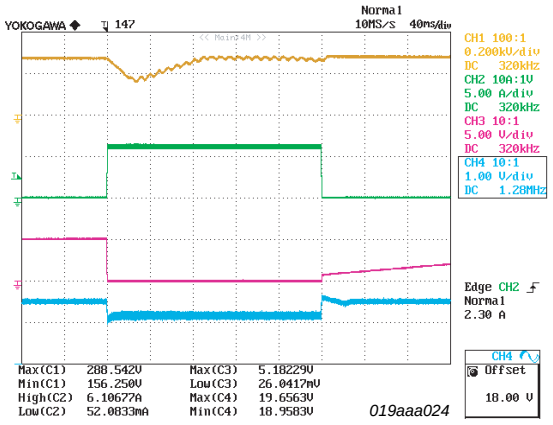
CH1 (brown): PFC bus voltage

CH2 (green): output current

Ch3 (magenta): PFCTIMER pin

Ch4 (cyan): output voltage

a. Mains input 90 V; 60 Hz



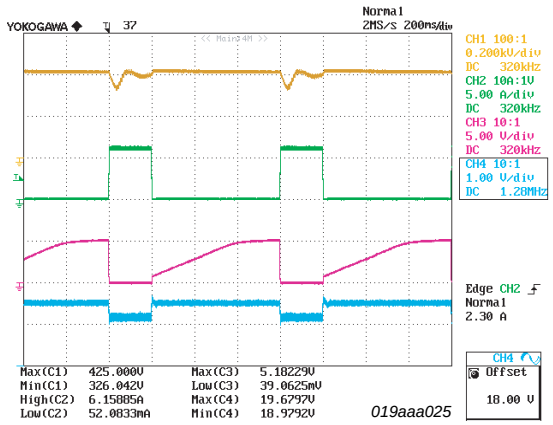
CH1 (brown): PFC bus voltage

CH2 (green): output current

Ch3 (magenta): PFCTIMER pin

Ch4 (cyan): output voltage

b. Mains input 90 V; 60 Hz (detail picture)



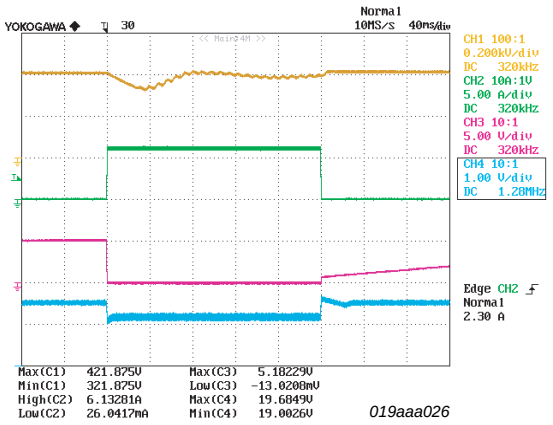
CH1 (brown): PFC bus voltage

CH2 (green): output current

Ch3 (magenta): PFCTIMER pin

Ch4 (cyan): output voltage

c. Mains input 230 V; 50 Hz



CH1 (brown): PFC bus voltage

CH2 (green): output current

Ch3 (magenta): PFCTIMER pin

Ch4 (cyan): output voltage

d. Mains input 230 V; 50 Hz (detail picture)

Fig 11. Dynamic load response

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

4. ElectroMagnetic Compatibility (EMC)

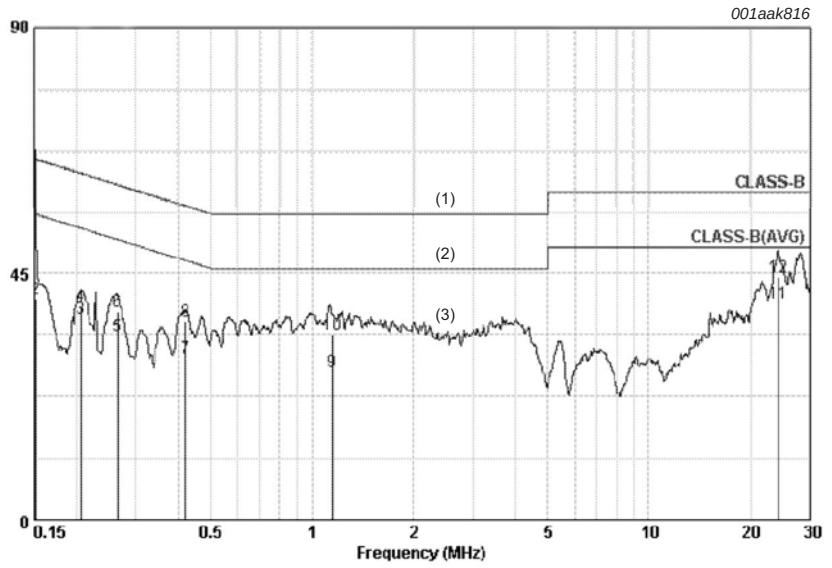
4.1 Conducted emission

Test Conditions:

- The adapter is subjected to maximum load
- The ground connection of the output cable is connected to EMC ground

Criteria to pass:

CISPR22 Class B with -10 dB production margin, unless otherwise stated.



(1) QP limit
(2) AV limit
(3) Peak reading

The conducted EMI measurement of 110 V neutral is close to 110 V line

Fig 12. Conducted EMI 110 V line

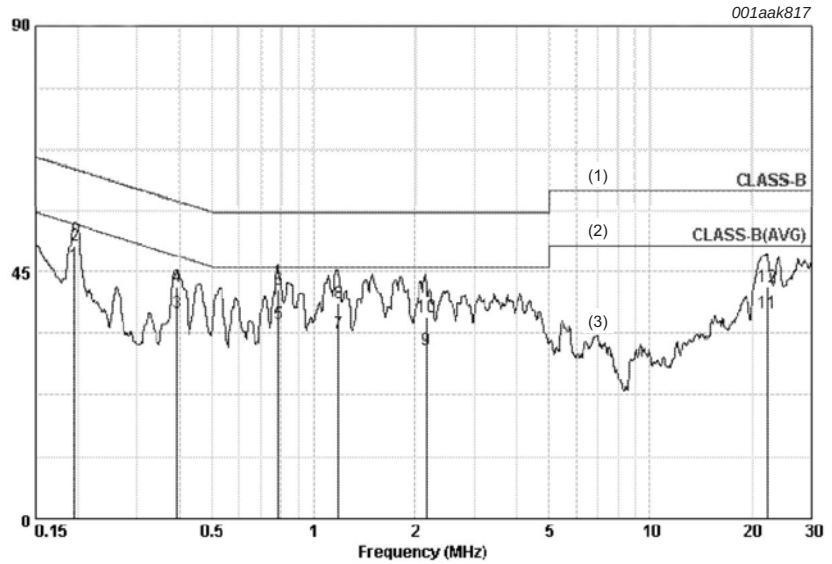
Table 13. Conducted EMI measurement 110 V line

Refer to Figure 12 points 1 and 2 on the peak reading graph

No.	Frequency (MHz)	Correction factor (dB)	Reading dBμV		Emission dBμV		Limit dBμV		Margins dB	
			QP	AV	QP	AV	QP	AV	QP	AV
11 and 12	24.250	0.095	44.342	39.485	44.437	39.580	60.000	50.000	−15.563	−10.420

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



(1) QP limit

(2) AV limit

(3) Peak reading

The conducted EMI measurement of 230 V neutral is close to 230 V line

Fig 13. Conducted EMI 230 V line

Table 14. Conducted EMI measurement 230 V line

Refer to Figure 13 points 1, 2 and 3 on the peak reading graph.

No.	Frequency (MHz)	Correction factor (dB)	Reading (dBμV)		Emission (dBμV)		Limit (dBμV)		Margins (dB)	
			QP	AV	QP	AV	QP	AV	QP	AV
1 and 2	0.195	0.071	49.746	46.337	49.817	46.408	63.808	53.808	−13.991	−7.400
3 and 4	0.393	0.055	42.393	37.662	42.448	37.717	58.004	48.004	−15.556	−10.287
5 and 6	0.784	0.031	41.712	35.555	41.734	35.586	56.00	46.00	−14.257	−10.414

4.2 Immunity against lighting surges

Test conditions:

- Combination wave: 1.2/50 μs open circuit voltage and 8/20 μs short circuit current
- Test voltage: 2 kV
- L1 to L2: 2 Ω; L1 to PE, L2 to PE and L1 + L2 to PE: 12 Ω
- Phase angle: 0°, 90°, 180° and 270°
- Number of tests: 5 positive and 5 negative
- Pulse repetition rate: 20 s

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Test result:

- There is no disruption of functionality

4.3 Immunity against ESD

Test conditions:

- ESD air discharge at the ground contact of the output cable

Criteria to pass:

- IEC61000-4-2 air discharge level 3 (8 kV) and level 4 (15 kV)

Table 15. Immunity against ESD

Performance of the adapter at an ESD air discharge

ESD performance	No disruption of function	Auto recovery
Demo board according to schematic	±12 kV	±15 kV
Demo board with 6 M x 10 M across Y-cap	±16.5 kV	-

4.4 Mains harmonic reduction

Test conditions:

- The adapter is set to the maximum continuous load of 4.62 A
- The input voltage is 230 V; 50 Hz

Criteria to pass:

- Compliance with EN61000-3-2 A14 class D

Test result:

- Passed, see Table 16

Table 16. MHR according EN61000-3-2 A14, class D

Harmonic no.	Measured (mA)	Limit (mA)	Harmonic no.	Measured (mA)	Limit (mA)
1	437.2	-	21	1.2	20.1
3	113.5	338.1	23	7.3	18.2
5	37.2	189.0	25	2.3	16.7
7	10.5	99.4	27	5.2	15.3
9	7.3	49.7	29	2.3	14.2
11	9.0	34.8	31	2.5	13.2
13	6.0	34.8	33	0.9	12.4
15	6.7	29.5	35	4.0	11.6
17	3.0	25.5	37	1.2	10.9
19	4.9	22.5	39	3.8	10.3

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

INTENTIONALLY LEFT BLANK

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

5. Schematic

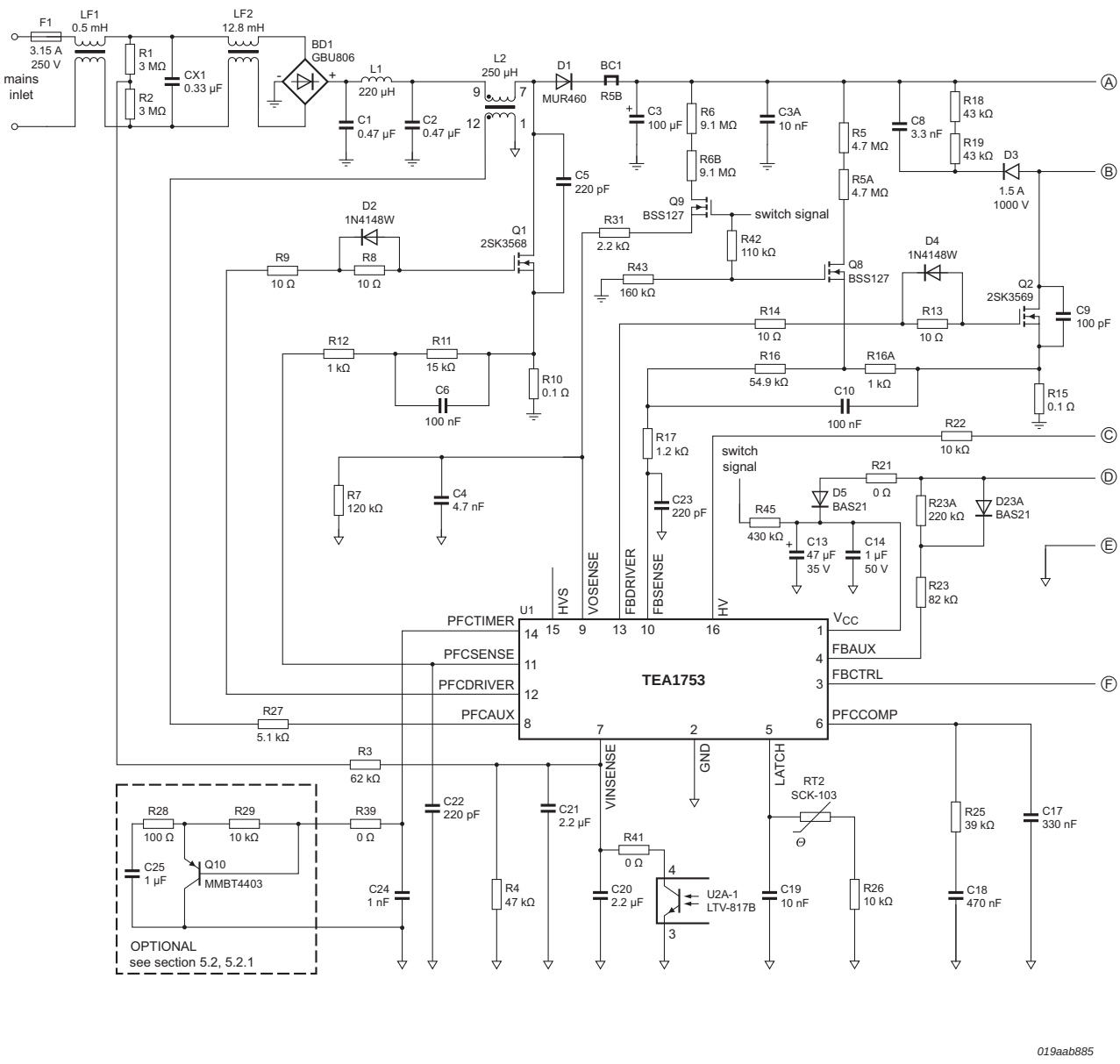


Fig 14. Schematic of 90 W TEA1753 and TEA1791 adapter solution (part 1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

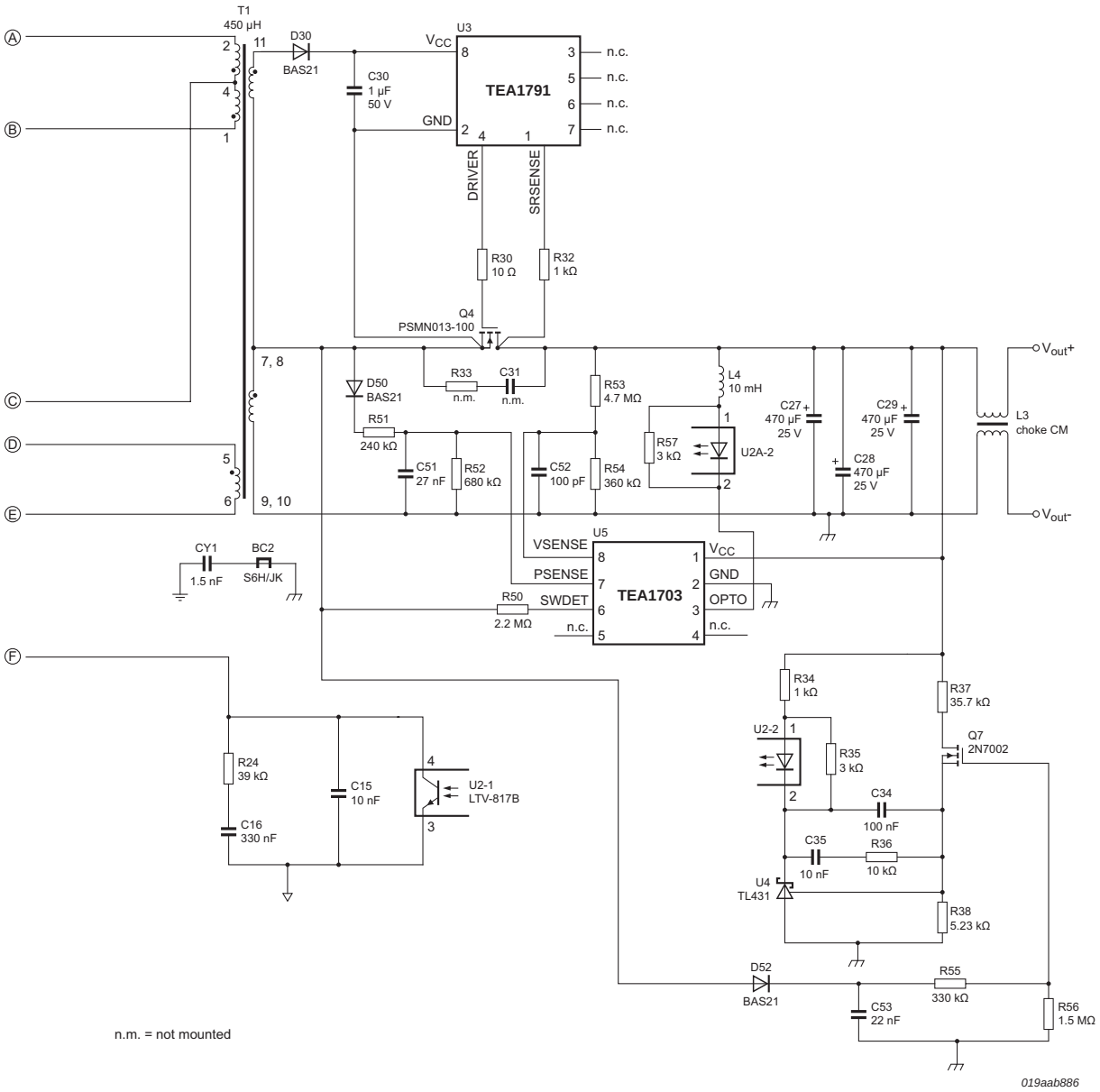


Fig 15. Schematic of 90 W TEA1753 and TEA1791 adapter solution (part 2)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

6. Bill of materials

Table 17. Default bill of materials for a 90 W TEA1753, TEA1703 and TEA1791 adapter solution

Reference	Component	Package	Remark
R1	3 MΩ, 1 %	1206	-
R2	3 MΩ, 1 %	1206	-
R3	62 kΩ, 1 %	1206	-
R4	47 kΩ, 1 %	0603	-
R5	4.7 MΩ, 1 %	1206	-
R5A	4.7 MΩ, 1 %	1206	-
R6	9.1 MΩ, 1 %	1206	-
R6B	9.1 MΩ, 1 %	1206	-
R7	120 kΩ, 1 %	0603	-
R8	10 Ω, 5 %	0805	-
R9	10 Ω, 5 %	0805	-
R10	0.1 Ω, 5 %	axial	metal-oxide film
R11	15 kΩ, 5 %	0603	-
R12	1 kΩ, 5 %	0805	-
R13	10 Ω, 5 %	0805	-
R14	10 Ω, 5 %	0805	-
R15	0.1 Ω, 1 %	axial	metal-oxide film
R16	54.9 kΩ, 1 %	0603	-
R16A	1 kΩ, 1 %	0603	-
R17	1.2 kΩ, 1 %	0603	-
R18	43 kΩ, 5 %	1206	-
R19	43 kΩ, 5 %	1206	-
R21	0 Ω	0603	-
R22	10 kΩ, 5 %	0805	-
R23	82 kΩ, 1 %	0603	-
R23A	220 kΩ, 1 %	0603	-
R24	39 kΩ, 5 %	0603	-
R25	39 kΩ, 5 %	0603	-
R26	10 kΩ, 5 %	0603	-
R27	5.1 kΩ, 5 %	1206	-
R28	100 Ω, 5 %	0603	-
R29	10 kΩ, 5 %	0603	-
R30	10 Ω, 5 %	0805	-
R31	2.2 kΩ, 1 %	0603	-
R32	1 kΩ, 5 %	0805	-
R33	not Mounted	-	-
R34	1 kΩ, 5 %	0603	-
R35	3 kΩ, 5 %	0603	-
R36	10 kΩ, 5 %	0603	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 17. Default bill of materials for a 90 W TEA1753, TEA1703 and TEA1791 adapter solution *...continued*

Reference	Component	Package	Remark
R37	35.7 kΩ, 1 %	0603	-
R38	5.23 kΩ, 1 %	0603	-
R39	0 Ω	0805	-
R41	0 Ω	0603	-
R42	110 kΩ, 5 %	0603	-
R43	160 kΩ, 5 %	0603	-
R45	430 kΩ, 5 %	0603	-
R50	2.2 MΩ, 5 %	0603	-
R51	240 kΩ, 5 %	0603	-
R52	680 kΩ, 5 %	0603	-
R53	4.7 MΩ, 5 %	0603	-
R54	360 kΩ, 5 %	0603	-
R55	330 kΩ, 5 %	0603	-
R56	1.5 MΩ, 5 %	0603	-
R57	3 kΩ, 5 %	0603	-
RT2	NTC 100 kΩ; D = 5 mm	radial lead	TTC050104
C1	film capacitor; 0.47 μF; 450 V, 10 %	-	-
C2	film capacitor; 0.47 μF; 450V, 10 %	-	-
C3	electrolytic capacitor; 100 μF; 400 V; 105 °C	radial 16 × 30 mm	-
C3A	10 nF; 1 kV; Z5U	disk 11.5 mm	-
C4	4.7 nF; 25 V; X7R	0603	-
C5	220 pF; 630 V; NP0	1206	-
C6	100 nF; 25 V; X7R	0603	-
C8	3.3 nF; 630 V	1206	-
C9	100 pF; 630 V; NP0	1206	-
C10	100 nF; 25 V; X7R	0805	-
C13	electrolytic capacitor 47 μF; 35 V; 105 °C	radial 5 × 11 mm	low-impedance type
C14	1 μF; 50 V; Y5V	0805	-
C15	10 nF; 25 V; X7R	0603	-
C16	330 nF; 10 V; X7R	0603	timing capacitor; review tolerance
C17	330 nF; 10 V; X7R	0603	-
C18	470 nF; 10 V; X7R	0603	-
C19	10 nF; 25 V; X7R	0603	-
C20	2.2 μF; 10 V; Y5V	0603	-
C21	2.2 μF; 10 V; Y5V	0603	-
C22	220 pF; 50 V; NP0	0603	10 V is permitted
C23	220 pF; 50 V; NP0	0603	10 V is permitted
C24	1 nF; 50 V; X7R	0603	10 V is permitted
C25	1 μF; 16 V; X7R	0603	10 V is permitted
C27	electrolytic capacitor; 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type
C28	electrolytic capacitor; 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 17. Default bill of materials for a 90 W TEA1753, TEA1703 and TEA1791 adapter solution *...continued*

Reference	Component	Package	Remark
C29	electrolytic capacitor; 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type
C30	1 μF; 50 V; Y5V	0805	-
C31	not mounted	-	-
C34	100 nF; 25 V; X7R	0603	-
C35	10 nF; 25 V; X7R	0603	-
C51	27 nF; 25 V; X7R	0603	-
C52	100 pF; 50 V; NP0	0603	-
C53	22 nF; 25 V; X7R	0603	-
CX1	0.33 μF; 275 V (AC); X2	MKP	-
CY1	1.5 nF; 400 V (AC); Y1	pitch 10 mm	-
BD1	GBU806; 8 A; 600 V	flat/mini	-
D1	MUR460; 4 A; 600 V	DO-201AD	Vishay
D2	1N4148W	SOD80	-
D3	S2M	SMB	-
D4	1N4148W	SOD80	-
D5	BAS21	SOT23	NXP Semiconductors
D23A	BAS21	SOT23	NXP Semiconductors
D30	BAS21	SOT23	NXP Semiconductors
D50	BAS21	SOT23	NXP Semiconductors
D52	BAS21	SOT23	NXP Semiconductors
Q1	2SK3568	TO220F	-
Q2	2SK3569	TO220F	-
Q4	PSMN013-100	TO220F	NXP Semiconductors
Q7	2N7002	SOT23	-
Q8	BSS127	SOT23	-
Q9	BSS127	SOT23	-
Q10	MMBT4403	SOT23	-
U1	TEA1753	SO16	NXP Semiconductors, GreenChip III PFC and flyback controller
U2	LTV817B	DIP4-W	CTR 130-260, spacing 10.16 mm
U2A	LTV817B	DIP4-W	CTR 130-260, spacing 10.16 mm
U3	TEA1791	SMD, SO8	NXP Semiconductors, GreenChip SR controller
U4	D431	SOT23R	Double Microelectronics
U5	TEA1703	SMD, SO8	NXP Semiconductors, GreenChip SMPS standby control IC
T1	flyback transformer 450 μH	PQ3220	see specification in Section 7.1
L1	inductor 220 μH	T50-52	-
L2	PFC inductor 250 μH	RM10	see specification in Section 7.2
L3	inductor CM 200 μH	T12*6*4	-
L4	inductor 10 mH	axial	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 17. Default bill of materials for a 90 W TEA1753, TEA1703 and TEA1791 adapter solution *...continued*

Reference	Component	Package	Remark
LF1	inductor CM 500 μH	T12*6*4	-
LF2	inductor CM 12.8 MH	T16*12*18	
BC1	bead core R5B/XP N4/AMAX	RH 4*6*2	placed at cathode of D1
BC2	bead core S6H/JK N6/AMAX	RH 3.5*4.2*1.3	placed at lead of CY1
F1	fuse T 3.15 A; 250 V	LT5	-

7. Transformer and inductor specifications

7.1 Flyback transformer T1 specifications

- Primary inductance: 450 μH (±5 %)
- Leakage inductance: 6 μH (max)
- Core/bobbin: PQ3220
- Core material: PC44
- HI-POT primary - secondary: 3 kV; 5 mA; 3 s

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

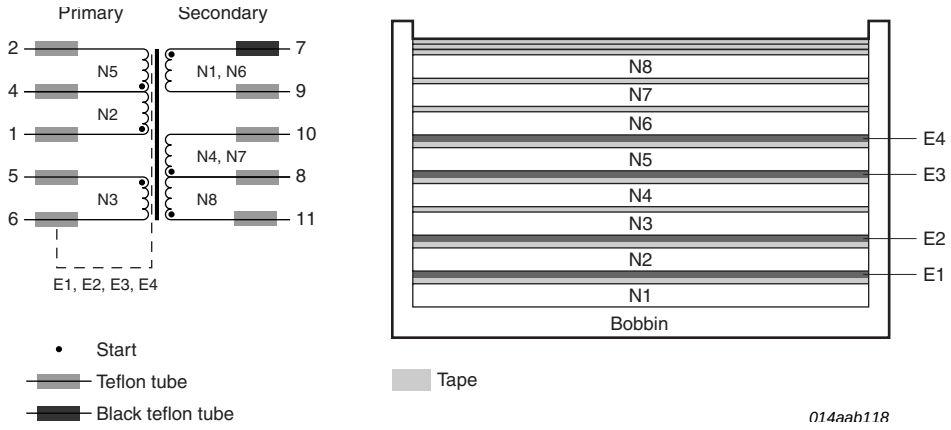


Fig 16. Flyback transformer schematic

Table 18. Flyback transformer winding details

Winding order		Pin number		Wire type	Number of wires	Number of turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1:	N1	7	9	TIW 0.3 mm ∅	2	6	1	TEX-E
2:	E1	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
3:	N2	1	4	2-UEW 0.5mm ∅	1	16	1	
4:	E2	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
5:	N3	5	6	2-UEW 0.25mm ∅	2	7	1	
6:	N4	8	10	TIW 0.3 mm ∅	2	6	1	TEX-E

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 18. Flyback transformer winding details

Winding order		Pin number		Wire type	Number of wires	Number of turns		Remarks
		Start	Finish			Winding	MYLAR tape	
7:	E3	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
8:	N5	4	2	2-UEW 0.5mm ∅	1	16	1	
9:	E4	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
10:	N6	7	9	TIW 0.3 mm ∅	2	6	1	TEX-E
11:	N7	8	10	TIW 0.3 mm ∅	2	6	1	TEX-E
12:	N8	11	8	TIW 0.3 mm ∅	1	5	3	TEX-E; close winding method

7.2 PFC inductor L2 specifications

- Primary inductance: 250 μH (±10 %).
- Core/bobbin: RM10.
- Core material: NC-2H.

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

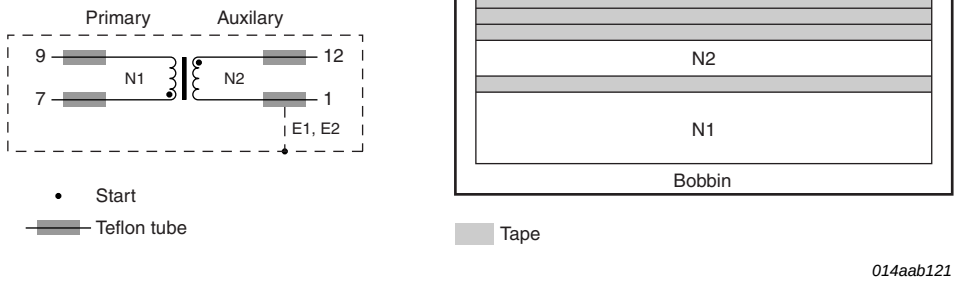


Fig 17. PFC inductor L2 schematic

Table 19. PFC inductor L2 winding details

Winding order		Pin no.		Winding type	Number of wires	Number turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1	N1	9	7	USTC 0.1 mm ∅	30	40 turns	1 turn	-
2	N2	12	1	2-UEW 0.22 mm ∅	2	2.5 turns	3 turns	-

8. PCB layout

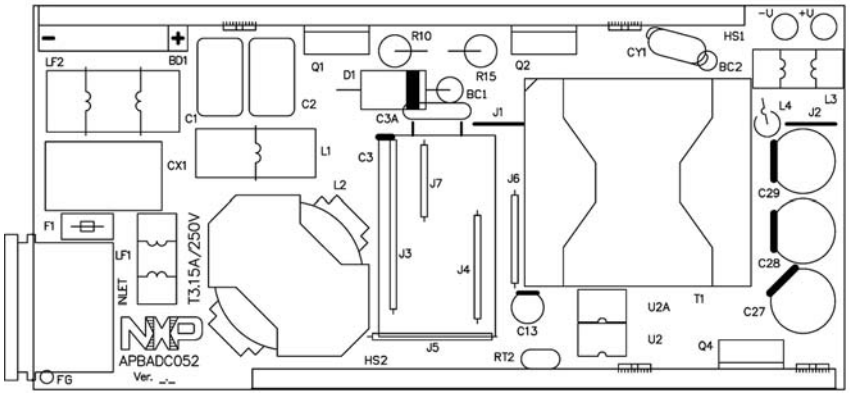
The SMPS printed circuit board is a single sided board. Dimensions are 125 mm x 59 mm.

The PCBs are 1.6 mm FR2 with single sided 2 oz. copper (70 m) layer.

The Gerber file set for production of the PCB is available through the local NXP Semiconductors sales office

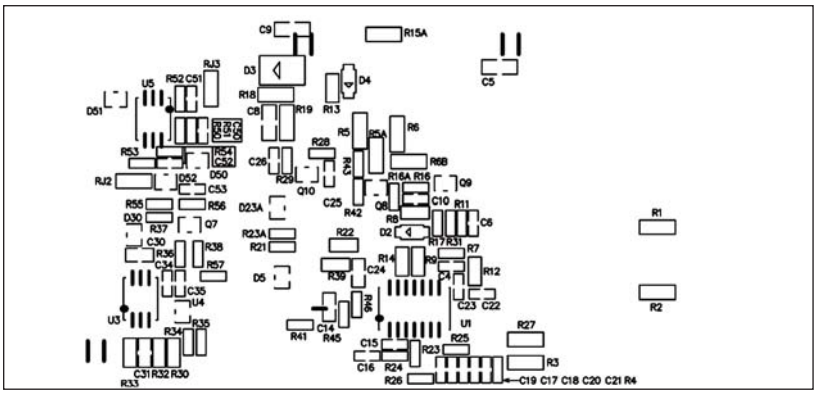
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



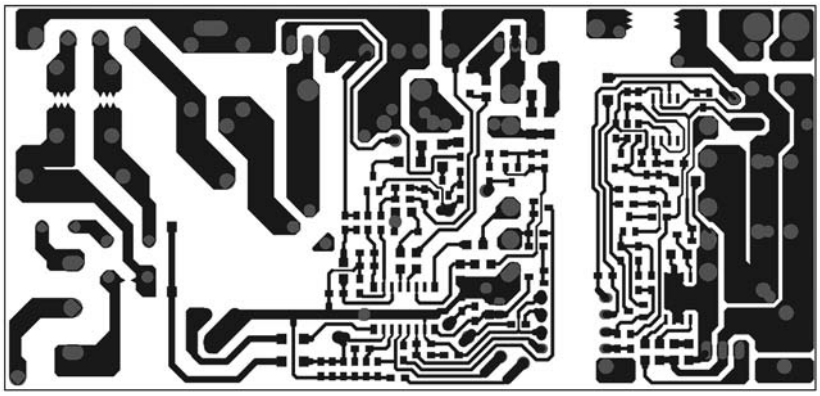
019aab488

Fig 18. Demo board top silk (top view)



019aab489

Fig 19. Demo board bottom silk (bottom view)



019aab490

Fig 20. Demo board bottom copper (bottom view)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

9. Abbreviations

Table 20. Abbreviations table

Acronym	Description
CC	Constant Current
CR	Constant Resistance
CV	Constant Voltage
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	ElectroMagnetic Susceptibility
ESD	ElectroStatic discharge
FLR	Fast Latch Reset
LISN	Line Impedance Standardization Network
MHR	Mains Harmonic Reduction
OTP	OverTemperature Protection
OCP	OverCurrent Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PE	Protective Earth
PFC	Power Factor Correction
SCP	Short-Circuit Protection
SMPS	Switched Mode Power Supply
SR	Synchronous Rectification
TIW	Triple Insulated Wire
UEW	polyUrethane Enameled Wire
USTC	polyUrethane Silk Tetrone Covered

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

10. Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits.

The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

11. Contents

1 Introduction 3
2 Specification. 4
3 Performance data. 5
3.1 Test setup 5
3.1.1 Test equipment 5
3.1.2 Test conditions 5
3.2 Efficiency 5
3.2.1 ENERGY STAR efficiency 5
3.2.1.1 Active mode efficiency 5
3.2.1.2 No-load input power 6
3.2.1.3 Full load efficiency PFC plus flyback stage . . . 7
3.3 Timing and protection 7
3.3.1 Switch-on delay and output rise time 7
3.3.2 Brownout and brownout recovery 9
3.3.3 Output short circuit protection 10
3.3.4 Output OverCurrent Protection (OCP) 12
3.3.5 Output OverVoltage Protection (OVP) 12
3.3.6 OverTemperature Protection (OTP) 13
3.3.7 Fast latch reset 14
3.4 Output regulation and characterization 15
3.4.1 Load regulation 15
3.4.2 Line regulation 16
3.4.3 Ripple and noise PARD (Periodic And Random Deviation) 16
3.4.4 Dynamic load response 17
4 ElectroMagnetic Compatibility (EMC) 19
4.1 Conducted emission 19
4.2 Immunity against lighting surges 20
4.3 Immunity against ESD 21
4.4 Mains harmonic reduction 21
5 Schematic 23
6 Bill of materials 25
7 Transformer and inductor specifications . . . 28
7.1 Flyback transformer T1 specifications 28
7.2 PFC inductor L2 specifications 29
8 PCB layout 29
9 Abbreviations 31
10 Legal information. 32
10.1 Definitions 32
10.2 Disclaimers 32
10.3 Trademarks. 32
11 Contents 33

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 April 2011
Document identifier: UM10444