CMOS ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER

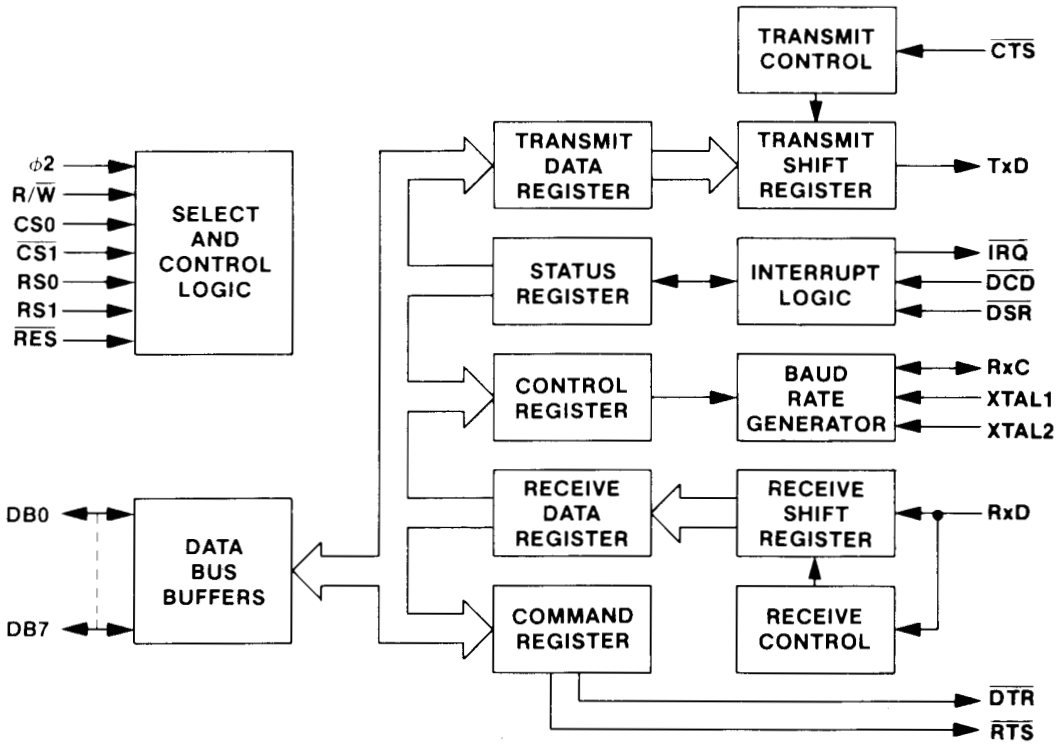
FEATURES

- CMOS process technology for low power consumption
- 15 programmable baud rates (50 to 19,200 baud)
- External 16X clock input for nonstandard baud rates to 125,000 baud
- Programmable interrupt and status registers
- Full-duplex or half-duplex operating modes
- Selectable 5, 6, 7, 8 or 9 bit transmission rates
- Programmable word length, parity generation and detection, and number of stop bits
- Programmable parity options - odd, even, none, mark or space
- Includes data set and modem control signals
- False start bit detection
- Serial echo mode
- Four operating frequencies - 1, 2, 3 and 4 MHz

GENERAL DESCRIPTION

The CMD G65SC51 is an Asynchronous Communications Interface Adapter which offers many versatile features for interfacing 6500/6800 microprocessors to serial communication data sets and modems. The G65SC51's most significant feature is its internal baud rate generator, allowing programmable baud rate selection from 50 to 19,200 baud. This full range of baud rates is derived from a single standard 1.8432 MHz external crystal. For non-standard baud rates up to 125,000 baud, an external 16X clock input is provided. In addition to its powerful communications control features, the G65SC51 offers the advantages of CMD's leading edge CMOS technology, i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

Block Diagram



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Absolute Maximum Ratings: (See Note)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating. Note: Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70° Commercial

Parameter	Symbol	Min	Max	Unit
Input High Voltage (Except XTAL1)	V_{IH}	2.0	V_{DD} + 0.3	V
Input High Voltage (XTAL1 only)	V_{IHX}	3.1		V
Input Low Voltage (Except XTAL1)	V_{IL}	-0.3	0.8	V
Input Low Voltage (XTAL1 only)	V_{ILX}		1.9	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins	I_{IN}		±1.0	µA
Three-State Leakage Current, (V_{IN} = 0.4 to 2.4V)	I_{TSI}		±10.0	µA
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200µA)	V_{OH}	2.4		V
Supply Current (No Load) f = 1MHz f = 2MHz f = 3MHz f = 4MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1MHz) Standby (Static)	P_D P_{DSB}		11.0 300	mW µW
Input Capacitance (f = 1MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1MHz)	C_{OUT}		10.0	pF

AC Characteristics - Processor Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	-	500	-	330	-	250	-	ns
Phase 2 Pulse Width High	t_{PWH}	470	-	240	-	160	-	120	-	ns
Phase 2 Pulse Width Low	t_{PWL}	470	-	240	-	160	-	120	-	ns
Phase 2 Transition	$t_{R,F}$	-	30	-	30	-	30	-	30	ns
Read Timing										
Select, R/W* Setup	t_{ACR}	160	-	90	-	65	-	45	-	ns
Select, R/W* Hold	t_{CAR}	0	-	0	-	0	-	0	-	ns
Data Bus Delay	t_{CDR}	-	320	-	190	-	130	-	90	ns
Data Bus Hold	t_{HR}	10	-	10	-	10	-	10	-	ns
Write Timing										
Select R/W* Setup	t_{ACW}	160	-	90	-	65	-	45	-	ns
Select R/W* Hold	t_{CAW}	0	-	0	-	0	-	0	-	ns
Data Bus Setup	t_{DCW}	195	-	90	-	65	-	45	-	ns
Data Bus Hold	t_{HW}	10	-	10	-	10	-	10	-	ns

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AC Characteristics - Transmit/Receive Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Transmit/Receive Clock Cycle Time(1)	t_{CCY}	400	-	400	-	400	-	400	-	ns
Transmit/Receive Clock High Time	t_{CH}	175	-	175	-	175	-	175	-	ns
Transmit/Receive Clock Low Time	t_{CL}	175	-	175	-	175	-	175	-	ns
XTAL 1 to TxD Propagation Delay	t_{DD}	-	500	-	330	-	250	-	250	ns
Propagation Delay (RTS*, DTR*)	t_{DLY}	-	500	-	330	-	250	-	250	ns
IRQ* Propagation Delay (Clear)(2)	t_{IRQ}	-	500	-	500	-	500	-	500	ns

(1) The baud rate with external clocking is Baud Rate = $\frac{1}{16 \times t_{CCY}}$

(2) Propagation Delay is a function of external RC time constant.

Timing Diagrams

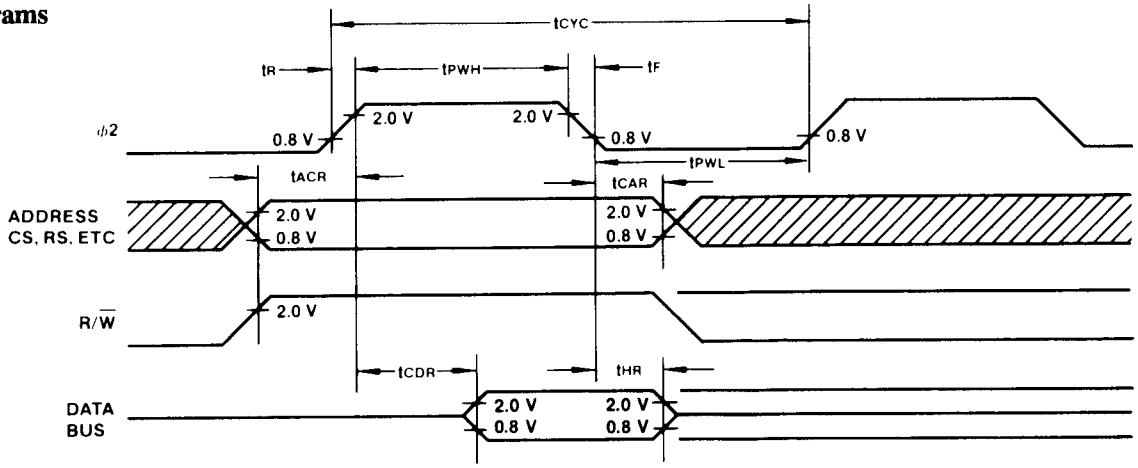


Figure 1. Read Timing

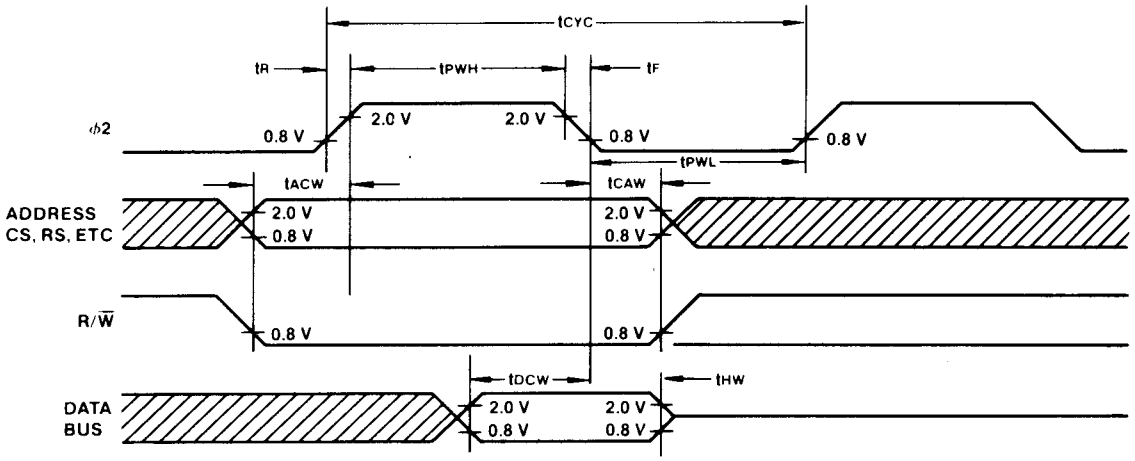
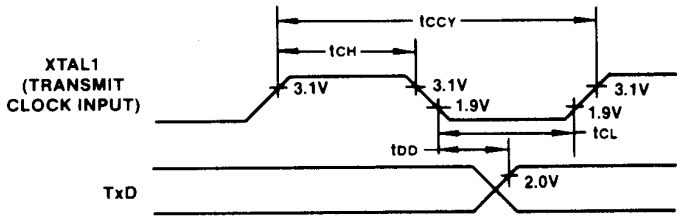


Figure 2. Write Timing

Note: Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

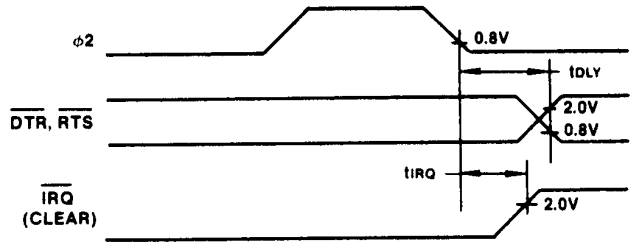
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Timing Diagrams (cont.)



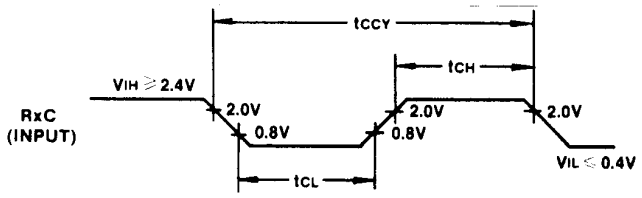
NOTE: 1. TxD is 1/16 TxC rate.
2. XTAL input voltage VIL ≤ 1.5V, VIH ≥ 3.5V.

Figure 3. Transmit Timing External Clock



NOTE: 1. Voltage levels shown are VIL ≤ 0.4V, VIH ≥ 2.4V.

Figure 4. Interrupt and Output Timing



NOTE: 1. RxD rate is 1/16 RxC rate.
2. Voltage levels shown are VIL ≤ 0.4V, VIH ≥ 2.4V.

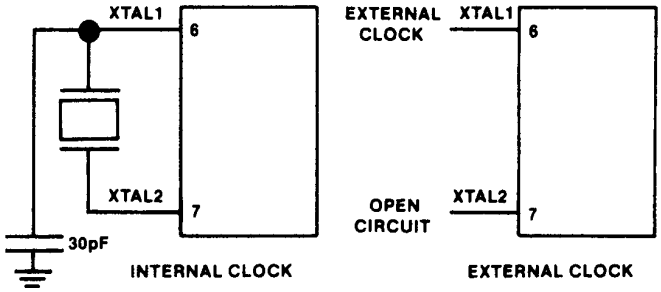
Figure 5 - Receive External Clock Timing

Test and Crystal Specifications

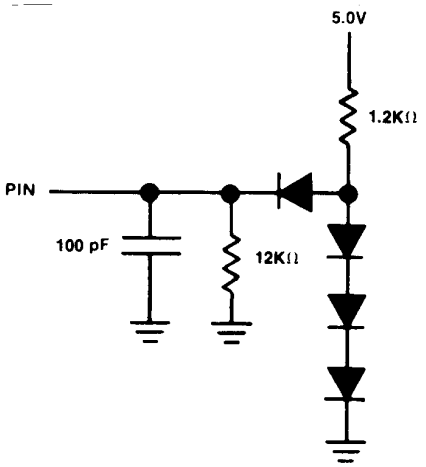
1. Temperature stability ± 0.01% (-40°C to +85°C)
2. Characteristics at 25°C ± 2°C

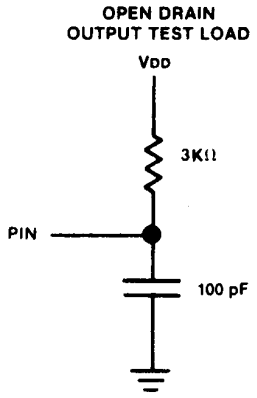
a. Frequency (MHz)	1.8432
b. Frequency tolerance (±%)	0.02
c. Resonance mode	Series
d. Equivalent resistance (ohm)	400 max.
e. Drive level (mW)	2
f. Shunt capacitance (pF)	7 max.
g. Oscillation mode	Fundamental

Clock Generation - G65SC51



Test Load





* Denotes inverted signal.

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Signal Description (Microprocessor Interface)

Reset (RES*)
Reset clears all internal registers during system initialization.

Interrupt Request (IRQ*)
The Interrupt Request (IRQ*) output signal is generated by the Interrupt Control Logic. IRQ* is normally held to a high level and goes low when an interrupt occurs. IRQ* is an open-drain output, thus allowing the IRQ* signal to be wire-ORed to a common microprocessor Interrupt input line.

Read/Write (R/W*)
The R/W* signal is generated by the microprocessor and is used to control the transfer of data between the G65SC51 and the microprocessor. When R/W* is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC51 to the microprocessor (Read operation). Conversely, when R/W* is in the low state (Logic 0), data is transferred from the processor to the G65SC51 (Write operation).

Input Clock (ϕ2)
The ϕ2 clock is used to trigger all data transfers between the microprocessor and the G65SC51.

Data Bus (DB0-DB7)
The eight bidirectional Data Bus lines are used to transfer data between the G65SC51 and the microprocessor. During a Read operation, data is transferred from the G65SC51 to the microprocessor. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to the G65SC51. The Data Bus lines are in the high impedance state when the G65SC51 is unselected.

Chip Select (CS0, CS1*)
The two Chip Select lines are normally connected to the processor address lines either directly or through decoders. To access a selected G65SC51, CS0 must be high (Logic 1) and CS1* must be low (Logic 0).

Register Select (RS0, RS1)
The two Register Select lines are normally connected to the processor address lines. This allows the processor to select the various G65SC51 internal registers. Refer to Table 1 for internal register select coding.

Table 1. Register Select Coding

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control Registers can be accessed during both Read and Write operations. Programmed Reset operation does not cause data transfer, but is used to clear (reset) all G65SC51 internal registers. Programmed Reset is used in a slightly different way as compared to the hardware Reset (RES*). These differences are described under each individual register description.

Signal Description (Communication Interface)

Transmit Data (TxD)
TxD is an output line used to transfer NRZ (Non-Return-to-Zero) data to a modem. The LSB (Least Significant Bit) of the Transmit Data Register is the first data bit transmitted. The rate of data transmission (baud rate) is determined by the selected baud rate.

Receive Data (RxD)
RxD is an input line used to receive NRZ input data from a modem. The LSB is always the first data bit received. Received data will always be at the G65SC51's internally programmed baud rate or the baud rate of an externally generated receiver clock. The baud rate is a selection which is made by programming the Control Register. See Figure 6, Control Register Format.

Receive Clock (RxC)
RxC serves as a bidirectional "pin" which can be either the 16X Clock Input or the receiver 16X Clock Output. The 16X Clock Output mode results if the internal baud rate generator is selected for External Receiver Clocking. See Figure 6, Control Register Format.

Request to Send (RTS*)
RTS* is an output line used as a control function to the modem. The state of RTS* is determined by the contents of the Command Register. Refer to Figure 7, Command Register Format.

Data Carrier Detect (DCD*)
DCD* is an input line used to indicate carrier-detect output status from the modem. A low level indicates the modem carrier signal is present, and a high level indicates the modem carrier signal is not present. DCD* is a high impedance input and must not be used as a no-connect. That is, if unused, this pin must be driven high or low, but not switched.

NOTE: If Command Register Bit 0 is a high (Logic 1) and a change of state on DCD* occurs, IRQ* will be set, and the Status Register Bit 5 will reflect the new level. The state of DCD* does not affect Transmitter operation, but must be low (Logic 0) for the Receiver to operate.

Clear to Send (CTS*)
CTS is an input used to control Transmitter operation. The Transmitter is enabled when CTS* is low (Logic 0), and is automatically disabled when CTS* is high (Logic 1).

Data Terminal Ready (DTR*)
DTR is an output line used to indicate G65SC51 status to the modem, and is controlled by the processor via Bit 0 of the Command Register. DTR* low (Logic 0) indicates the G65SC51 is enabled, while DTR* high (Logic 1) indicates the device is disabled.

Data Set Ready (DSR*)
DSR* is an input line used to indicate modem status to the G65SC51. DSR* low (Logic 0) indicates the modem is "ready", while a high (Logic 1) indicates the modem is in a "not ready" state. Like DCD, DSR is a high impedance input and must not be used as a no-connect. If unused, this line must be driven either high or low, but not switched.

NOTE: If Command Register Bit 0 is high (Logic 1) and a change of state on DSR* occurs, IRQ* will be set, and Status Register Bit 6 will reflect the new level. The state of DSR* does not affect either Transmitter or Receiver operation.

* Denotes inverted signal.

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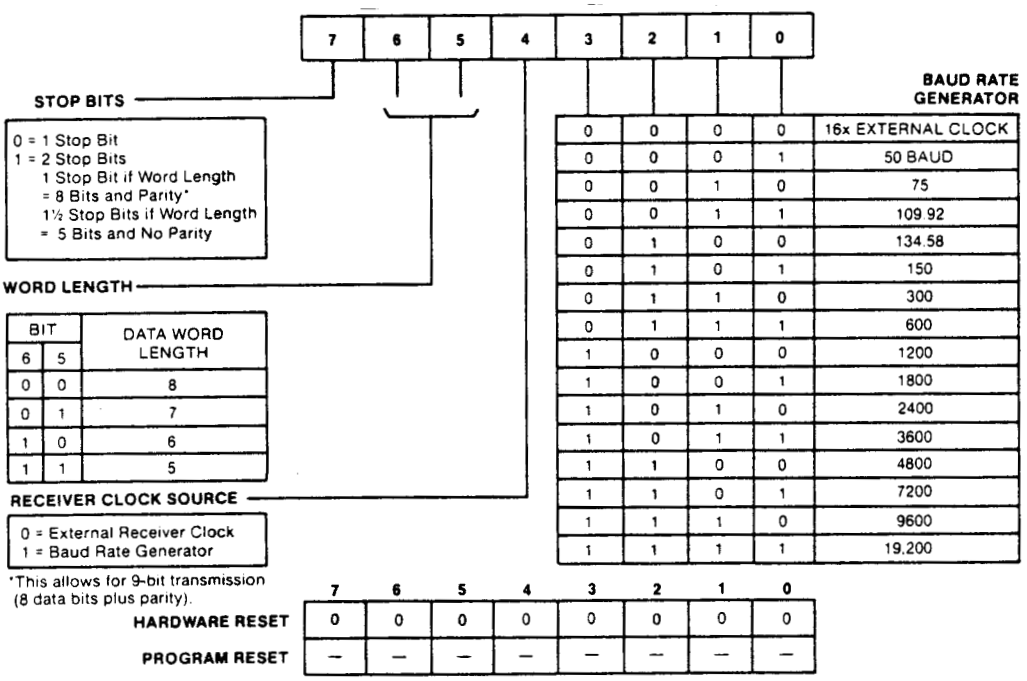


Figure 6 - Control Register Format

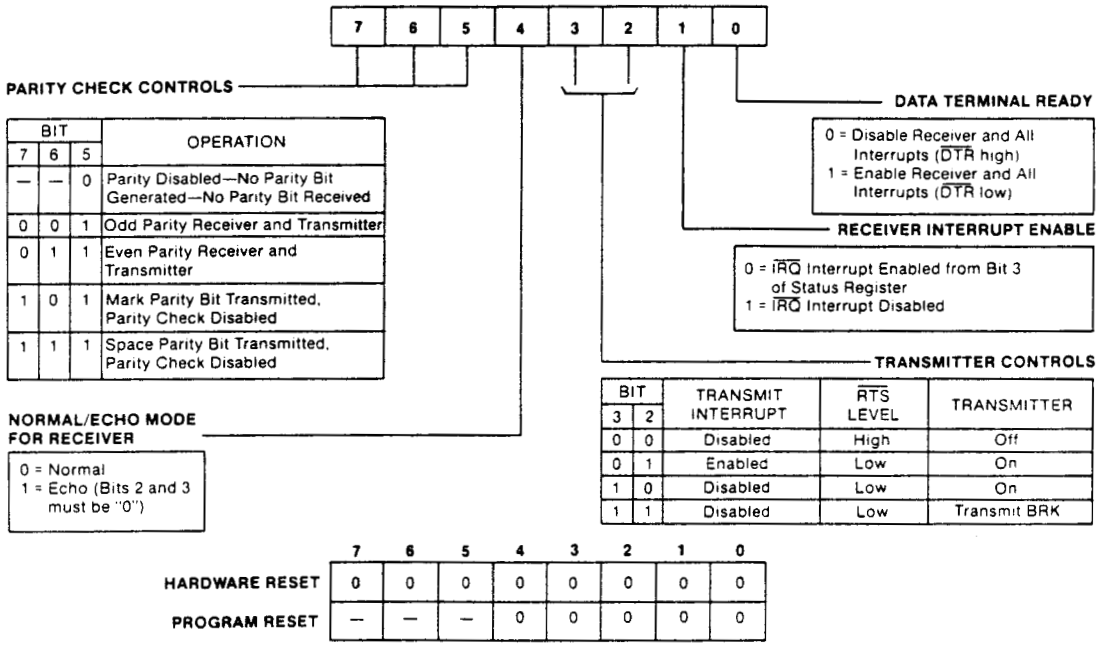


Figure 7 - Command Register Format

*** Denotes inverted signal.**

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External Crystal Pins (XTAL1, XTAL2)

These two crystal pins are normally used to connect an external crystal (1.8432 MHz) to the internal baud rate generator. This crystal is used to derive the full range of available baud rates. For nonstandard baud rates, an externally generated clock may be connected to the XTAL1 pin. In this case, the XTAL2 pin must float.

Internal Functions

Figure 8 shows the Transmitter/Receiver sections of the G65SC51. Bits 0-3 of the Control Register are used to select the "divisor" which in turn generates the selected baud rate for the Transmitter. Should the Receiver clock be using the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the G65SC51.

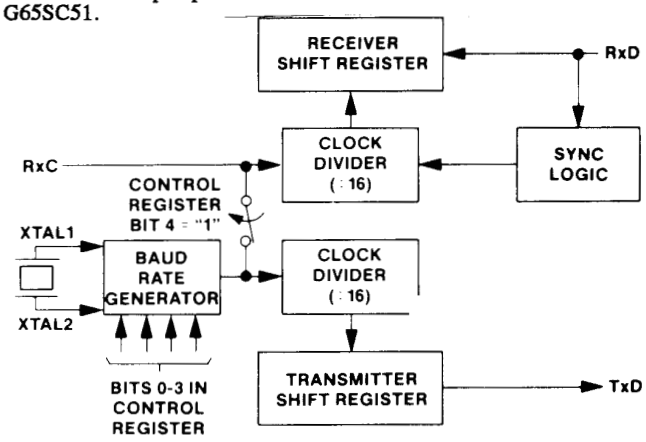


Figure 8. Transmitter/Receiver Clock Circuits

Control Register

The Control Register selects the various operating modes for the G66SC51. Note that the Baud Rate Generator, word length, number of stop bits and Receiver Clock Source are all controlled by the Control Register. Refer to Figure 6, Control Register Format, for detailed operation and programming information.

Command Register

The Command Register is used to control Transmit/Receive functions. Refer to Figure 7, Command Register Format, for detailed operation and programming information.

Transmit and Receive Data Registers

The Transmit and Receive Data Registers are used as temporary data storage within the G65SC51. Transmit Data Register characteristics are as follows:

- Bit 0 is always the leading bit during any transmission.
- Unused data bits are always the high-order bits in the data word. These unused high-order bits are "don't care" during data transmission.

Receive Register characteristics are as follows:

- Bit 0 is always the leading bit during any transmission.
- Unused data bits are always the high-order bits and are "zeros" for the receiver.
- Parity bits are not stored in the Receive Register. The parity bits are stripped off after being used for external parity checking. Therefore, received data in the Receive Data Register will have all parity and unused high-order bits as "zeros".

Figure 9 shows an example of a transmitted or received data word which contains eight data bits, a parity bit and a single stop bit.

Status Register

The Status Register indicates to the processor the status of various G65SC51 functions. Refer to Figure 10 for detailed Status Register operation and programming information.

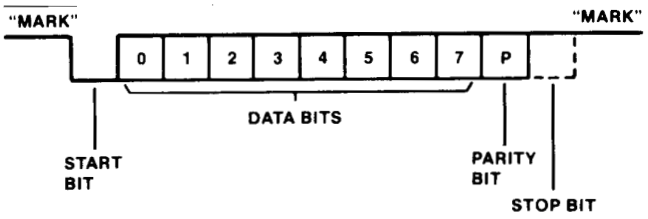
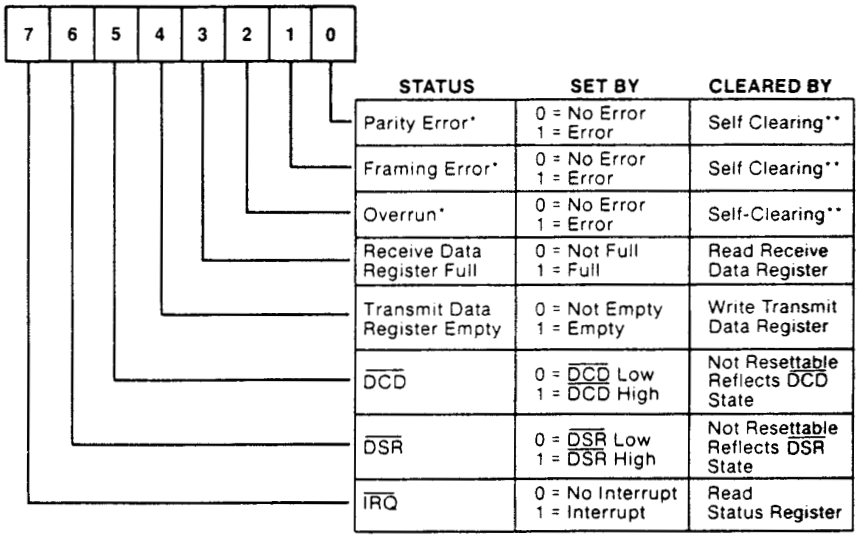


Figure 9. Serial Data Stream Example



*NO INTERRUPT GENERATED FOR THESE CONDITIONS
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR-FREE RECEIPT OF DATA

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	--	--	1	0	0	0	0
PROGRAM RESET	—	—	—	—	—	0	—	—

Figure 10. Status Register Format

* Denotes inverted signal.

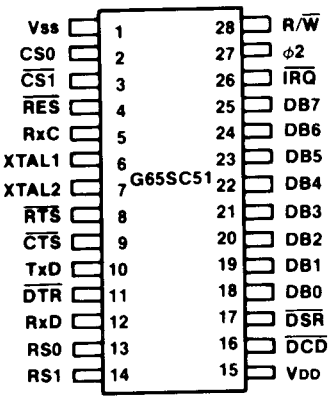
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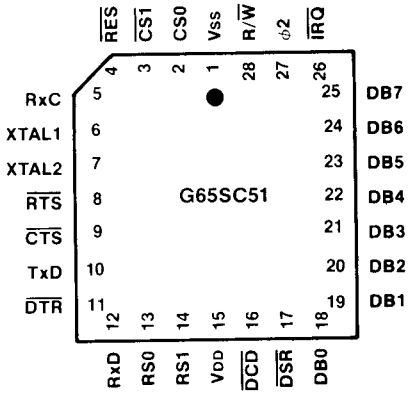
Pin Function Table

CS0, $\overline{CS1}$	Chip Select
$\overline{RES}$	Reset
$\phi 2$	Input Clock
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request
RS0, RS1	Register Selects
XTAL1, XTAL2	Crystal Inputs
TxD	Transmit Data
RxD	Receive Data

RxC	Receive Clock
$\overline{RTS}$	Request to Send
$\overline{CTS}$	Clear to Send
$\overline{DTR}$	Data Terminal Ready
$\overline{DSR}$	Data Set Ready
$\overline{DCD}$	Data Carrier Detect
DB0-DB7	Data Bus
V_{DD}	Positive Power Supply (+5.0 volts)
V_{SS}	Internal Logic Ground

Pin Configuration

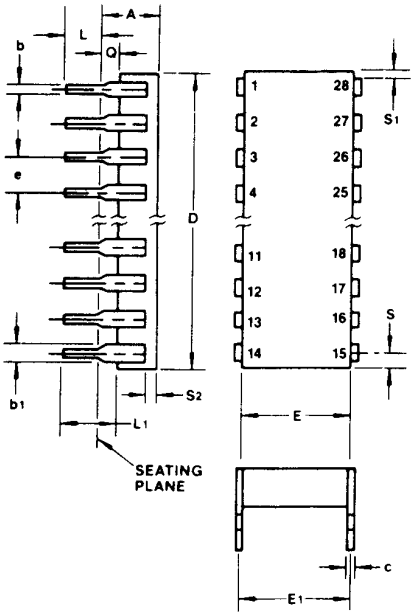




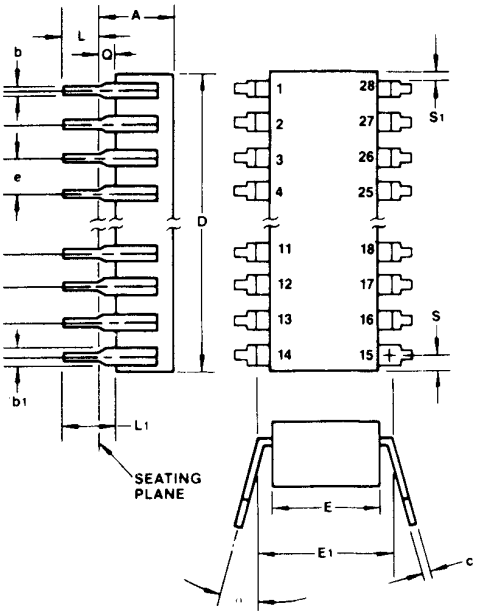
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Packaging Information

Ceramic Package

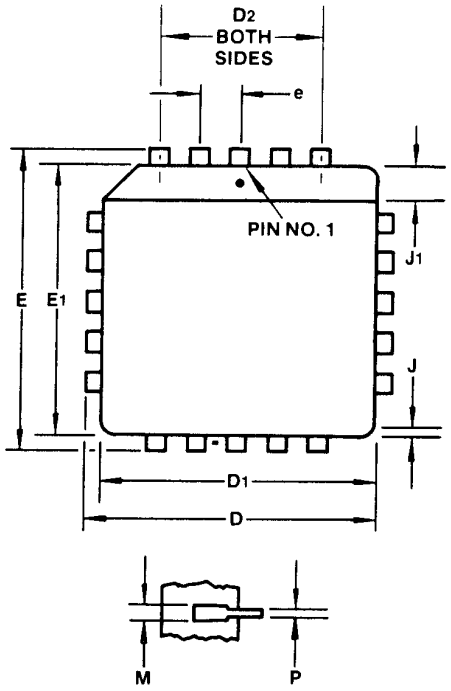


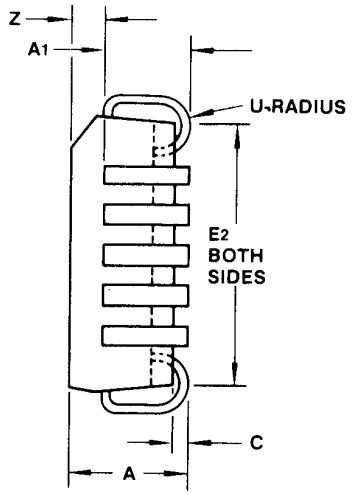
Plastic & Cerdip Package



28-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.490	—	53.24
E	0.510	0.620	12.95	15.75
E1	0.520	0.630	13.21	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.020	0.060	0.51	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

Plastic Leaded Chip Carrier



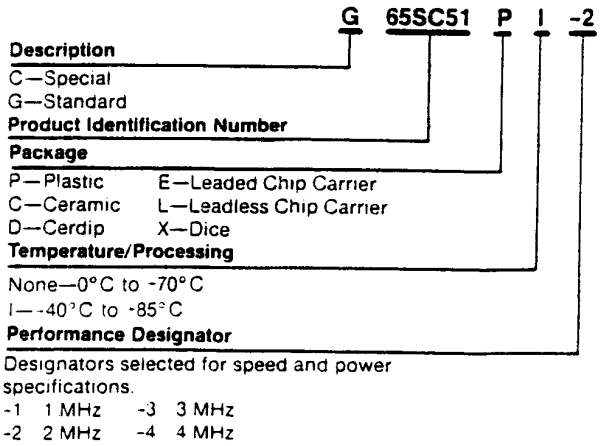


N = NO. LEADS

28-LEAD CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.20	4.57
A1	0.090	0.120	2.29	3.04
C	0.020	—	0.51	—
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.430	11.582
D2	0.300 REF		7.62 BSC	
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.430	11.582
E2	0.390	0.430	9.91	10.92
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	28		28	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

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Ordering Information



Warning

MOS Circuits are subject to damage from static discharge. Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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NOTES:

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