
EM83040 LCD driver

1.General description

The EM83040 is a dot matrix LCD driver which is fabricated by low power CMOS technology. This chip includes 80- bits shift register , 80 bits data latch and 80 bits level driver. A LCD RAM inside can be mapping to LCD signal. It converts RAM data to parallel data and output lcd waveform to LCD.

2.Features

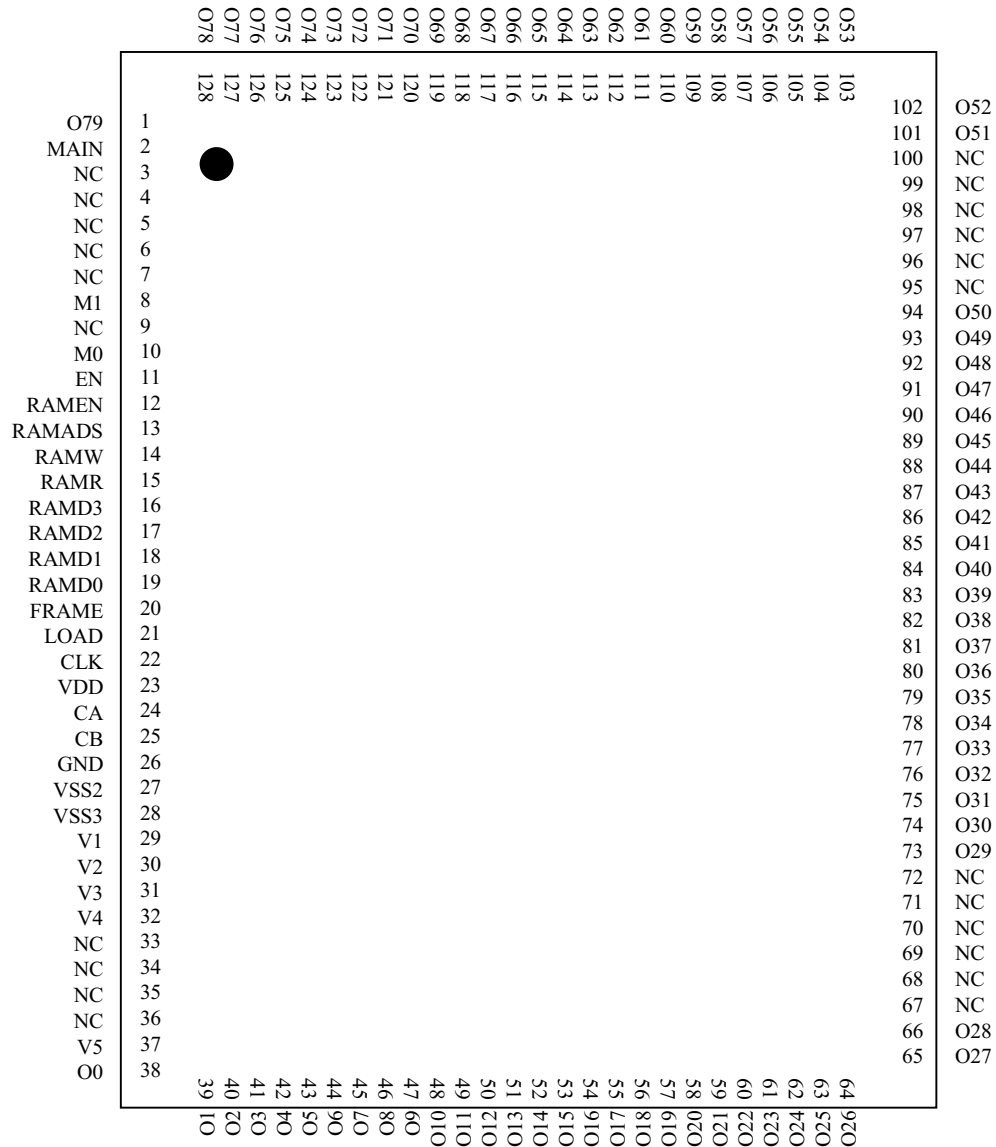
- (1) Supply power 2.4~6V
- (2) Internal RAM : 2.5k x 4 bits
- (3) RAM can be controlled by eight signals including four bit data bus.
- (4) LCD drive voltage :<18V
- (5) Duty: 1/32, 1/48, 1/80
- (6) Bias voltage can be supplied externally
- (7) Build in DC converter double and triple
- (8) Modularized function: connect to another 83040 to extent LCD matrix
- (9) One DC converter enabled and other 83040 can shared with this.
- (10) Chip form (EM83040H), 128 pin package (14mm x 20mm EM83040AQ), 160 pin package (EM83040BQ)

3.Application

- (1) Data Bank
- (2) LCD toy
- (3) Education computer

4.Pin assignment

EM83040AQ





EM83040BQ

	NC	121	120	NC
	NC	122	119	NC
	NC	123	118	NC
	NC	124	117	NC
	NC	125	116	NC
	051	126	115	NC
	052	127	114	NC
	053	128	113	NC
	054	129	112	NC
	055	130	111	NC
	056	131	110	O50
	057	132	109	O49
	058	133	108	O48
	059	134	107	O47
	060	135	106	O46
	061	136	105	O45
	062	137	104	O44
	063	138	103	O43
	064	139	102	O42
	065	140	101	O41
	066	141	100	O40
	067	142	99	O39
	068	143	98	O38
	069	144	97	O37
	070	145	96	O36
	071	146	95	O35
	072	147	94	O34
	073	148	93	O33
	074	149	92	O32
	075	150	91	O31
	076	151	90	O30
	077	152	89	O29
	078	153	88	NC
	079	154	87	NC
	MAIN	155	86	NC
	M1	156	85	NC
	NC	157	84	NC
	NC	158	83	NC
	NC	159	82	NC
	NC	160	81	NC
NC	1		80	NC
NC	2		79	NC
NC	3		78	NC
NC	4		77	NC
NC	5		76	NC
NC	6		75	820
NC	7		74	820
NC	8		73	920
M0	9		72	520
EN	10		71	820
RAMEN	11		70	820
RAMADS	12		69	820
RAMW	13		68	820
RAMR	14		67	820
RAMD3	15		66	820
RAMD2	16		65	820
RAMD1	17		64	820
RAMD0	18		63	820
FRAME	19		62	820
LOAD	20		61	820
CLK	21		60	820
VDD	22		59	820
CA	23		58	820
CB	24		57	820
GND	25		56	820
VSS2	26		55	820
VSS3	27		54	820
V1	28		53	820
V2	29		52	820
V3	30		51	820
NC	31		50	820
NC	32		49	820
NC	33		48	820
NC	34		47	820
NC	35		46	820
NC	36		45	820
NC	37		44	820
NC	38		43	820
NC	39		42	820
NC	40		41	820

5. Block diagram

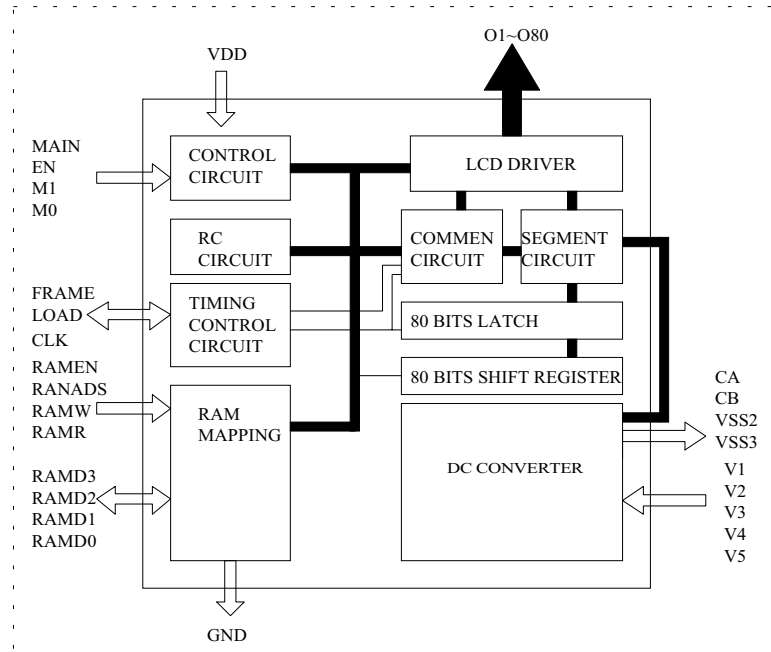


Fig2

6.Pin description

VDD	Power	
GND	power	Ground
VSS3	Power	EN=0 and MAIN=1, 2*VDD output, EN=1, VSS3=VDD
VSS2	Power	EN=0 and MAIN=1, 3*VDD output, EN=1, VSS2=VDD
MAIN	I	Master or slave control signal. MAIN=1 ,master unit MAIN=0 , slave unit
EN	I	This pin control whole chip power. This chip will work when this pin is connectted to ground. And whole chip will disable when connect to VDD voltage. EN=0 and MAIN=1 the chip will generate VSS2, VSS3, FRAME, LOAD, CLK signal and internal RC clock. EN=1, standby mode
M1	I	Mode select
M0	I	Mode select
RAMEN		RAM read and write control signal. 1 => can not read and write. 0=> can read and write.
RAMADS		RAM data select signal 1=> RAM Data , 0=>Address
RAMW		RAM write signal, low write
RAMR		RAM read signal, low read
RAMD3~RAMD0		RAM data or address bus
CLK	I/O	System clock. MAIN=1 , the master unit will output system clock. MAIN=0 , the slave will accept the clock from master unit.
LOAD	I/O	LCD load signal between one COMMON signal to another . MAIN=1 , the master unit will output LOAD signal. MAIN=0 , the slave will accept the signal from master unit.
FRAME	I/O	LCD frame control . MAIN=1 , the master unit will output FRAME signal. MAIN=0 , the slave will accept the signal from master unit.
CA	I	Coupling capacitor
CB	I	Coupling capacitor
V1~V5	I	Reference voltage input ,highest V1..lowest V5
O1~O80	O	LCD waveform output

7.Function description

(1)User can use MAIN pin to chose master unit or slave unit.

MAIN	Unit	Function
1	MASTER	Generate these signals Clk, Frame, Load, VSS2, VSS3, Internal RC clock
0	SLAVE	Accept these signals Clk, Frame, Load, V1, V2, V3, V4, V5

(2)User can use M1,M2 to chose four modes. As followed

MASTER	MAIN	M1	M0	Segment	Common	Ps.
Mode1	1	0	0	Reserved for test		
Mode2	1	0	1		O(80:1)=C(80:1)	
Mode3	1	1	0	O(32:1)=S(32:1)	O(80:33)=C(48:1)	
Mode4	1	1	1	O(48;1)=S(48:1)	O(80:49)=C(32:1)	
SLAVE	MAIN	M1	M0	Segment	Common	Ps.
Mode1	0	0	0	Reserved for test		M1, M0 should as same as master unit
Mode2	0	0	1	O(80:1)=S(80:1)		
Mode3	0	1	0	O(80:1)=S(80:1)		
Mode4	0	1	1	O(80:1)=S(80:1)		
				Ps: S=segment	C=common	

(3)RAM control

Write mode

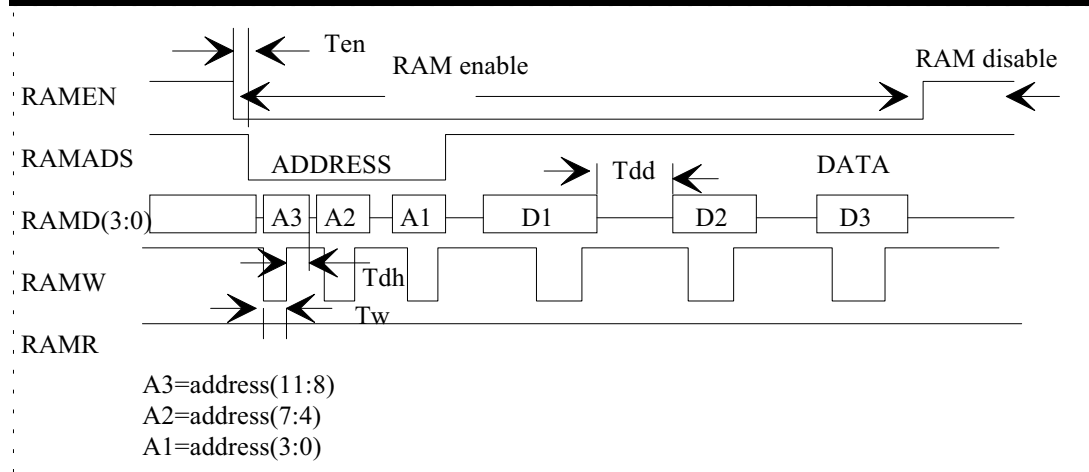


Fig3

LCD RAM can be written or read with control signal. The RAMEN pin can select a RAM which can be read or write. The RAMADS pin can select whether RAMD(3:0) are data or address of RAM. At the address mode, RAMADS is low and user should send address three times. From address (11:8) to address (3:0). Then it will go into data mode when RAMADS is high. In data mode, user can send one or more nibble data which address can be increased by internal counter.

Once the RAMEN pin is high, the RAM can not read and write.

(4)read mode

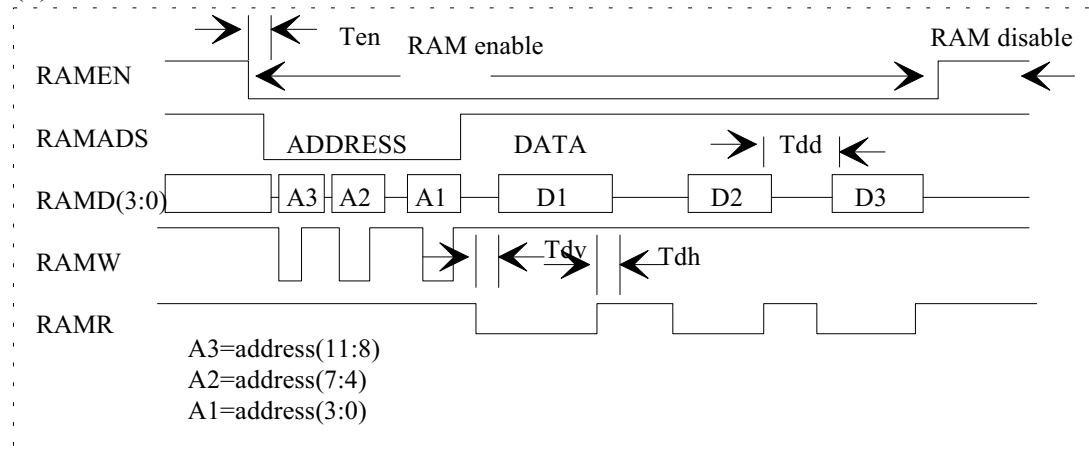


fig4

As same as write mode, user has to send address three times. And read data from RAM one by one which address can be increased by internal counter. Note!! Be sure to make RAMR low pulse 2 μ S ($Tdv + \text{data}$) width and 2 μ S (Tdd) high width at least.

(5)RAM mapping

RAM address is from 0 to address 2559

User fill “1” to LCD RAM , LCD driver will generate “light” waveform. Otherwise , it will generate a “dark” waveform. The LCD RAM area is mapped to segment 1 to segment 80 from address 0 to address 19. And user can refer to fig.5 to get the idea of

address2559	address2547.....	address2528	COM80
GENERAL RAM	LCD RAM		
address0063	address0039	address0032	COM2
address0031	address0019	address0000	COM1
	b3 b2 b1 b0	b3 b2 b1 b0	
	s80s79s78s77	s4 s3 s2 s1	

LCD ram mapping. The other RAM can use as general RAM for data storage.

Fig5

(6)LCD waveform

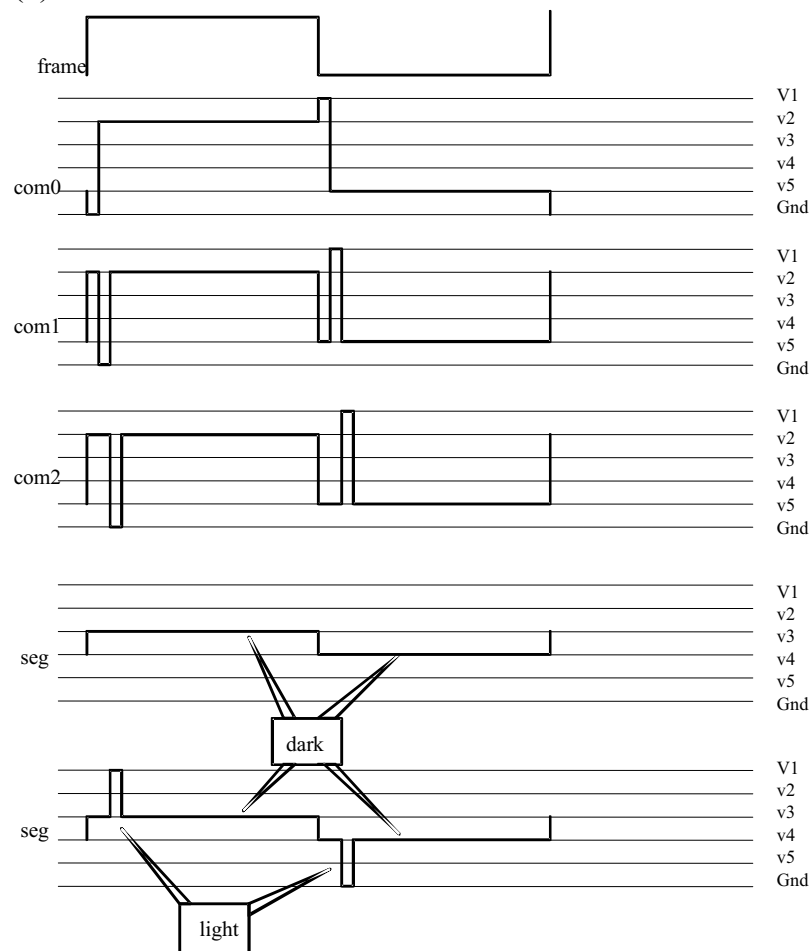


Fig6

8. Absolute rating

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	V+	<6	V
INPUT VOLTAGE	V _{in}	-0.5 TO V _{dd} +0.5	V
OPERATING TEMPERATURE RANGE	T _a	0 TO 70	°C

9. DC characteristic

(T_a=0°C ~ 70°C, V_{DD}=3V±5%, V_{SS}=0V)

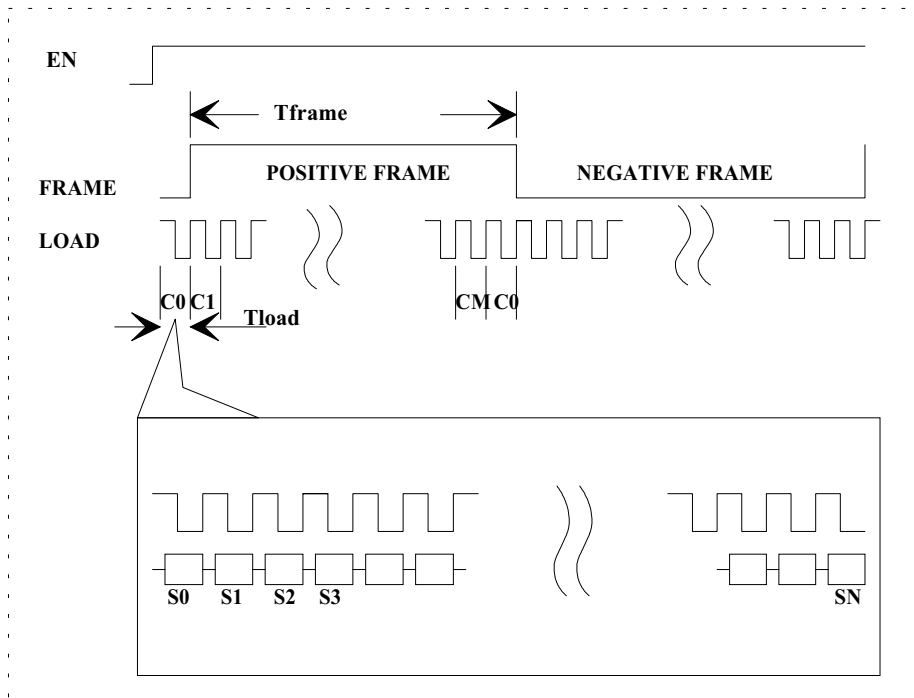
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IH}	Input High Voltage		2.0			V
V _{IL}	Input Low Voltage				0.8	V
I _{oh}	Output High current	V _{DD} =3V	100			μA
I _{ol}	Output low current	V _{DD} =3V	-100			μA
I _{sd}	Standby current	EN=1		1	4	μA
I _{op}	Operating current	EN=0 . MAIN =1 (MASTER) , DC converter enable, 1MHz clock INPUT=V _{DD}		400	600	μA
		EN=0 . MAIN =0 (SLAVE) , DC converter disable, 1MHz clock INPUT = V _{DD}		100	150	μA

10. AC Characteristic

(Ta=0°C ~ 70°C, VDD=3V, VSS=0V)

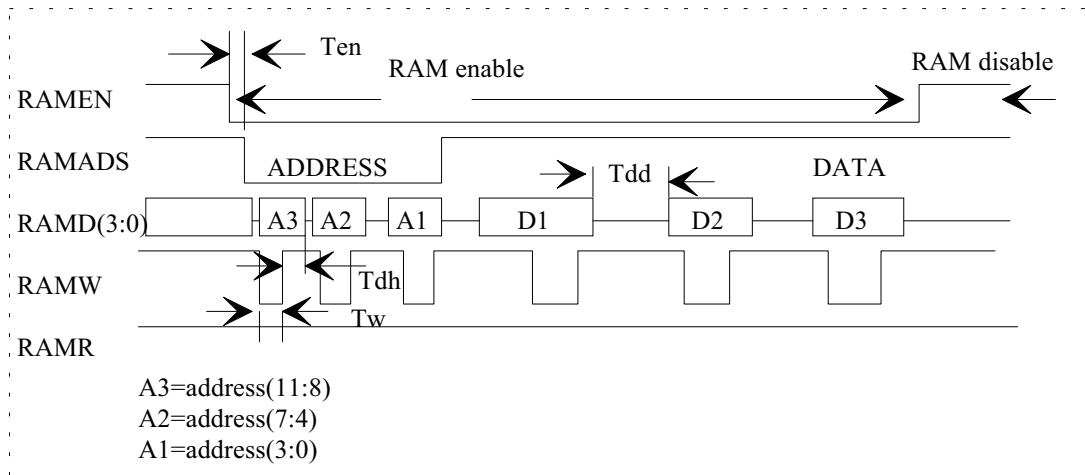
Symbol	Parameter	Min	Typ	Max	Unit
Tframe	Frame period		1/64		S
Tload	Load period		31		uS
Ten	Enable time	30			uS
Tw	Write low pulse	2			uS
Tdh	Data hold time	500			nS
Tdd	Data to data time	2			uS
Tdv	Data valid time	1500			nS

11. AC timing



LCD contrl timing

Fig7



LCD RAM write mode

Fig8

LCD RAM read mode

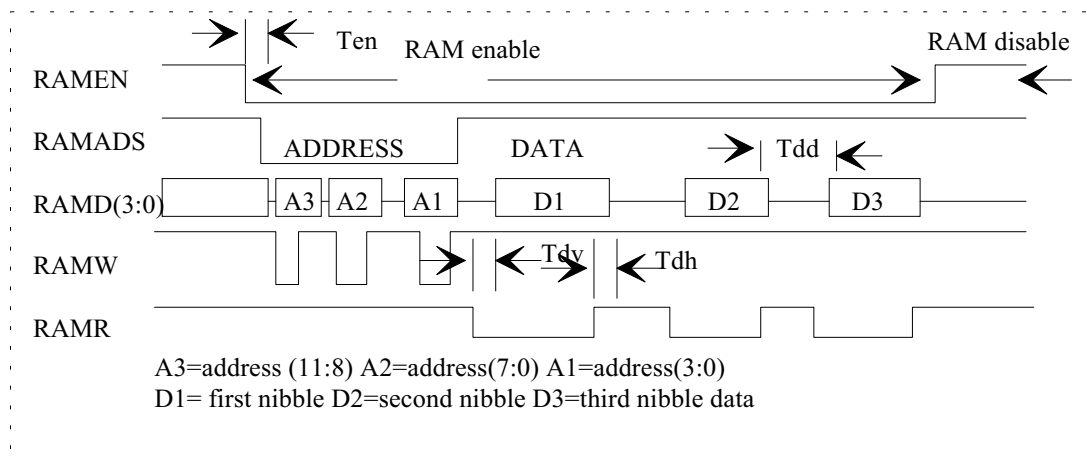


Fig9

12. Application circuit

(1), C32 x S48, 78861+83040

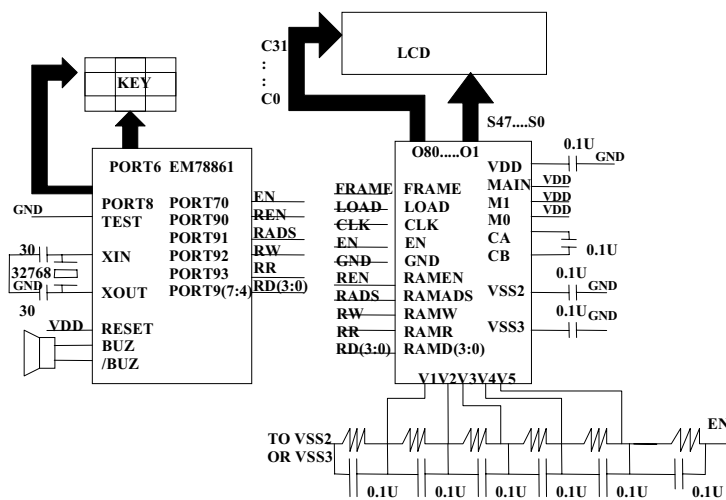


fig10

(2), C32 x S128, 78861 + 83040 + 83040

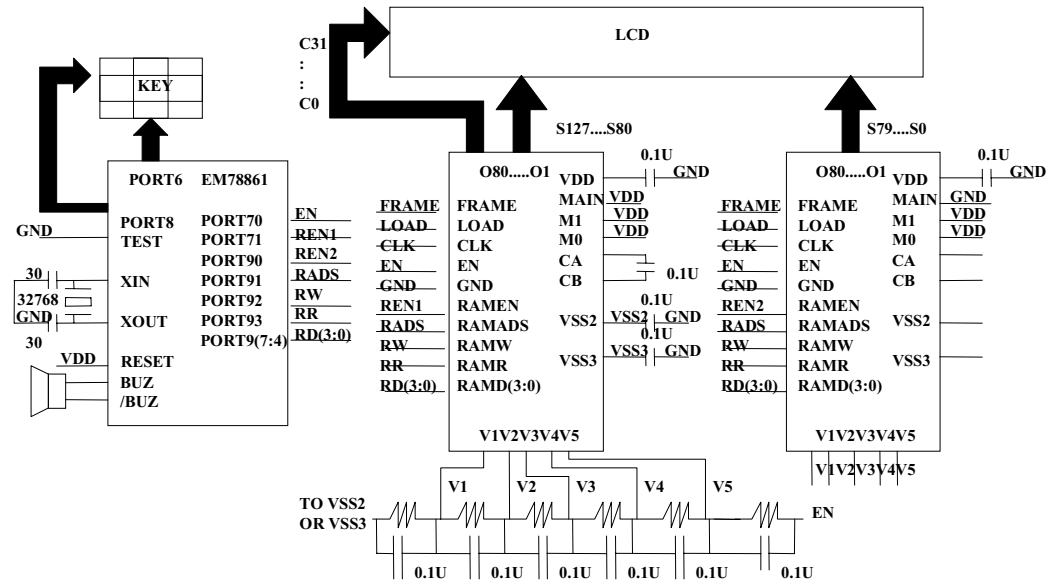


fig11

(3), C48 x S112, 78861 +83040 +83040

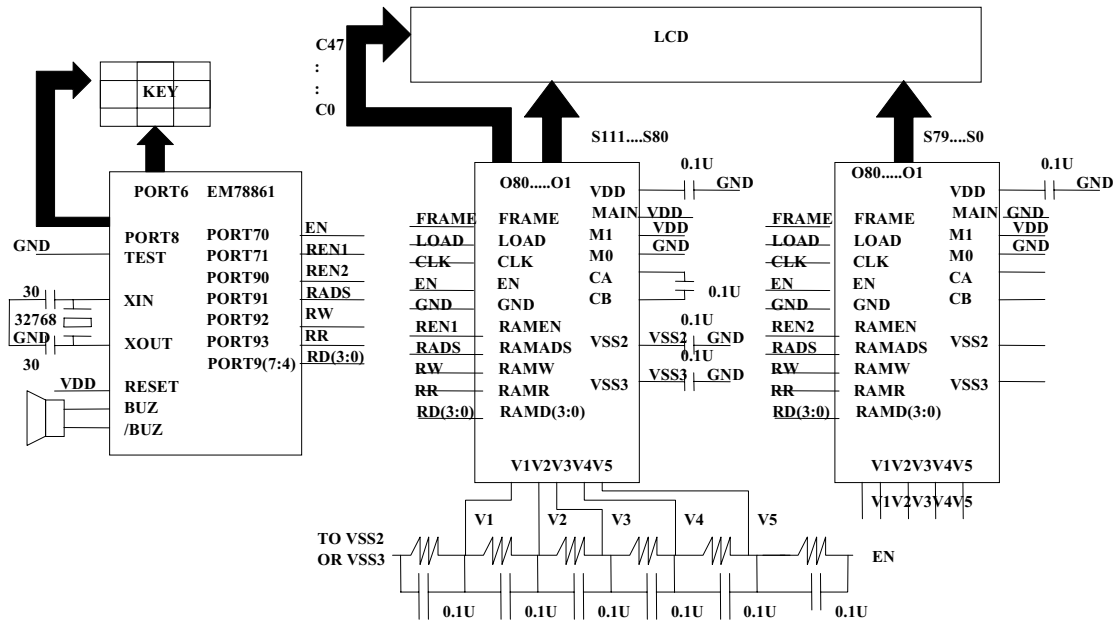


fig12

(4) C80 x S160, 78861 + 83040 +83040 +83040

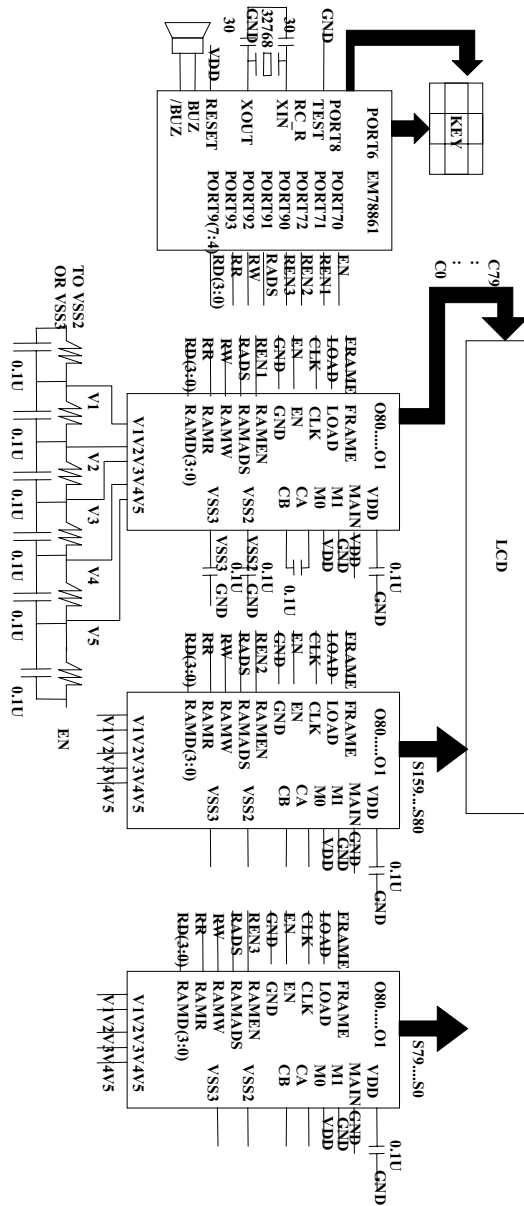
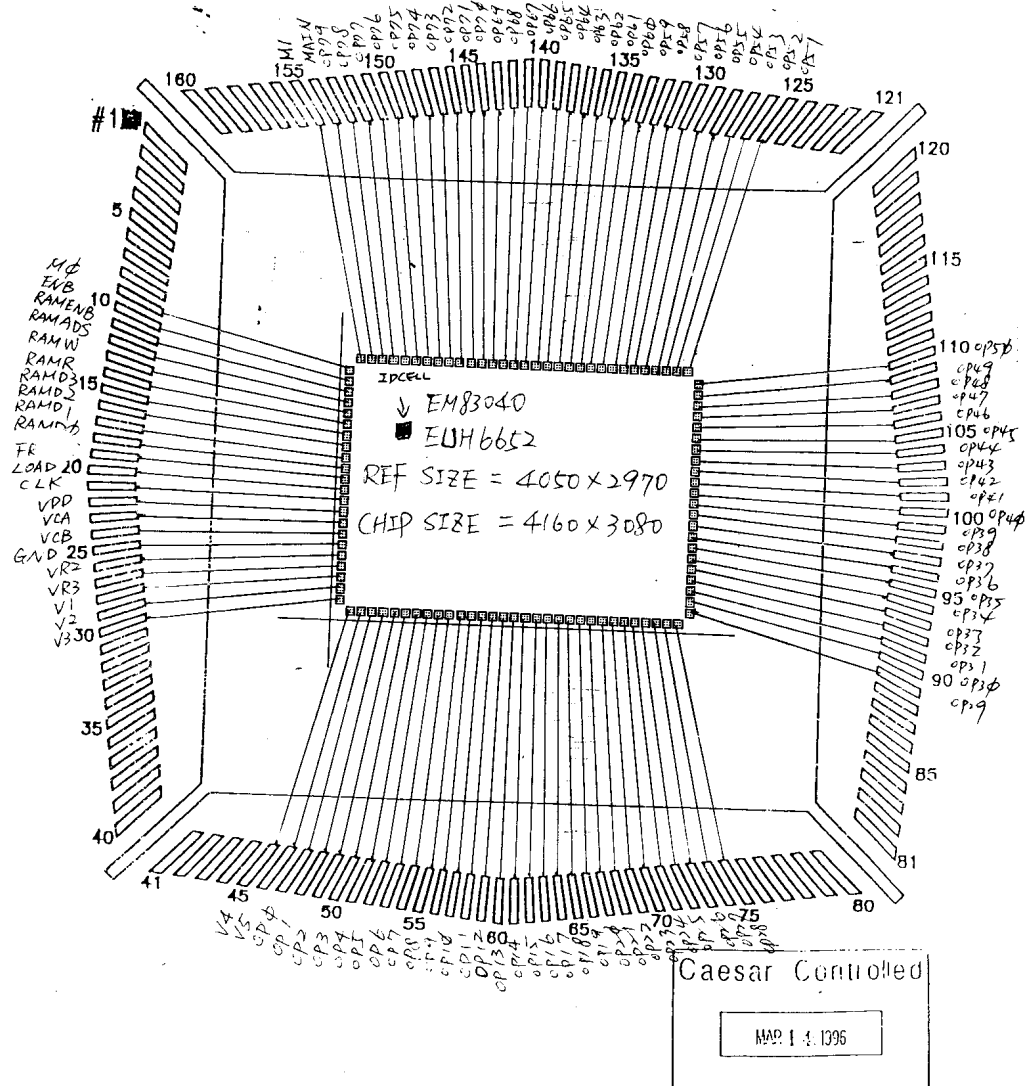


Fig13



euh6652 Pad Name & Cordinates Table			euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM			Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)	Pin No	Pad Name	Coordinate (X , Y)
1			26	VR2	-1920.0 ,-780.0
2			27	VR3	-1920.0 ,-900.0
3			28	V1	-1920.0 ,-1020.0
4			29	V2	-1920.0 ,-1140.0
5			30	V3	-1920.0 ,-1260.0
6			31		
7			32		
8			33		
9	M0	-1920.0 ,1260.0	34		
10	ENB	-1920.0 ,1140.0	35		
11	RAMENB	-1920.0 ,1020.0	36		
12	RAMADS	-1920.0 ,900.0	37		
13	RAMW	-1920.0 ,780.0	38		
14	RAMR	-1920.0 ,660.0	39		
15	RAMD_3_	-1920.0 ,540.0	40		
16	RAMD_2_	-1920.0 ,420.0	41		
17	RAMD_1_	-1920.0 ,300.0	42		
18	RAMD_0_	-1920.0 ,180.0	43		
19	FRAME	-1920.0 ,60.0	44		
20	LOAD	-1920.0 ,-60.0	45	V4	-1800.0 ,-1380.0
21	CLK	-1920.0 ,-180.0	46	V5	-1680.0 ,-1380.0
22	VDD	-1920.0 ,-300.0	47	OP_0_	-1560.0 ,-1380.0
23	VCA	-1920.0 ,-420.0	48	OP_1_	-1440.0 ,-1380.0
24	VCB	-1920.0 ,-540.0	49	OP_2_	-1320.0 ,-1380.0
25	GND	-1920.0 ,-660.0	50	OP_3_	-1200.0 ,-1380.0

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Structure Name: EUH6652 Chip Size: 4160 * 3080 UM			Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)	Pin No	Pad Name	Coordinate (X , Y)
51	OP_4_	-1080.0 , -1380.0	76		
52	OP_5_	-960.0 , -1380.0	77		
53	OP_6_	-840.0 , -1380.0	78		
54	OP_7_	-720.0 , -1380.0	79		
55	OP_8_	-600.0 , -1380.0	80		
56	OP_9_	-480.0 , -1380.0	81		
57	OP_10_	-360.0 , -1380.0	82		
58	OP_11_	-240.0 , -1380.0	83		
59	OP_12_	-120.0 , -1380.0	84		
60	OP_13_	0.0 , -1380.0	85		
61	OP_14_	120.0 , -1380.0	86		
62	OP_15_	240.0 , -1380.0	87		
63	OP_16_	360.0 , -1380.0	88		
64	OP_17_	480.0 , -1380.0	89	OP_29_	1920.0 , -1260.0
65	OP_18_	600.0 , -1380.0	90	OP_30_	1920.0 , -1140.0
66	OP_19_	720.0 , -1380.0	91	OP_31_	1920.0 , -1020.0
67	OP_20_	840.0 , -1380.0	92	OP_32_	1920.0 , -900.0
68	OP_21_	960.0 , -1380.0	93	OP_33_	1920.0 , -780.0
69	OP_22_	1080.0 , -1380.0	94	OP_34_	1920.0 , -660.0
70	OP_23_	1200.0 , -1380.0	95	OP_35_	1920.0 , -540.0
71	OP_24_	1320.0 , -1380.0	96	OP_36_	1920.0 , -420.0
72	OP_25_	1440.0 , -1380.0	97	OP_37_	1920.0 , -300.0
73	OP_26_	1560.0 , -1380.0	98	OP_38_	1920.0 , -180.0
74	OP_27_	1680.0 , -1380.0	99	OP_39_	1920.0 , -60.0
75	OP_28_	1800.0 , -1380.0	100	OP_40_	1920.0 , 60.0

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Pin No	Pad Name	Coordinate (X , Y)	Pin No	Pad Name	Coordinate (X , Y)
101	OP_41_	1920.0 ,180.0	126	OP_52_	1680.0 ,1380.0
102	OP_42_	1920.0 ,300.0	127	OP_53_	1560.0 ,1380.0
103	OP_43_	1920.0 ,420.0	128	OP_54_	1440.0 ,1380.0
104	OP_44_	1920.0 ,540.0	129	OP_55_	1320.0 ,1380.0
105	OP_45_	1920.0 ,660.0	130	OP_56_	1200.0 ,1380.0
106	OP_46_	1920.0 ,780.0	131	OP_57_	1080.0 ,1380.0
107	OP_47_	1920.0 ,900.0	132	OP_58_	960.0 ,1380.0
108	OP_48_	1920.0 ,1020.0	133	OP_59_	840.0 ,1380.0
109	OP_49_	1920.0 ,1140.0	134	OP_60_	720.0 ,1380.0
110	OP_50_	1920.0 ,1260.0	135	OP_61_	600.0 ,1380.0
111			136	OP_62_	480.0 ,1380.0
112			137	OP_63_	360.0 ,1380.0
113			138	OP_64_	240.0 ,1380.0
114			139	OP_65_	120.0 ,1380.0
115			140	OP_66_	0.0 ,1380.0
116			141	OP_67_	-120.0 ,1380.0
117			142	OP_68_	-240.0 ,1380.0
118			143	OP_69_	-360.0 ,1380.0
119			144	OP_70_	-480.0 ,1380.0
120			145	OP_71_	-600.0 ,1380.0
121			146	OP_72_	-720.0 ,1380.0
122			147	OP_73_	-840.0 ,1380.0
123			148	OP_74_	-960.0 ,1380.0
124			149	OP_75_	-1080.0 ,1380.0
125	OP_51_	1800.0 ,1380.0	150	OP_76_	-1200.0 ,1380.0



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