January 16, 2012

LMK00101

Ultra-low Jitter LVCMOS Fanout Buffer/Level Translator with Universal Input

1.0 General Description

The LMK00101 is a high performance, low noise LVCMOS fanout buffer which can distribute 10 ultra-low jitter clocks from a differential, single ended, or crystal input. The LMK00101 supports synchronous output enable for glitch free operation. The ultra low-skew, low-jitter, and high PSRR make this buffer ideally suited for various networking, telecom, server and storage area networking, RRU LO reference distribution, medical and test equipment applications.

The core voltage can be set to 2.5 or 3.3 V, while the output voltage can be set to 1.5, 1.8, 2.5 or 3.3 V. The LMK00101 can be easily configured through pin programming.

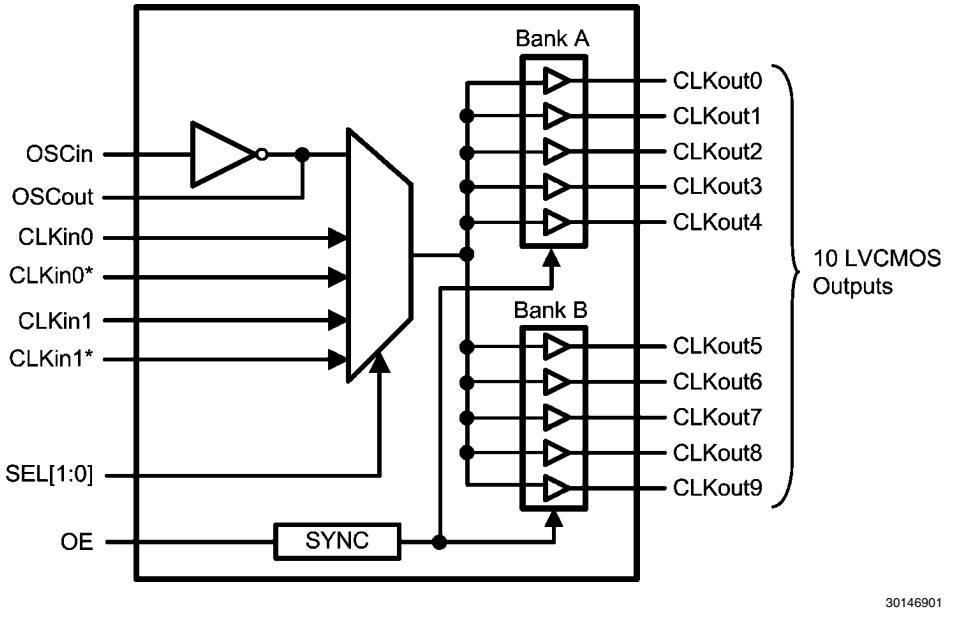
2.0 Target Applications

- LO Reference Distribution for RRU Applications
- SONET, Ethernet, Fibre Channel Line Cards
- Optical Transport Networks
- GPON OLT/ONU
- Server and Storage Area Networking
- Medical Imaging
- Portable Test and Measurement
- High-end A/V

3.0 Features

- 10 LVCMOS/LVTTL Outputs, DC to 200 MHz
- Universal Input
  - LVPECL
  - LVDS
  - HCSL
  - SSTL
  - LVCMOS / LVTTL
- Crystal Oscillator Interface
  - Crystal Input Frequency: 10 to 40 MHz
- Output Skew: 6 ps
- Additive Phase Jitter
  - 30 fs at 156.25 MHz (12 kHz to 20 MHz)
- Low Propagation Delay
- Operates with 3.3 or 2.5 V Core Supply Voltage
- Adjustable Output Power Supply
  - 1.5 V, 1.8 V, 2.5 V, and 3.3 V For Each Bank
- 32 pin LLP Package 5.0 x 5.0 x 0.8 mm

4.0 Functional Block Diagram

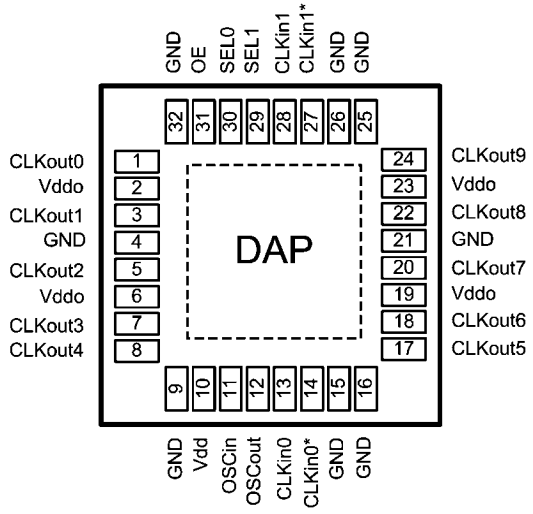


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5.0 Connection Diagram

32-Pin LLP Package



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6.0 Pin Descriptions

Pin #	Pin Name	Type	Description
DAP	DAP	-	The DAP should be grounded
1	CLKout0	Output	LVCMOS Output
2, 6	Vddo	Power	Power Supply for Bank A (CLKout0 to CLKout4) CLKout pins.
19,23	Vddo	Power	Power Supply for Bank B (CLKout5 to CLKout9) CLKout pins.
3	CLKout1	Output	LVCMOS Output
4,9,15,16, 21,25,26,32	GND	GND	Ground
5	CLKout2	Output	LVCMOS Output
7	CLKout3	Output	LVCMOS Output
8	CLKout4	Output	LVCMOS Output
10	Vdd	Power	Supply for operating core and input buffer
11	OSCin	Input	Input for Crystal
12	OSCout	Output	Output for Crystal
13	CLKin0	Input	Input Pin
14	CLKin0*	Input	Optional complimentary input pin
17	CLKout5	Output	LVCMOS Output
18	CLKout6	Output	LVCMOS Output
20	CLKout7	Output	LVCMOS Output
22	CLKout8	Output	LVCMOS Output
24	CLKout9	Output	LVCMOS Output
27	CLKin1*	Input	Optional Complimentary Input Pin
28	CLKin1	Input	Input Pin
29	SEL1	Input	MSB for Input Clock Selection. This pin has an internal pull-down resistor.
30	SEL0	Input	LSB for Input Clock Selection. This pin has an internal pull-down resistor.
31	OE	Input	Output Enable. This pin has an internal pull-down resistor.

7.0 Absolute Maximum Ratings (*Note 1*, *Note 2*)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Core Supply Voltage	Vdd	-0.3 to 3.6	V
Output Supply Voltage	Vddo	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to Vdd + 0.3	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 s)	T_L	+260	°C
Junction Temperature	T_J	+125	°C

8.0 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	-40	25	85	°C
Core Supply Voltage	Vdd	2.375	3.3	3.45	V
Output Supply Voltage (*Note 3*)	Vddo	1.425	3.3	Vdd	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of > 2.5 kV, a MM-ESD of > 250 V, and a CDM-ESD of > 1 kV.

Note 3: V_{ddo} should be less than or equal to V_{dd} ($V_{ddo} \leq V_{dd}$)

9.0 Package Thermal Resistance

32-Lead LLP

Package	Symbols	Ratings	Units
Thermal resistance from junction to ambient on 4-layer Jedec board (*Note 4*)	θ_{JA}	50	° C/W
Thermal resistance from junction to case (*Note 5*)	$\theta_{JC\ (DAP)}$	20	° C/W

Note 4: Specification assumes 5 thermal vias connect to die attach pad to the embedded copper plane on the 4-layer Jedec board. These vias play a key role in improving the thermal performance of the LLP. For best thermal dissipation it is recommended that the maximum number of vias be used on the board layout.

Note 5: Case is defined as the DAP (die attach pad).

10.0 Electrical Characteristics

(2.375 V ≤ Vdd ≤ 3.45 V, 1.425 ≤ Vddo ≤ Vdd, -40 °C ≤ T_A ≤ 85 °C, Differential inputs. Typical values represent most likely parametric norms at Vdd = Vddo = 3.3 V, T_A = 25 °C, at the Recommended Operation Conditions at the time of product characterization and are not guaranteed). Test conditions are: F_{test} = 100 MHz, Load = 5 pF in parallel with 50 Ω unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Total Device Characteristics						
Vdd	Core Supply Voltage		2.375	2.5 or 3.3	3.45	V
Vddo	Output Supply Voltage		1.425	1.5,1.8, 2.5, or 3.3	Vdd	V
I_{Vdd}	Core Current	No CLKin		16	25	mA
		V_{ddo} = 3.3 V, F_{test} = 100 MHz		24		
		V_{ddo} = 2.5 V, F_{test} = 100 MHz		20		
$I_{Vddo[n]}$	Current for Each Output	V_{ddo} = 2.5 V, OE = High, F_{test} = 100 MHz		5		mA
		V_{ddo}= 3.3 V, OE = High, F_{test} = 100 MHz		7		
		OE = Low		0.1		
I_{Vdd} + I_{Vddo}	Total Device Current with Loads on all outputs	OE = High @ 100 MHz		95		mA
		OE = Low		16		
Power Supply Ripple Rejection (PSRR)						
PSRR	Ripple Induced Phase Spur Level	100 kHz, 100 mVpp Ripple Injected on V_{dd}, V_{ddo} = 2.5 V		-44		dBc
Outputs (*Note 6*)						
Skew	Output Skew	Measured between outputs, referenced to CLKout0		6		ps
f_{CLKout}	Output Frequency (*Note 7*)		DC		200	MHz
t_{Rise}	Rise/Fall Time	V_{dd} = 3.3 V, V_{ddo} = 1.8 V, C_L = 10 pF		500		ps
		V_{dd} = 2.5 V, V_{ddo} = 2.5 V, C_L = 10 pF		300		
		V_{dd} = 3.3 V, V_{ddo} = 3.3 V, C_L = 10 pF		200		
V_{CLKout}Low	Output Low Voltage				0.1	V
V_{CLKout}High	Output High Voltage		Vddo-0.1			
R_{CLKout}	Output Resistance			50		ohm
t_j	RMS Additive Jitter	f_{CLKout} = 156.25 MHz, CMOS input slew rate ≥ 2 V/ns C_L = 5 pF, BW = 12 kHz to 20 MHz		30		fs

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Digital Inputs (OE, SEL0, SEL1)						
V_{Low}	Input Low Voltage	Vdd = 2.5 V			0.4	V
V_{High}	Input High Voltage	Vdd = 2.5 V	1.3			V
		Vdd = 3.3 V	1.6			
I_{IH}	High Level Input Current				50	uA
I_{IL}	Low Level Input Current		-5		5	uA
CLKin0/0* and CLKin1/1* Input Clock Specifications, (*Note 9*, *Note 10*)						
I_{IH}	High Level Input Current	V_{CLKin} = Vdd			20	uA
I_{IL}	Low Level Input Current (*Note 8*)	V_{CLKin} = 0 V	-20			uA
V_{IH}	Input High Voltage				Vdd	V
V_{IL}	Input Low Voltage		GND			V
V_{CM}	Differential Input Common Mode Input Voltage (*Note 12*)	V_{ID} = 150 mV	0.5		Vdd-1.2	V
		V_{ID} = 350 mV	0.5		Vdd-1.1	
		V_{ID} = 800 mV	0.5		Vdd-0.9	
V_{ID}	Differential Input Voltage Swing	CLKin driven differentially	0.15		1.5	V
OSCin/OSCout Pins						
f_{OSCin}	Input Frequency (*Note 7*)	Single-Ended Input, OSCout floating	DC		200	MHz
f_{XTAL}	Crystal Frequency Input Range	Fundamental Mode Crystal ESR < 200 Ω ($f_{Xtal} \leq$ 30 MHz) ESR < 120 Ω (f_{Xtal} > 30 MHz) (*Note 11*, *Note 7*)	10		40	MHz
C_{OSCin}	Shunt Capacitance			1		pF

Note 6: AC Parameters for CMOS are dependent upon output capacitive loading

Note 7: Guaranteed by characterization.

Note 8: V_{IL} should not go below -0.3 volts.

Note 9: See *Section 12.1 Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD}.

Note 10: Refer to application note AN-912 Common Data Transmission Parameters and their Definitions for more information.

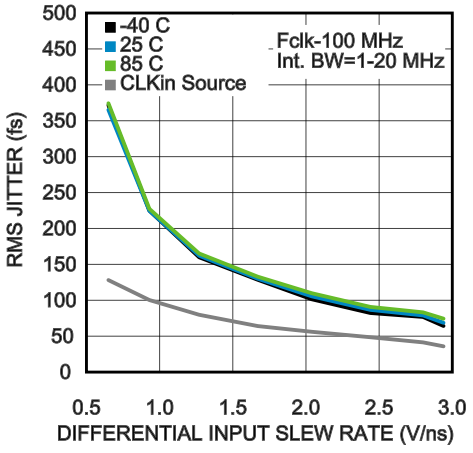
Note 11: The ESR requirements stated are what is necessary in order to ensure that the Oscillator circuitry has no start up issues. However, lower ESR values for the crystal might be necessary in order to stay below the maximum power dissipation requirements for that crystal.

Note 12: When using differential signals with V_{CM} outside of the acceptable range for the specified V_{ID}, the clock must be AC coupled.

11.0 Typical Performance Characteristics

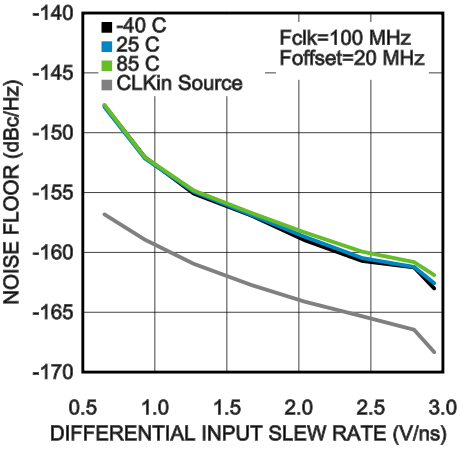
Unless otherwise specified: $V_{dd} = V_{ddo} = 3.3$ V, $T_A = 20$ °C, $C_L = 5$ pF, CLKin driven differentially, input slew rate ≥ 2 V/ns.

RMS Jitter vs. CLKin Slew Rate @ 100 MHz



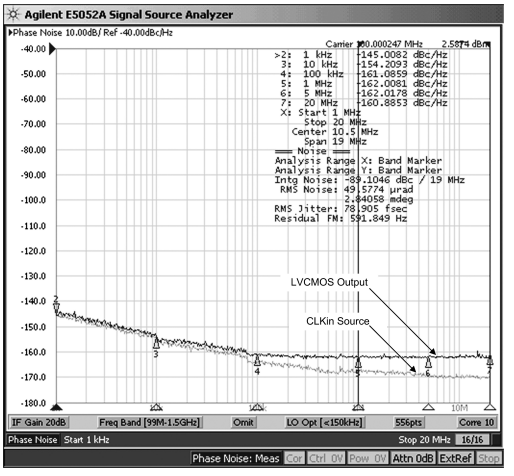
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Noise Floor vs. CLKin Slew Rate @ 100 MHz



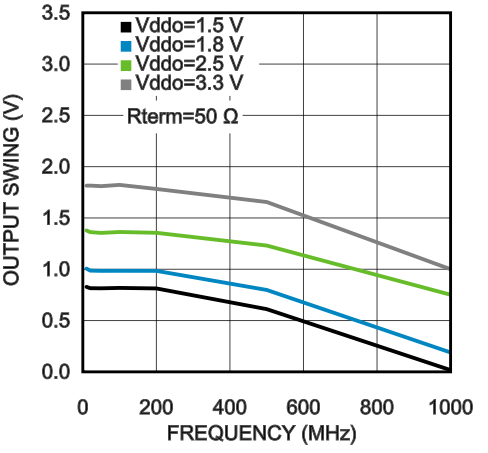
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LVCMOS Phase Noise @ 100 MHz (*Note 13*)



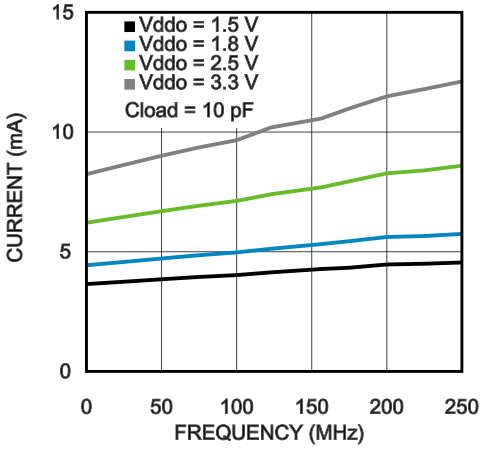
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LVCMOS Output Swing vs. Frequency



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Iddo per Output vs Frequency



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Note 13: Test conditions: LVCMOS Input, slew rate ≥ 2 V/ns, C_L = 5 pF in parallel with 50 Ω, BW = 1 MHz to 20 MHz.

12.0 Measurement Definitions

12.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first section

Figure 1 illustrates the two different definitions side-by-side for inputs and *Figure 2* illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined in volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

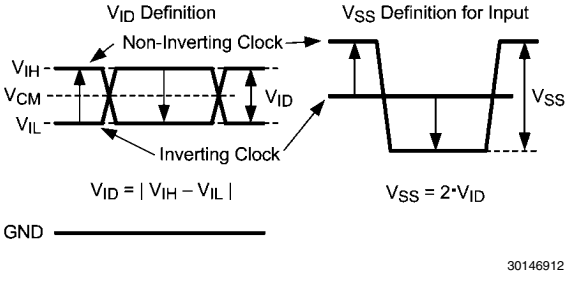


FIGURE 1. Two Different Definitions for Differential Input Signals

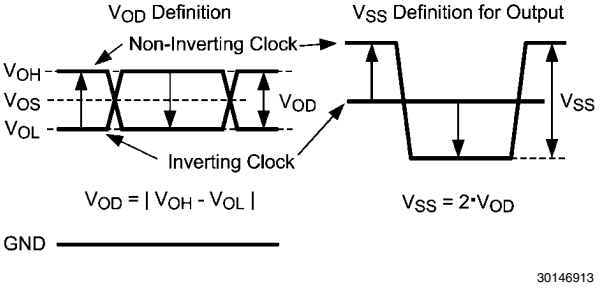


FIGURE 2. Two Different Definitions for Differential Output Signals

13.0 Functional Description

The LMK00101 is a 10 output LVCMOS clock fanout buffer with low additive jitter that can operate up to 200 MHz. It features a 3:1 input multiplexer with a crystal oscillator input, single supply or dual supply (lower power) operation, and pin-programmable device configuration. The device is offered in a 32-pin LLP package.

13.1 V_{dd} and V_{ddo} Power Supplies (*Note 14*, *Note 15*)

Separate core and output supplies allow the output buffers to operate at the same supply as the Vdd core supply (3.3 V or 2.5 V) or from a lower supply voltage (3.3 V, 2.5 V, 1.8 V, or 1.5 V). Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

Bank A (CLKout0 to CLKout4) and Bank B (CLKout5 to CLKout9) may also be operated at different V_{ddo} voltages, provided neither V_{ddo} voltage exceeds V_{dd}.

Note 14: Care should be taken to ensure the V_{ddo} voltage does not exceed the Vdd voltage to prevent turning-on the internal ESD protection circuitry.

Note 15: DO NOT DISCONNECT OR GROUND ANY OF THE V_{ddo} PINS as the V_{ddo} pins are internally connected within an output bank.

13.2 CLOCK INPUTS

The LMK00101 has three different inputs, CLKin0/CLKin0*, CLKin1/CLKin1*, and OSCin that can be driven in different manners that are described in the following sections.

13.2.1 SELECTION OF CLOCK INPUT

Clock input selection is controlled using the SEL0 and SEL1 pins as shown in *Table 1*. Refer to *Section 14.1 Driving the Clock Inputs* for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator will start-up and its clock will be distributed to all outputs. Refer to *Section 14.2 Crystal Interface* for more information. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal.

TABLE 1. Input Selection

SEL1	SEL0	Input
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin (Crystal Mode)

13.2.1.1 CLKin/CLKin* Pins

The LMK00101 has two differential inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can be driven single-ended or differentially. They can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, or other differential and singled ended signals that meet the input requirements under the “CLKin0/0* and CLKin1/1* Input Clock Specifications” portion of the *Section 10.0 Electrical Characteristics* and (*Note 12*). Refer to *Section 14.1 Driving the Clock Inputs* for more details on driving the LMK00101 inputs.

In the event that a Crystal mode is not selected and the CLKin pins do not have an AC signal applied to them, *Table 2* following will be the state of the outputs.

TABLE 2. CLKinX Input vs. Output States

CLKinX	CLKinX*	Output State
Open	Open	Logic Low
Logic Low	Logic Low	Logic Low
Logic High	Logic Low	Logic High
Logic Low	Logic High	Logic Low

13.3 CLOCK OUTPUTS

The LMK00101 has 10 LVCMOS outputs.

13.3.1 Output Enable Pin

When the output enable pin is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state as shown in *Table 3*.

TABLE 3. Output Enable Pin States

OE	Outputs
Low	Disabled (Hi-Z)
High	Enabled

The OE pin is synchronized to the input clock to ensure that there are no runt pulses. When OE is changed from Low to High, the outputs will initially have an impedance of about 400 Ω to ground until the second falling edge of the input clock. Starting with the second falling edge of the input clock, the outputs will buffer the input. If the OE pin is taken from Low to High when there is no input clock present, the outputs will either go High or Low and stay a that state; they will not oscillate. When the OE pin is taken from High to Low the outputs will become Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

13.3.2 Using Less than Ten Outputs

Although the LMK00101 has 10 outputs, not all applications will require all of these. In this case, the unused outputs should be left floating with a minimum copper length (*Note 16*) to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

Note 16: For best soldering practices, the minimum trace length should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

14.0 Application Information

14.1 Driving the Clock Inputs

The LMK00101 has two differential inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, and other differential and single ended signals that meet the input requirements specified in *Section 10.0 Electrical Characteristics*. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID})/dynamic range. AC coupling may also be employed to shift the input signal to within the V_{CM} range.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have a high slew rate of 2 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

While it is recommended to drive CLKin0 and CLKin1 with a differential signal input, it is possible to drive them with a single ended clock. The single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKinX input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in *Figure 3*, *Figure 4*, or *Figure 5* depending upon the application.

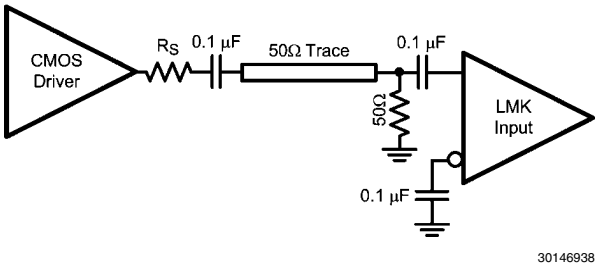


FIGURE 3. Single-Ended LVCMOS Input, AC Coupling, Near and Far End Termination

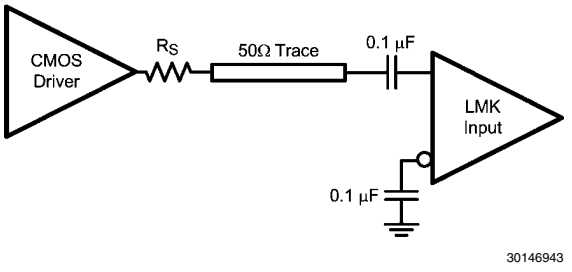


FIGURE 4. Single-Ended LVCMOS Input, AC Coupling, Near End Termination

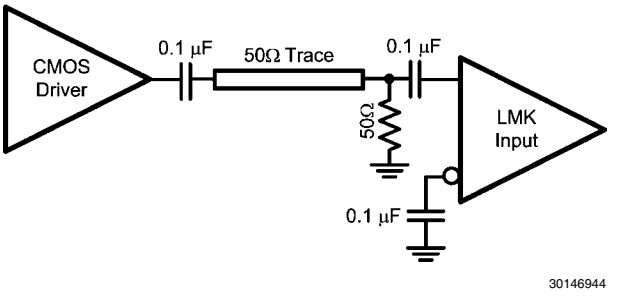


FIGURE 5. Single-Ended LVCMOS Input, AC Coupling, Far End Termination

A single ended clock may also be DC coupled to CLKinX as shown in *Figure 6*. If the DC coupled input swing has a common mode level near the devices internal bias of 1.4 V, then only a 0.1 µF bypass cap is required on CLKinX*. Otherwise, if the input swing is not optimally centered near the internal bias voltage, then CLKinX* should be externally biased to the midpoint voltage of the input swing. This can be achieved using external biasing resistors, R_{B1} and R_{B2}, or another low-noise voltage reference. The external bias voltage should be within the specified input common voltage (VCM) range. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

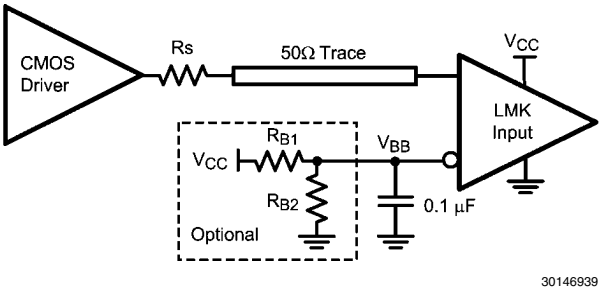


FIGURE 6. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in *Figure 7*. Configurations similar to *Figure 4* or *Figure 5* could also be used as long as the OSCout pin is left floating. The input clock should be AC coupled to the OSCin pin, which has an internally generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLKinX) since it offers higher operating frequency, better common mode, improved power supply noise rejection, and greater performance over supply voltage and temperature variations.

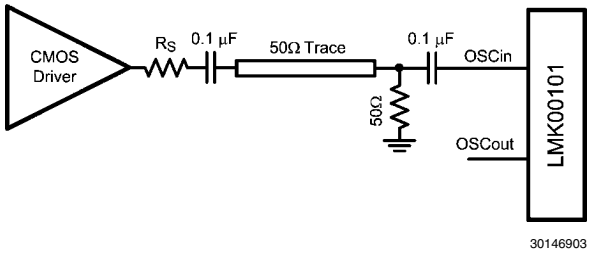


FIGURE 7. Driving OSCin with a Single-Ended External Clock

14.2 Crystal Interface

The LMK00101 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in *Figure 8*.

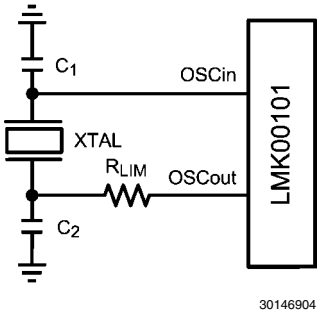


FIGURE 8. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 to 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 1 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1 to 3 pF) can affect the discrete load capacitor values, C_1 and C_2. For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so *Equation 1* can be rewritten in terms of C_1only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY}) * 2 \quad (3)$$

Section 10.0 Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR} * (1 + C_0 / C_L)^2 \quad (4)$$

Where:

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the maximum equivalent series resistance specified for the crystal.
- C_L is the load capacitance specified for the crystal.
- C_0 is the minimum shunt capacitance specified for the crystal.

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in *Figure 8*, an external resistor, R_{LIM}, can be used to limit the crystal drive level if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ

14.3 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00101, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00101, power supply ripple rejection (PSRR), was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the V_{ddo} supply. The PSRR test setup is shown in *Figure 9*.

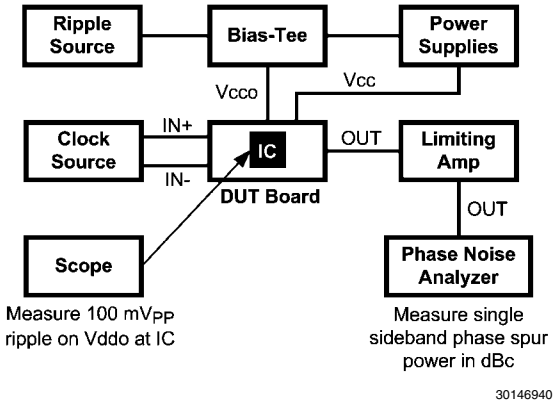


FIGURE 9. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the V_{ddo} supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the V_{ddo} pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 100 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on V_{ddo} = 2.5 V
- Ripple frequency: 100 kHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ\ (ps\ pk\text{-}pk) = [(2 * 10^{(PSRR/20)}) / (\pi * f_{clk})] * 10^{12} \quad (5)$$

14.4 Power Supply Bypassing

The V_{dd} and V_{ddo} power supplies should have a high frequency bypass capacitor, such as 100 pF, placed very close to each supply pin. Placing the bypass capacitors on the same layer as the LMK00101 improves input sensitivity and performance. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

14.5 Thermal Management

For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in *Figure 10*. More information on soldering LLP packages and gerber footprints can be obtained: http://www.national.com/en/packaging/index.html.

A recommended footprint including recommended solder mask and solder paste layers can be found at: http://www.national.com/en/packaging/gerber.html for the SQA32A package.

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in *Figure 10* should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

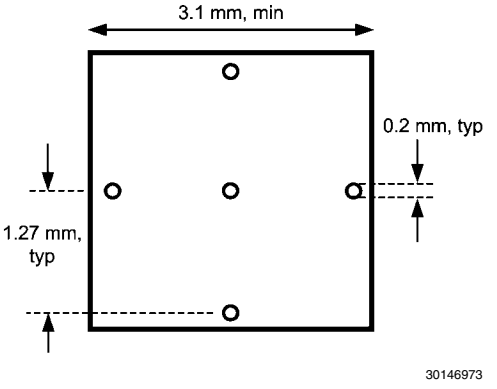
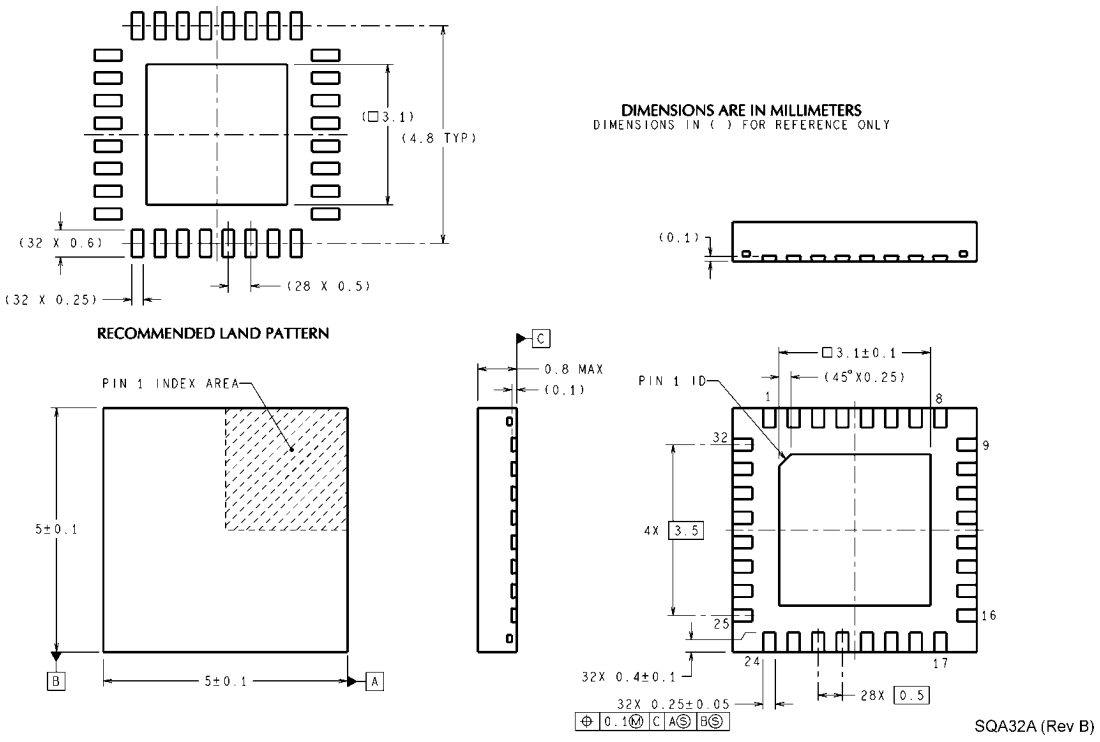


FIGURE 10. Recommended Land and Via Pattern

15.0 Physical Dimensions inches (millimeters) unless otherwise noted



Leadless Leadframe Package (Bottom View)
32 Pin LLP Package

16.0 Ordering Information

Order Number	Package Marking	Packaging
LMK00101SQX	K00101	2500 Unit Tape and Reel
LMK00101SQ		1000 Unit Tape and Reel
LMK00101SQE		250 Unit Tape and Reel

Notes

Notes

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