16-Bit, 10 MSPS, PulSAR Differential ADC

AD7626

FEATURES

Throughput: 10 MSPS
SNR: 91.5 dB
16-bit no missing codes
INL: ±0.45 LSB
DNL: ±0.35 LSB
Power dissipation: 136mW
32-lead LFCSP (5 mm × 5 mm)
SAR architecture
- **No latency/no pipeline delay**

16-bit resolution with no missing codes
Zero error: ±1LSB
Differential input range: ±4.096 V
Serial LVDS interface
- **Self-clocked mode**
- **Echoed-clock mode**
- **LVDS or CMOS option for conversion control (CNV signal)**

Reference options
- **Internal: 4.096 V**
- **External (1.2 V) buffered to 4.096 V**
- **External: 4.096 V**

APPLICATIONS

Digital imaging systems
- **Digital X-ray**
- **Digital MRI**
- **CCD and IR cameras**

High speed data acquisition
High dynamic range telecommunications receivers
Spectrum analysis
Test equipment

FUNCTIONAL BLOCK DIAGRAM

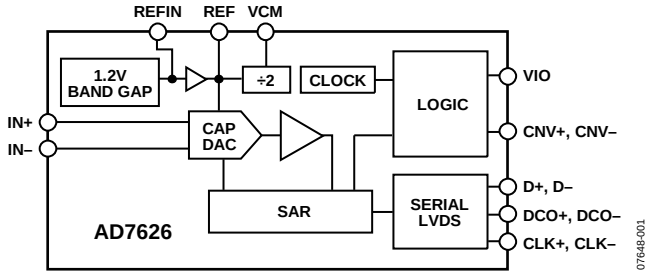


Figure 1.

GENERAL DESCRIPTION

The AD7626 is a 16-bit, 10 MSPS, charge redistribution successive approximation register (SAR) based architecture analog-to-digital converter (ADC). SAR architecture allows unmatched performance both in noise (91.5 dB SNR) and in linearity (±0.45 LSB INL). The AD7626 contains a high speed, 16-bit sampling ADC, an internal conversion clock, and an internal buffered reference. On the CNV edge, it samples the voltage difference between the IN+ and IN− pins. The voltages on these pins swing in opposite phase between 0 V and REF. The 4.096 V reference voltage, REF, can be generated internally or applied externally.

All converted results are available on a single LVDS self-clocked or echoed-clock serial interface, reducing external hardware connections.

The AD7626 is housed in a 32-lead, 5 mm × 5 mm LFCSP with operation specified from −40°C to +85°C.

Table 1. Fast PulSAR® ADC Selection

Input Type	Resolution (Bits)	1 MSPS to <2 MSPS	2 MSPS to 3 MSPS	6 MSPS	10 MSPS
Differential (Ground Sense)	16	AD7653 AD7667 AD7980 AD7983			
True Bipolar	16	AD7671			
Differential (Antiphase)	16	AD7677 AD7623	AD7621 AD7622	AD7625	AD7626
Differential (Antiphase)	18	AD7643 AD7982 AD7984	AD7641		

Rev. A
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REVISION HISTORY

1/10—Rev. 0 to Rev. A

Changes to Description of Pin 5 and Pin 6, Table 6 ... 8
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9/09—Revision 0: Initial Version

SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.5 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range		$V_{REF}/2 - 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V
CMRR	f_{IN} = 1 MHz		68		dB
Input Current	Midscale input		168		µA
THROUGHPUT					
Complete Cycle				100	ns
Throughput Rate		0.1		10	MSPS
DC ACCURACY					
Integral Linearity Error		−1.5	±0.45	+1.5	LSB
No Missing Codes		16			Bits
Differential Linearity Error		−0.5	±0.35	+0.5	LSB
Transition Noise			0.6		LSB
Zero Error, T_{MIN} to T_{MAX}		−6	±1	+6	LSB
Zero Error Drift			0.5		ppm/°C
Gain Error, T_{MIN} to T_{MAX}			8	20	LSB
Gain Error Drift			0.7		ppm/°C
Power Supply Sensitivity[1]	VDD1 = 5 V ± 5%		0.4		LSB
	VDD2 = 2.5 V ± 5%		0.2		LSB
AC ACCURACY					
f_{IN} = 20 kHz, −0.5 dBFS					
Dynamic Range		90.5	91.5		dB
Signal-to-Noise Ratio		90	91		dB
Spurious-Free Dynamic Range			105		dB
Total Harmonic Distortion			−105.5		dB
Signal-to-(Noise + Distortion)		89.5	91		dB
f_{IN} = 100 kHz, −0.5 dBFS					
Signal-to-Noise Ratio			91.3		dB
Spurious-Free Dynamic Range			104.5		dB
Total Harmonic Distortion			−102.5		dB
Signal-to-(Noise + Distortion)			91		dB
f_{IN} = 2.4 MHz, −1 dBFS					
Signal-to-Noise Ratio			88.5		dBFS
Spurious-Free Dynamic Range			84		dB
Total Harmonic Distortion			−86		dB
Signal-to-(Noise + Distortion)			85		dB
f_{IN} = 2.4 MHz, −6 dBFS					
Signal-to-Noise Ratio			89		dBFS
Spurious-Free Dynamic Range			84		dB
Total Harmonic Distortion			−93		dB
Signal-to-(Noise + Distortion)			88		dB
−3 dB Input Bandwidth			95		MHz
Aperture Jitter			0.25		ps rms
INTERNAL REFERENCE					
Output Voltage	REFIN @ 25°C	1.18	1.19	1.2	V
Temperature Drift	−40°C to +85°C		±15		ppm/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE BUFFER					
REFIN Input Voltage Range		1.18	1.2	1.22	V
REF Output Voltage Range	REF @ 25°C, EN0 = EN1 = 1	4.076	4.096	4.116	V
Line Regulation	VDD1 ± 5%, VDD2 ± 5%		5		mV
EXTERNAL REFERENCE					
Voltage Range	REF		4.096		V
VCM PIN					
VCM Output			REF/2		
VCM Error		−0.015		+0.015	V
Output Impedance			5		kΩ
LVDS I/O (ANSI-644)					
Data Format			Serial LVDS twos complement		
Differential Output Voltage, V_{OD}	R_L = 100 Ω	245	290	454	mV
Common-Mode Output Voltage, V_{OCM}	R_L = 100 Ω	980[2]	1130	1375	mV
Differential Input Voltage, V_{ID}		100		650	mV
Common-Mode Input Voltage, V_{ICM}		800		1575	mV
POWER SUPPLIES					
Specified Performance					
VDD1		4.75	5	5.25	V
VDD2		2.37	2.5	2.63	V
VIO		2.37	2.5	2.63	V
Operating Currents					
Static—Not Converting					
VDD1			3.5	4.5	mA
VDD2			16.7	21.2	mA
VIO			11.6	13.5	mA
With Internal Reference	10 MSPS throughput				
VDD1			10.4	11.2	mA
VDD2			23.5	27.8	mA
VIO	Echoed-clock mode		15.8	17.8	mA
With External Reference	10 MSPS throughput				
VDD1			7.5	8.8	mA
VDD2			23	28	mA
VIO	Echoed-clock mode		16.4	18.5	mA
Power-Down	EN0 = 0, EN1 = 0				
VDD1			0.6	4	µA
VDD2			0.8	10	µA
VIO			1	5	µA
Power Dissipation[3]					
Static—Not Converting			88	107	mW
With Internal Reference	10 MSPS throughput		150	170	mW
With External Reference	10 MSPS throughput		136	160	mW
Power-Down			8	58	µW
Energy per Conversion	10 MSPS throughput		13.6		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] Using an external reference.
[2] The ANSI-644 LVDS specification has a minimum output common mode (V_{OCM}) of 1125 mV.
[3] Power dissipation is for the AD7626 device only. In self-clocked interface mode, 0.9 mW is dissipated in the 100 Ω terminator. In echoed-clock interface mode, 1.8 mW is dissipated in two 100 Ω terminators.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.37 V to 2.63 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions[1]	t_{CYC}	100		10,000	ns
CNV High Time	t_{CNVH}	10		40	ns
CNV to D (MSB) Ready	t_{MSB}			100	ns
CNV to Last CLK (LSB) Delay	t_{CLKL}			72	ns
CLK Period[2]	t_{CLK}	3.33	4	$(t_{CYC} - t_{MSB} + t_{CLKL})/n$	ns
CLK Frequency	f_{CLK}		250	300	MHz
CLK to DCO Delay (Echoed-Clock Mode)	t_{DCO}	0	4	7	ns
DCO to D Delay (Echoed-Clock Mode)	t_D		0	1	ns
CLK to D Delay	t_{CLKD}	0	4	7	ns

[1] The maximum time between conversions is 10,000 ns. If CNV± is left idle for a time greater than the maximum value of t_{CYC}, the subsequent conversion result is invalid.
[2] For the maximum CLK period, the window available to read data is $t_{CYC} - t_{MSB} + t_{CLKL}$. Divide this time by the number of bits (n) to be read giving the maximum CLK± frequency that can be used for a given conversion CNV frequency. In echoed-clock interface mode, n = 16; in self-clocked interface mode, n = 18.

TIMING DIAGRAMS

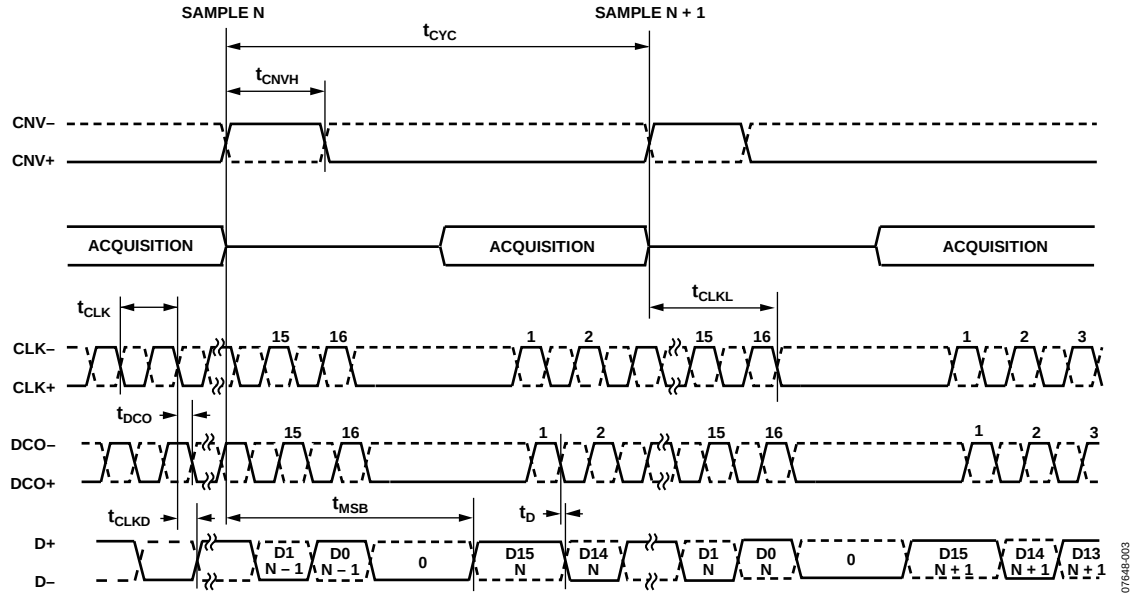


Figure 2. Echoed-Clock Interface Mode Timing Diagram

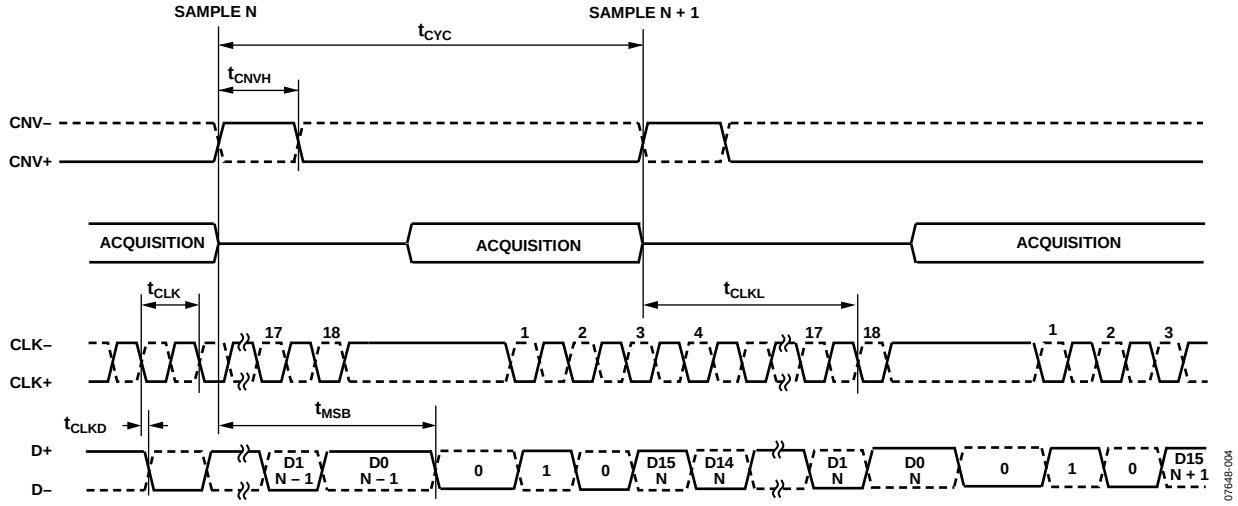


Figure 3. Self-Clocked Interface Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN– to GND[1]	–0.3 V to REF + 0.3 V or ±130 mA
REF[2] to GND	–0.3 V to +6 V
VCM, CAP2 to GND	–0.3 V to +6 V
CAP1, REFIN to GND	–0.3 V to +2.7 V
Supply Voltage	
VDD1	–0.3 V to +6 V
VDD2, VIO	–0.3 V to +3 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Input Current to Any Pin Except Supplies[3]	±10 mA
Operating Temperature Range (Commercial)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
ESD	1 kV

[1] See the Analog Inputs section.
[2] Keep CNV± low for any external REF voltage > 4.3 V applied to the REF pin.
[3] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_VQ	40	4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

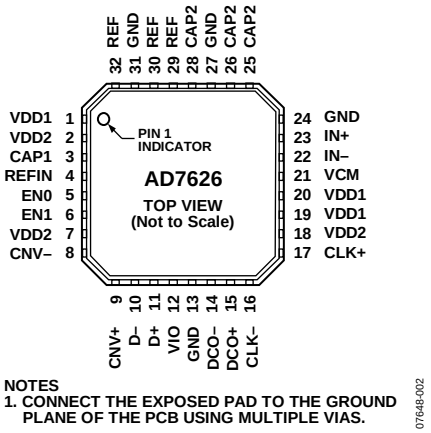


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VDD1	P	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
2	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor. The 2.5 V supply source should supply this pin first, then be traced to the other VDD2 pins (Pin 7 and Pin 18).
3	CAP1	AO	Connect this pin to a 10 nF capacitor.
4	REFIN	AI/O	Prebuffer Reference Voltage. When using the internal reference, this pin outputs the band gap voltage and is nominally at 1.2 V. It can be overdriven with an external reference voltage such as the ADR280. In either internal or external reference mode, a 10 µF capacitor is required. If using an external 4.096 V reference (connected to REF), this pin is a no connect and does not require any capacitor.
5, 6	EN0, EN1	DI	Enable. Operates from 2.5 V logic. The logic levels of these pins set the operation of the device as follows: EN1 = 0, EN0 = 0: power-down mode. EN1 = 0, EN0 = 1: external 1.2 V reference applied to the REFIN pin required. EN1 = 1, EN0 = 0: external 4.096 V reference applied to the REF pin required. EN1 = 1, EN0 = 1: internal reference and internal reference buffer in use.
7	VDD2	P	Digital 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
8, 9	CNV–, CNV+	DI	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV– is grounded; otherwise, CNV+ and CNV– are differential LVDS inputs.
10, 11	D–, D+	DO	LVDS Data Outputs. The conversion data is output serially on these pins.
12	VIO	P	Input/Output Interface Supply. Use a 2.5 V supply and decouple this pin with a 100 nF capacitor.
13	GND	P	Ground. Return path for the 100 nF capacitor connected to Pin 12.
14, 15	DCO–, DCO+	DO	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self-clocked interface mode is selected. In this mode, the 16-bit results on D are preceded by an initial 0 (which is output at the end of the previous conversion), followed by a 2-bit header (10) to allow synchronization of the data by the digital host with extra logic. The 1 in this header provides the reference to acquire the subsequent conversion result correctly. When DCO+ is not grounded, the echoed-clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be captured in the digital host on the next rising edge of DCO+.
16, 17	CLK–, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
18	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
19, 20	VDD1	P	Analog 5 V Supply. Isolate these pins from Pin 1 with a ferrite bead and decouple them with a 100 nF capacitor.
21	VCM	AO	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
22	IN–	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.

Pin No.	Mnemonic	Type[1]	Description
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN−.
24	GND	P	Ground.
25, 26, 28	CAP2	AO	Connect all three CAP2 pins together and decouple them with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 27 (GND).
27	GND	P	Ground. Return path for the 10 µF capacitor connected to Pin 25, Pin 26, and Pin 28.
29, 30, 32	REF	AI/O	Buffered Reference Voltage. When using the internal reference or the 1.2 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference, such as the ADR434 or the ADR444, the internal reference buffer must be disabled. In either case, connect all three REF pins together and decouple them with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 31 (GND).
31	GND	P	Ground. Return path for the 10 µF capacitor connected to Pin 29, Pin 30, and Pin 32.
EP	Exposed pad		The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias. See the Exposed Paddle section for more information.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.5 V; REF = 4.096 V; all plots at 10 MSPS unless otherwise noted. FFT plots for 2 MHz, 3 MHz, and 5 MHz input tones use band pass filter (±400 kHz pass bandwidth around fundamental frequency).

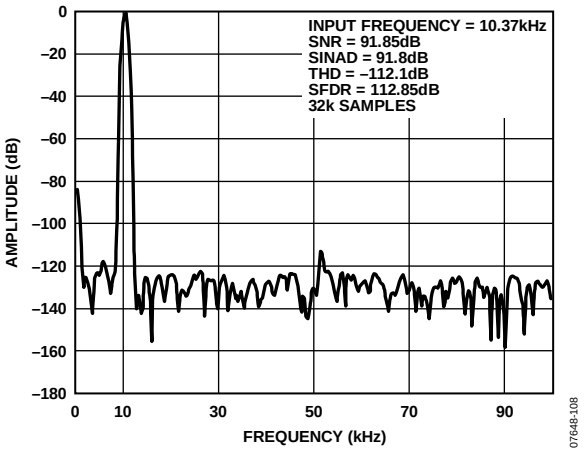


Figure 5. 10 kHz, –0.5 dB Input Tone, Zoomed View

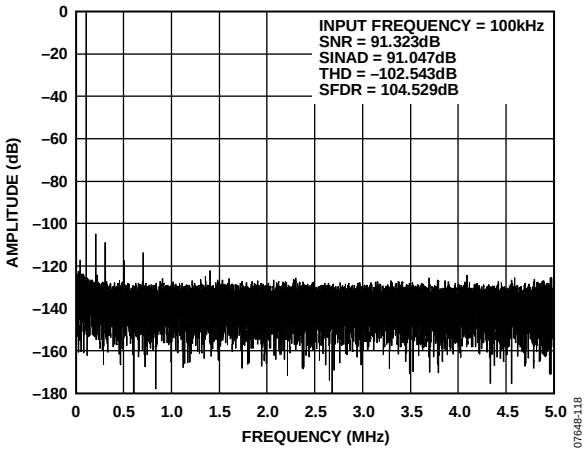


Figure 8.100 kHz, –0.5 dB Input Tone FFT, Full Frequency View

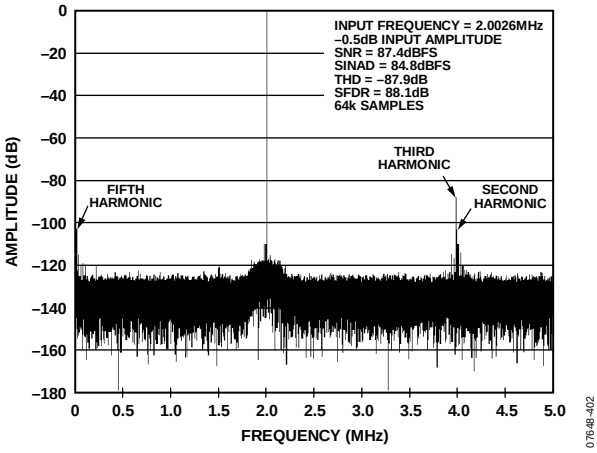


Figure 6. FFT, 2 MHz, –0.5 dB Input Tone, Wide View

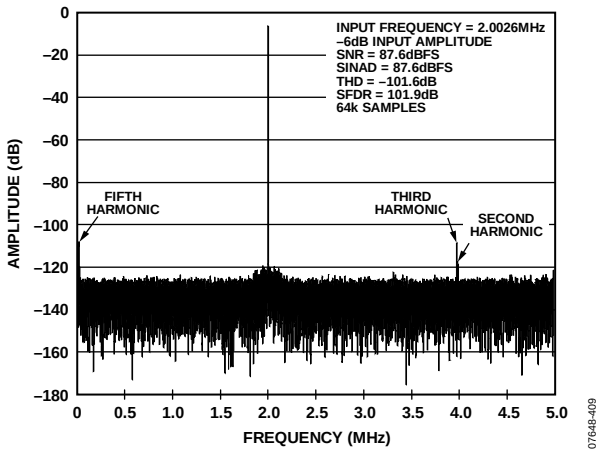


Figure 9. FFT, 2 MHz, –6 dB Input Tone, Wide View

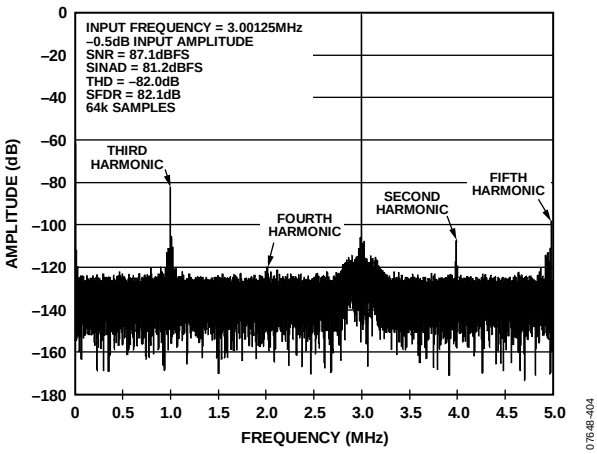


Figure 7. FFT, 3 MHz, –0.5 dB Input Tone, Wide View

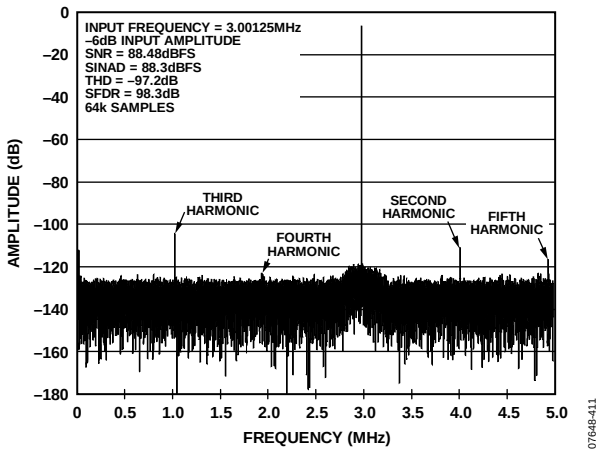


Figure 10. FFT, 3 MHz, –6 dB Input Tone, Wide View

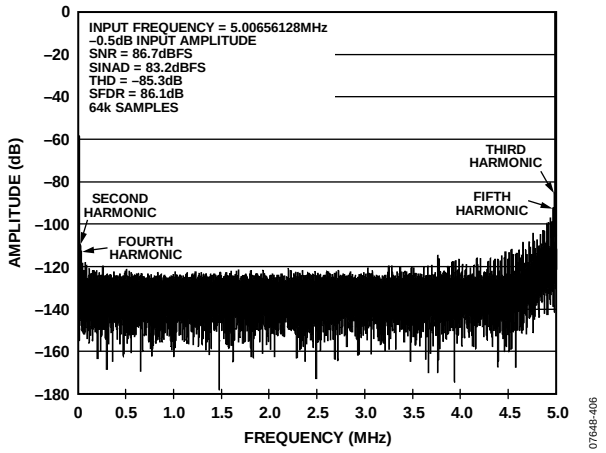


Figure 11. FFT, 5 MHz, –0.5 dB Input Tone, Wide View

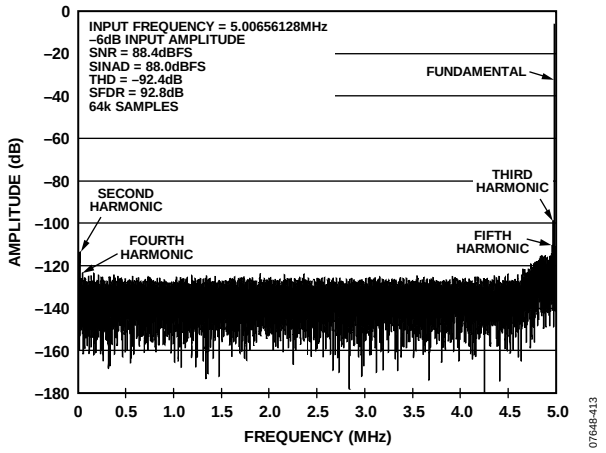


Figure 12. FFT, 5 MHz, –6 dB Input Tone, Wide View

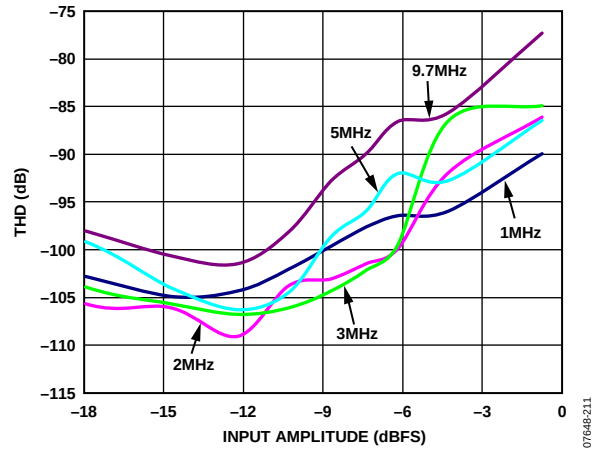


Figure 13. THD vs. Input Amplitudes at Input Frequency Tones of 10 kHz to 9.7 MHz

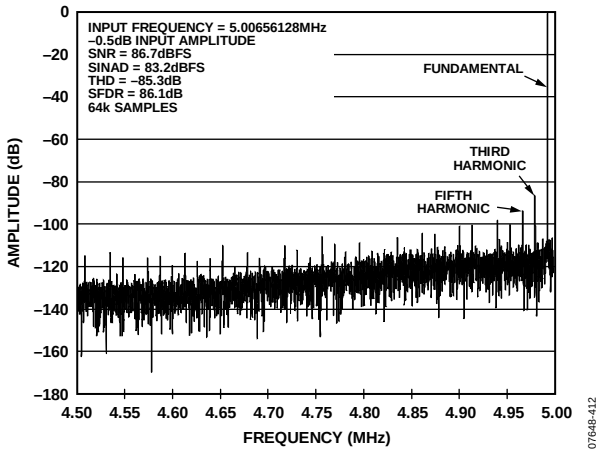


Figure 14. FFT, 5 MHz, –0.5 dB Input Tone Zoomed View

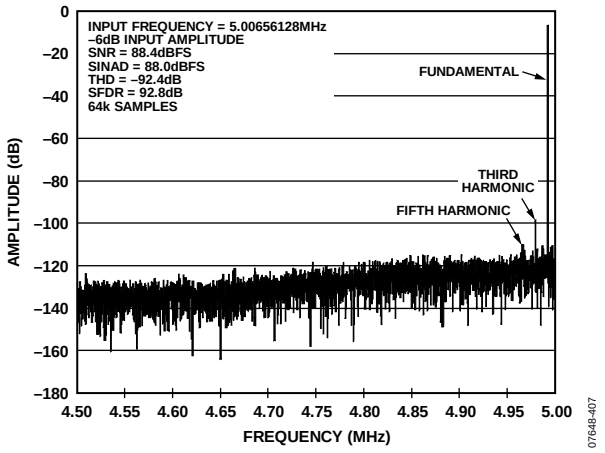


Figure 15. FFT, 5 MHz, –0.5 dB Input Tone Zoomed View

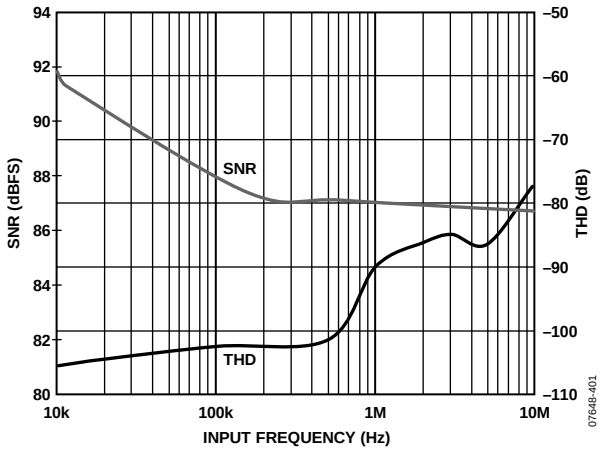


Figure 16. THD and SNR vs. Input Frequency (–0.5 dB Input Tone)

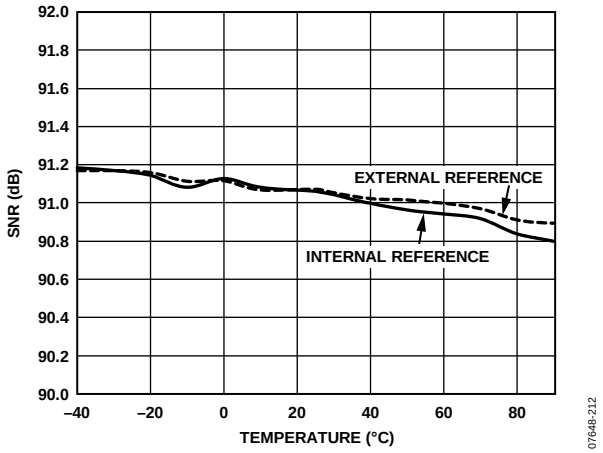


Figure 17. SNR vs. Temperature (−0.5 dB, 20 kHz Input Tone)

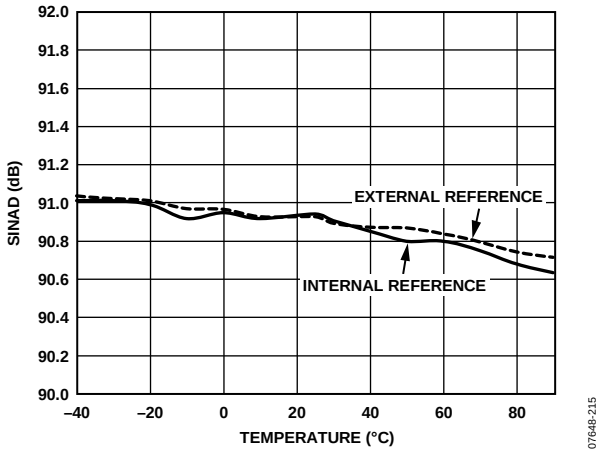


Figure 20. SINAD vs. Temperature (−0.5 dB, 20 kHz Input Tone)

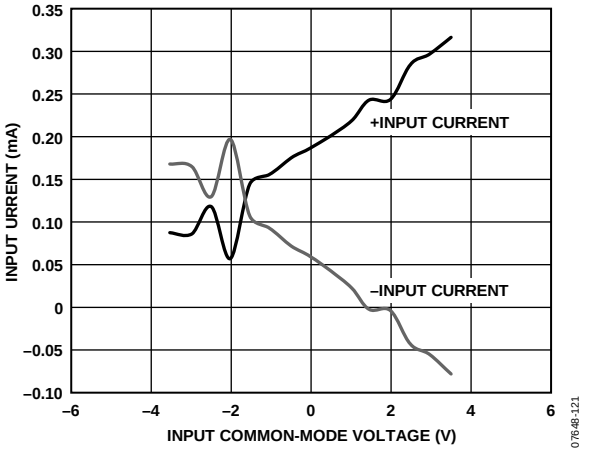


Figure 18. Input Current (IN+, IN−) vs. Differential Input Voltage (10 MSPS)

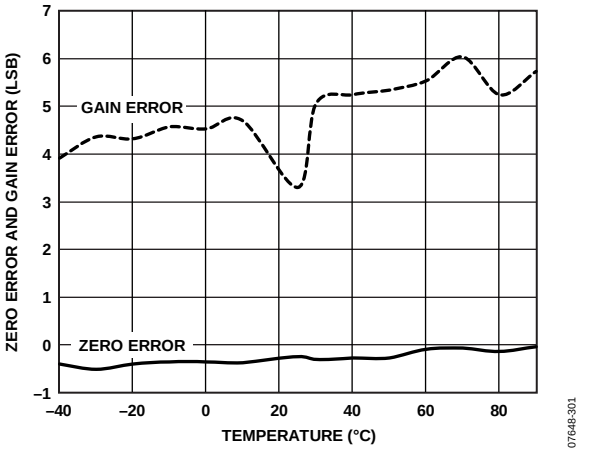


Figure 21. Zero Error and Gain Error vs. Temperature

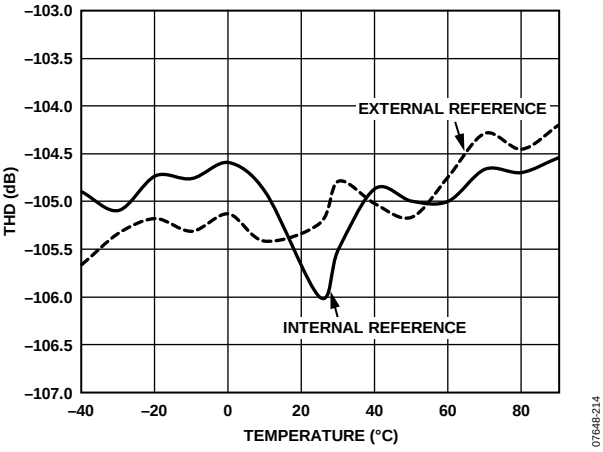


Figure 19. THD vs. Temperature (−0.5 dB, 20 kHz Input Tone)

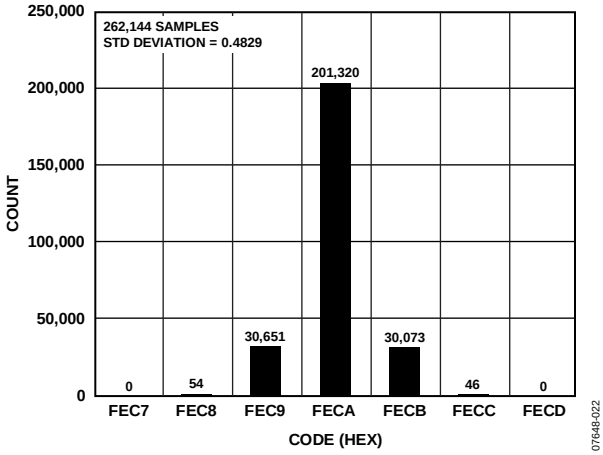


Figure 22. Histogram of 262,144 Conversions of a DC Input at the Code Center (Internal Reference)

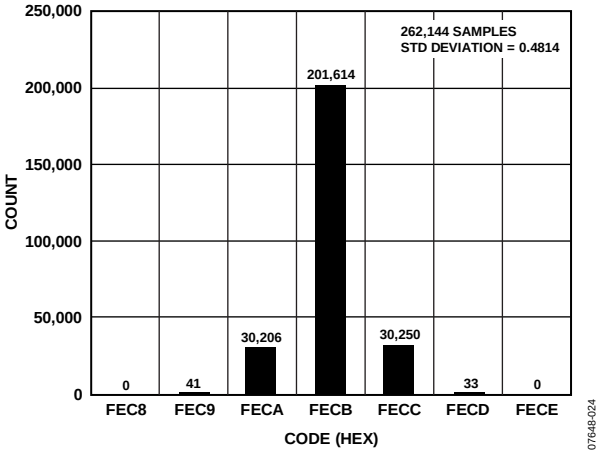


Figure 23. Histogram of 262,144 Conversions of a DC Input at the Code Center (External Reference)

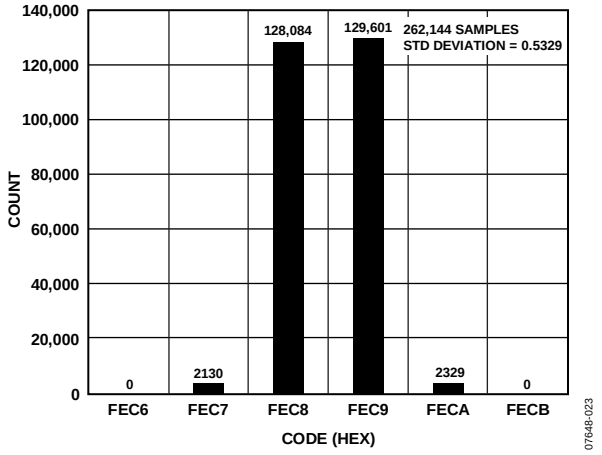


Figure 24. Histogram of 262,144 Conversions of a DC Input at the Code Transition

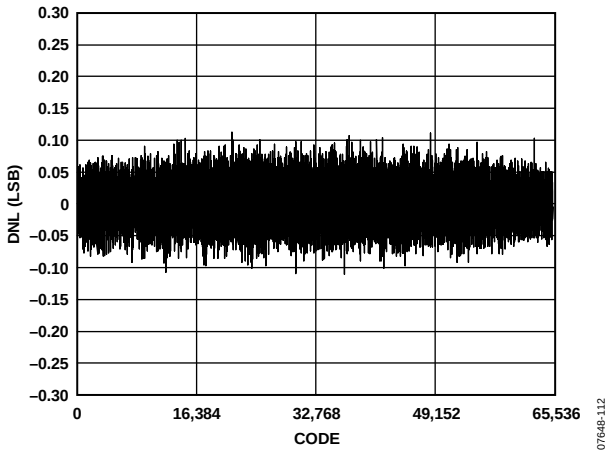


Figure 25. Differential Nonlinearity vs. Code (25°C)

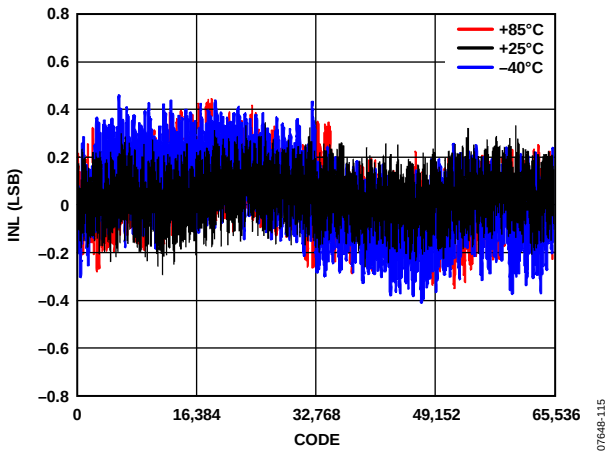


Figure 26. Integral Nonlinearity vs. Code vs. Temperature

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} at frequency, f_S.

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, *f*, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{\text{dB}} - 1.76)/6.02]$$

Gain Error
The first transition (from 100 … 000 to 100 …001) should occur at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = \frac{V_{INp\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Reference Voltage Temperature Coefficient
The reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}(Min)$ = minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
V_{REF} (25°C) = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error
Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Zero Error Drift

The ratio of the zero error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

THEORY OF OPERATION

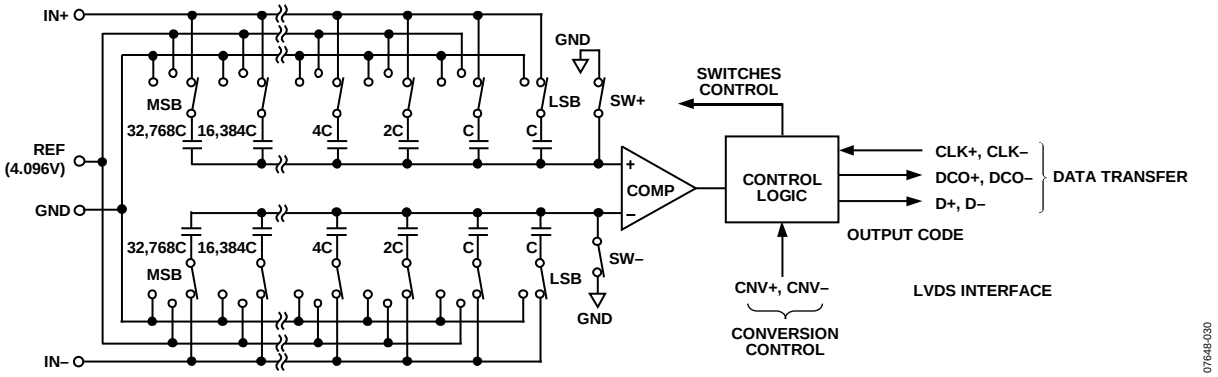


Figure 27. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7626 is a 10 MSPS, high precision, power efficient, 16-bit ADC that uses SAR-based architecture to provide a performance of 91.5 dB SNR, ±0.45 LSB INL, and ±0.35 LSB DNL.

The AD7626 is capable of converting 10,000,000 samples per second (10 MSPS). The device typically consumes 136 mW of power. The AD7626 offers the added functionality of a high performance on-chip reference and on-chip reference buffer.

The AD7626 is specified for use with 5 V and 2.5 V supplies (VDD1, VDD2). The interface from the digital host to the AD7626 uses 2.5 V logic only. The AD7626 uses an LVDS interface to transfer data conversions. The CNV+ and CNV− inputs to the part activate the conversion of the analog input. The CNV+ and CNV− pins can be applied using a CMOS or LVDS source.

The AD7626 is housed in a space-saving, 32-lead, 5 mm × 5 mm LFCSP.

CONVERTER INFORMATION

The AD7626 is a 10 MSPS ADC that uses SAR-based architecture to incorporate a charge redistribution DAC. Figure 27 shows a simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. In this way, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. A conversion phase is initiated when the acquisition phase is complete and the CNV input goes high. Note that the AD7626 can receive a CMOS or LVDS format CNV signal.

When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and 4.096 V (the reference voltage), the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65{,}536$). The control logic toggles these switches, MSB first, to bring the comparator back into a balanced condition. At the completion of this process, the control logic generates the ADC output code.

The AD7626 digital interface uses low voltage differential signaling (LVDS) to enable high data transfer rates.

The AD7626 conversion result is available for reading after t_{MSB} (time from the conversion start until MSB is available) has elapsed. The user must apply a burst LVDS CLK± signal to the AD7626 to transfer data to the digital host.

The CLK± signal outputs the ADC conversion result onto the data output D±. The bursting of the CLK± signal is illustrated in Figure 41 and Figure 42 and is characterized as follows:

- The differential voltage on CLK± should be held steady state in the time between t_{CLKL} and t_{MSB}.
- The AD7626 has two data read modes. For more information about the echoed-clock and self-clocked interface modes, see the Digital Interface section.

TRANSFER FUNCTIONS

The AD7626 uses a 4.096 V reference. The AD7626 converts the differential voltage of the antiphase analog inputs (IN+ and IN−) into a digital output. The analog inputs, IN+ and IN−, require a 2.048 V common-mode voltage (REF/2).

The 16-bit conversion result is in MSB first, twos complement format.

The ideal transfer functions for the AD7626 are shown in Figure 28 and Table 7.

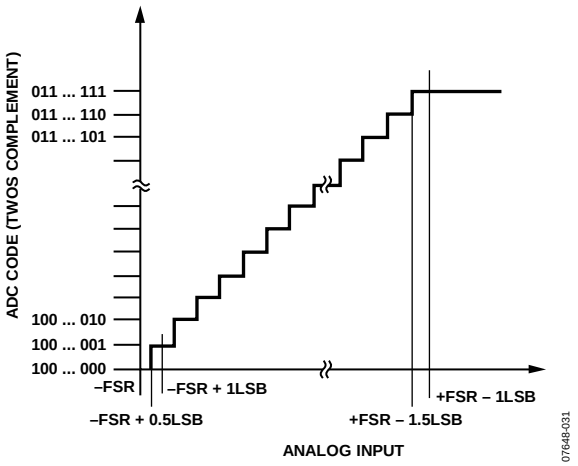


Figure 28. ADC Ideal Transfer Functions (FSR = Full-Scale Range)

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ – IN–) REF = 4.096 V	Digital Output Code Twos Complement (Hex)
FSR – 1 LSB	+4.095875V	0x7FFF
Midscale + 1 LSB	+125 µV	0x0001
Midscale	0 V	0x0000
Midscale – 1 LSB	−125 µV	0xFFFF
−FSR + 1 LSB	−4.095875 V	0x8001
−FSR	– 4.096 V	0x8000

ANALOG INPUTS

The analog inputs, IN+ and IN−, applied to the AD7626 must be 180° out of phase with each other. Figure 29 shows an equivalent circuit of the input structure of the AD7626.

The two diodes provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal does not exceed the reference voltage by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4899-1 in Figure 33) are different from those of the reference, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the part.

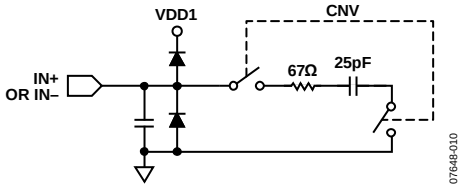


Figure 29. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected. The AD7626 shows some degradation in THD with higher analog input frequencies.

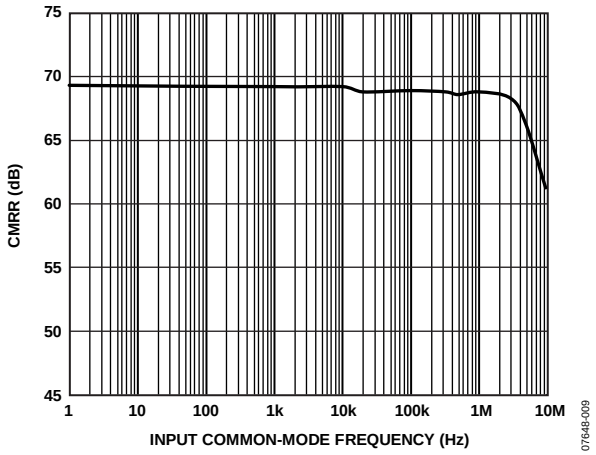
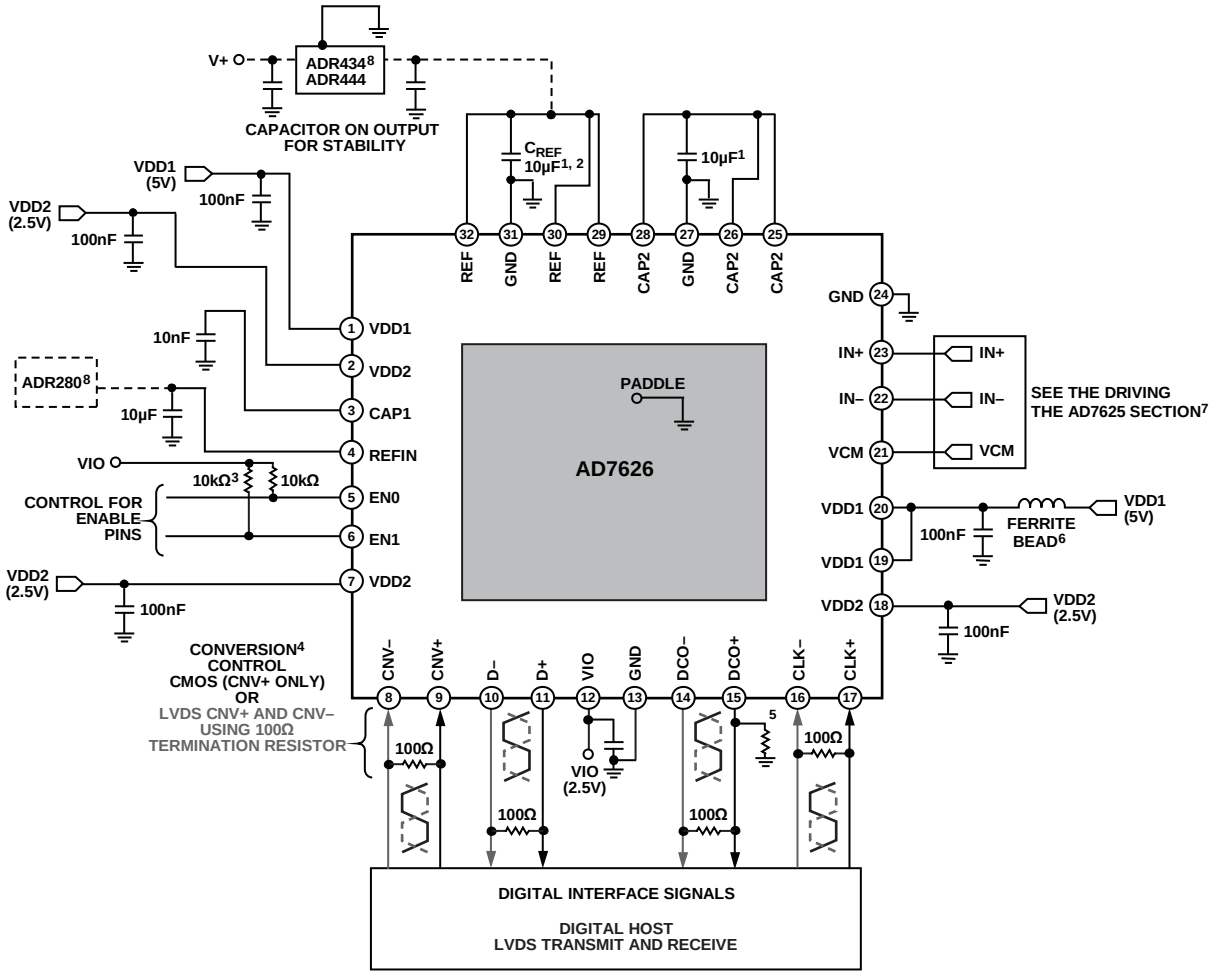


Figure 30. Analog Input CMRR vs. Frequency

TYPICAL CONNECTION DIAGRAM



[1] SEE THE LAYOUT, DECOUPLING, AND GROUNDING SECTION.
[2] C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR WITH LOW ESR AND ESL.
[3] USE PULL-UP OR PULL-DOWN RESISTORS TO CONTROL EN0 AND EN1 DURING POWER-UP. EN0 AND EN1 INPUTS CAN BE FIXED IN HARDWARE OR CONTROLLED USING A DIGITAL HOST (EN0 = 0 AND EN1 = 0 PUTS THE ADC IN POWER-DOWN).
[4] OPTION TO USE A CMOS (CNV+) OR LVDS (CNV±) INPUT TO CONTROL CONVERSIONS.
[5] TO ENABLE SELF-CLOCKED MODE, TIE DCO+ TO GND.
[6] CONNECT PIN 19 AND PIN 20 TO VDD1 SUPPLY; ISOLATE THE TRACE TO PIN 19 AND PIN 20 FROM THE TRACE TO PIN 1 USING A FERRITE BEAD SIMILAR TO WURTH 74279266.
[7] SEE THE DRIVING THE AD7626 SECTION FOR DETAILS ON AMPLIFIER CONFIGURATIONS.
[8] SEE THE VOLTAGE REFERENCE OPTIONS SECTION FOR DETAILS.

Figure 31. Typical Application Diagram

DRIVING THE AD7626

Differential Analog Input Source

Figure 33 shows an ADA4899-1 driving each differential input to the AD7626.

Single-Ended-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver (as shown in Figure 32) allows for a differential input into the part. This configuration, when provided with an input signal of 0 V to 4.096 V, produces a differential ±4.096 V with midscale at 2.048 V. The one-pole filter using R = 20 Ω and C = 56 pF provides a corner frequency of 140 MHz. The VCM output of the AD7626 can be buffered and then used to provide the required 2.048 V common-mode voltage.

Single-Ended or Fully Differential High Frequency Driver

In applications that require higher input frequency tones, the ADA4932-1 can be used to drive the inputs to the AD7626. The ADA4932-1 is a differential driver, which also allows the user the option of single-ended-to-differential conversion.

Figure 34 shows the typical circuit for a 50 Ω source impedance (ac-coupled in this example). The input to the ADA4932-1 is configured to be balanced to the source impedance (in this case 50 Ω). Further information on balancing the input impedance to the source impedance can be found on the ADA4932-1 datasheet. The circuit shown in Figure 34 operates with an overall gain of ~0.5 when the termination input termination is taken into account.

Alternatively, the ADA4932-1 can be used with a fully differential source—it acts as an inverting differential driver.

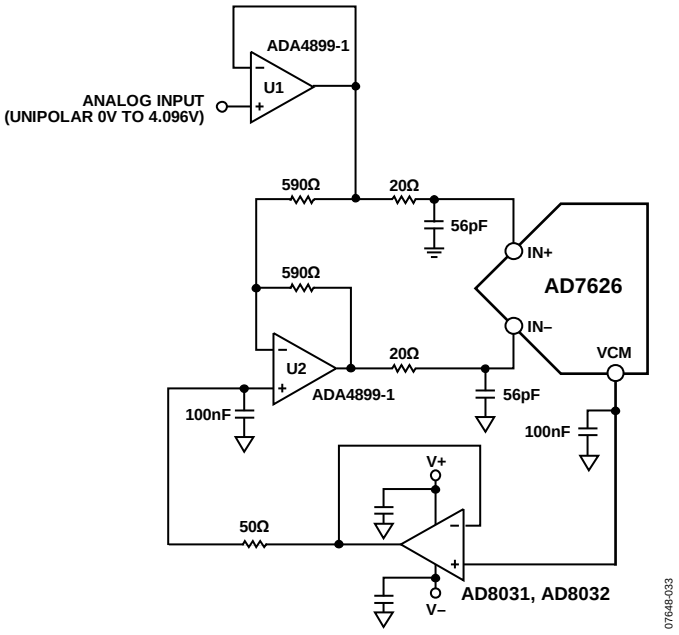


Figure 32. Single-Ended-to-Differential Driver Circuit Using ADA4899-1

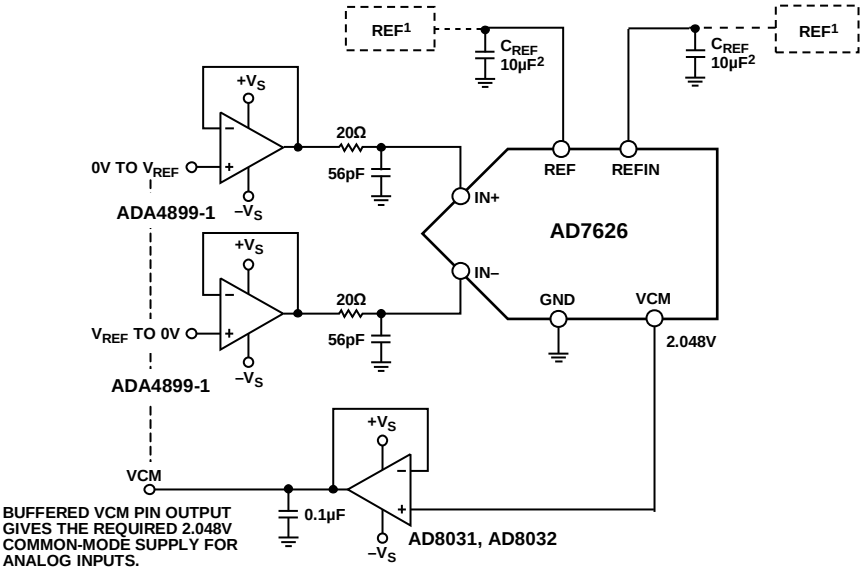


Figure 33. Driving the AD7626 from a Differential Analog Source Using ADA4899-1

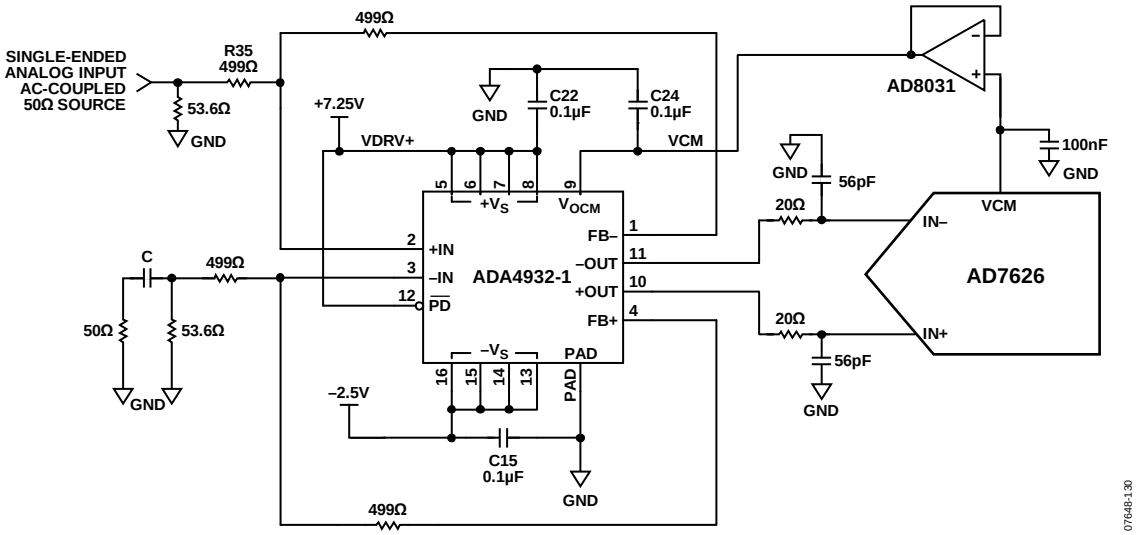


Figure 34. High Frequency Input Drive Circuit Using the ADA4932-1; Single-Ended-to Differential Configuration

VOLTAGE REFERENCE OPTIONS

The AD7626 allows flexible options for creating and buffering the reference voltage. The AD7626 conversions refer to 4.096 V only. The various options creating this 4.096 V reference are controlled by the EN1 and EN0 pins (see Table 8).

Table 8. Voltage Reference Options

Option	EN1	EN0	Reference Mode
A	1	1	Power-up Internal reference and internal reference buffer in use
B	0	1	External 1.2 V reference applied to REFIN pin required
C	1	0	External 4.096 V reference applied to REF pin required.
	0	0	Power-down mode

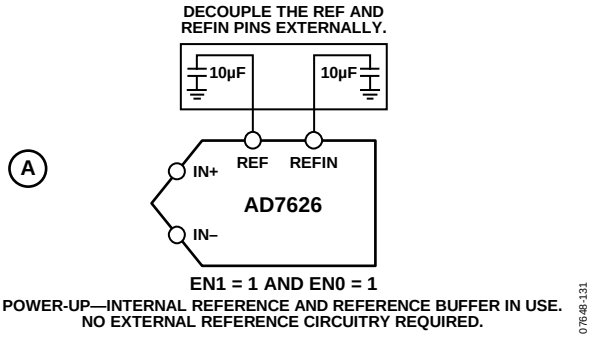


Figure 35. Powered Up, Internal Reference and Internal Reference Buffer

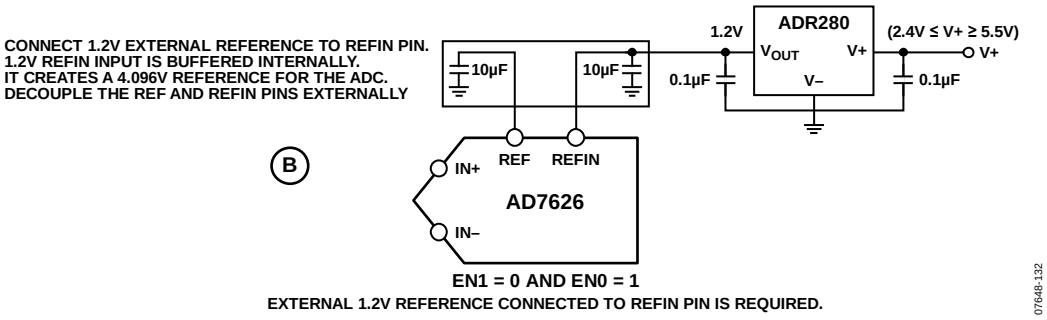


Figure 36. External 1.2 V Reference Using Internal Reference Buffer

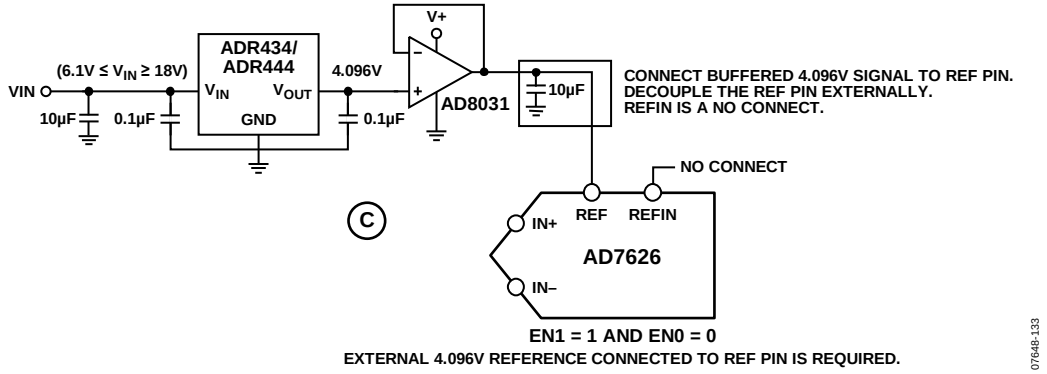


Figure 37. External 4.096 V Reference Applied to REF Pin

Wake-Up Time from EN1= 0, EN0 = 0

The AD7626 powers down when EN1 and EN0 are both set to 0. Selecting the correct reference choice from power-down, the user sets EN1 and EN0 to the required value shown in Table 8. The user may immediately apply CNV pulses to receive data conversion results. Typical wake-up times for the selected reference settings are shown in Table 9. Each time represents the duration from the EN1, EN0 logic transition to when the output of the ADC is settled to 0.5 LSB accuracy.

Table 9. Wake-Up Time from EN1=0, EN0 = 0

	Reference Mode	EN1	EN0	Wake-Up Time (0.5 LSB Accuracy)
A	Power-up Internal reference and internal reference buffer in use	1	1	9.5 sec
B	External 1.2 V reference applied to REFIN pin	0	1	25 ms
C	External 4.096 V reference applied to REF pin	1	0	65 µs

POWER SUPPLY

The AD7626 uses both 5 V (VDD1) and 2.5 V (VDD2) power supplies, as well as a digital input/output interface supply (VIO). VIO allows a direct interface with 2.5 V logic only. VIO and VDD2 can be taken from the same 2.5 V source; however, it is best practice to isolate the VIO and VDD2 pins using separate traces as well as to decouple each pin separately.

The 5 V and 2.5 V supplies required for the AD7626 can be generated using Analog Devices, Inc., LDOs such as the ADP3330-2.5, ADP3330-5, ADP3334, and ADP1708.

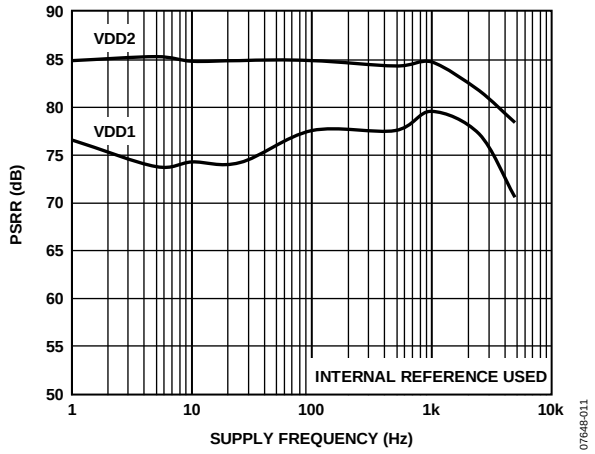


Figure 38. PSRR vs. Supply Frequency (350 mV pp Ripple on VDD2, 600 mV Ripple on VDD1)

Power-Up

When powering up the AD7626 device, first apply the 2.5 V VDD2 supply and VIO voltage to the device. After the VIO and 2.5 V VDD2 have been established, apply the 5 V VDD1 supply. If using an external reference with the AD7626, ensure that the EN0 and EN1 pins are connected to the correct logic values associated with the reference option of choice and then apply the external reference voltage. Finally, apply the analog inputs to the ADC.

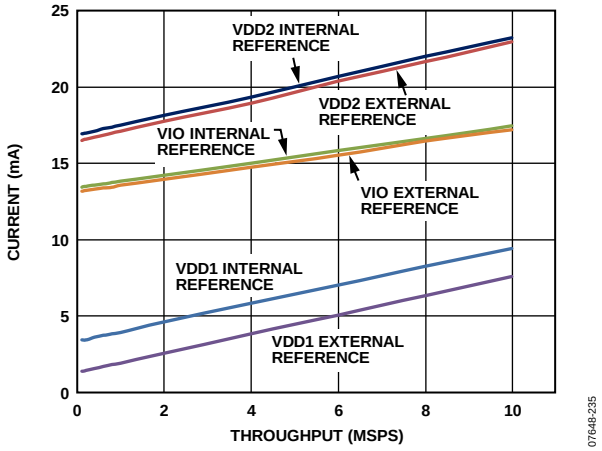


Figure 39. Current Consumption vs. Sampling Rate

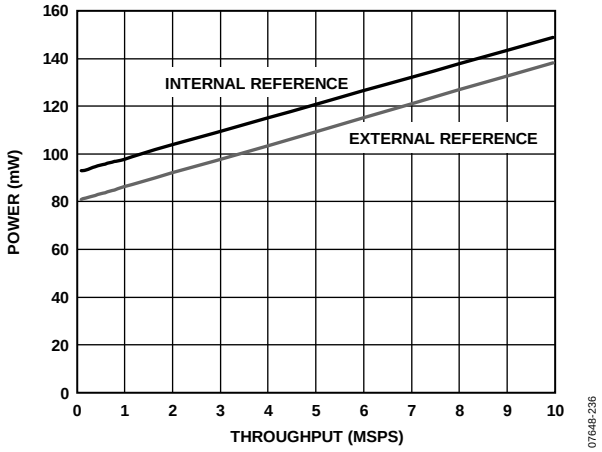


Figure 40. Power Dissipation vs. Sampling Rate

DIGITAL INTERFACE

Conversion Control

All analog-to-digital conversions are controlled by the CNV± signal. This signal can be applied in the form of a CNV+/CNV− LVDS signal, or it can be applied in the form of a 2.5 V CMOS logic signal to the CNV+ pin. The conversion is initiated by the rising edge of the CNV± signal.

After the AD7626 is powered up, the first conversion result generated is invalid. Subsequent conversion results are valid provided that the time between conversions does not exceed the maximum specification for t_{CYC}.

The two methods for acquiring the digital data output of the AD7626 via the LVDS interface are described in the following sections.

Echoed-Clock Interface Mode

The digital operation of the AD7626 in echoed-clock interface mode is shown in Figure 41. This interface mode, requiring only a shift register on the digital host, can be used with many digital hosts (such as FPGA, shift register, and microprocessor). It requires three LVDS pairs (D±, CLK±, and DCO±) between each AD7626 and the digital host.

The clock DCO± is a buffered copy of CLK± and is synchronous to the data, D±, which is updated on the falling edge of DCO + (t_D). By maintaining good propagation delay matching between D± and DCO± through the board and the digital host, DCO can be used to latch D± with good timing margin for the shift register.

Conversions are initiated by a rising edge CNV± pulse. The CNV± pulse must be returned low (≤ t_{CNVH} maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After the time, t_{MSB}, elapses, the host should begin to burst the CLK±. Note that, t_{MSB}, is the maximum time for the MSB of the new conversion result and should be used as the gating device for CLK±. The echoed clock, DCO±, and the data, D, are driven in phase with D± being updated on the falling edge of DCO+; the host should use the rising edge of DCO+ to capture D±. The only requirement is that the 16 CLK± pulses finish before the time (t_{CLKL}) elapses of the next conversion phase or the data is lost. From the t_{CLKL} to t_{MSB}, D± and DCO± are driven to 0. Set CLK± to idle low between CLK± bursts.

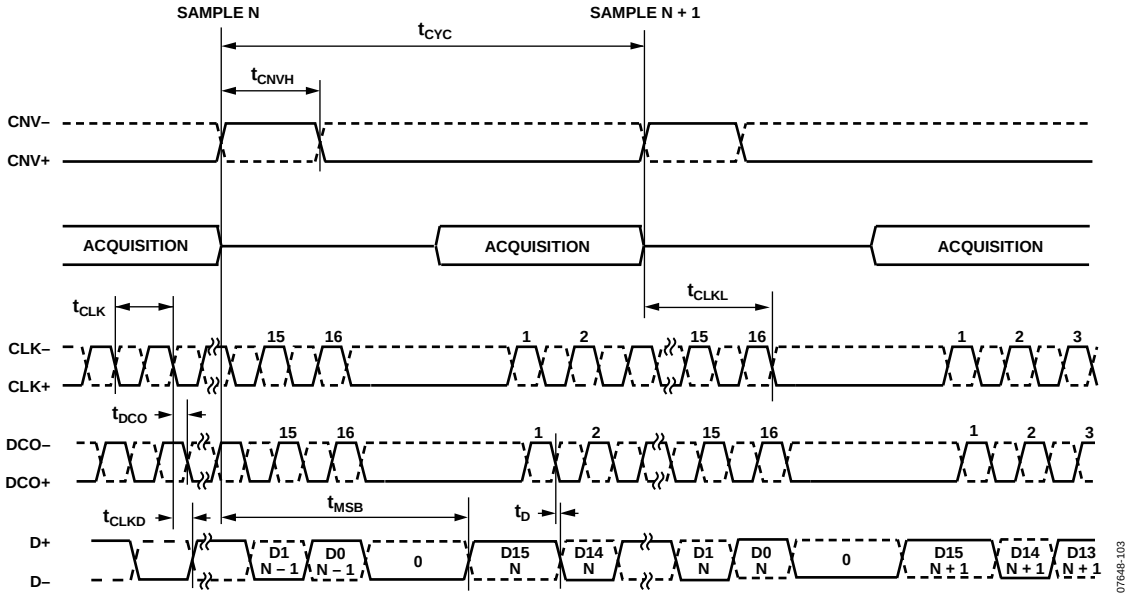


Figure 41. Echoed-Clock Interface Mode Timing Diagram

Self-Clocked Mode

The digital operation of the AD7626 in self-clocked interface mode is shown in Figure 42. This interface mode reduces the number of traces between the ADC and the digital host to two LVDS pairs (CLK± and D±) or to a single pair if sharing a common CLK±. Multiple AD7626 devices can share a common CLK± signal. This can be useful in reducing the number of LVDS connections to the digital host.

When the self-clocked interface mode is used, each ADC data-word is preceded by a 010 sequence. The first zero is automatically on D± once t_{MSB} has elapsed. The 2-bit header is then clocked out by the first two CLK± falling edges. This header is used to synchronize D± of each conversion in the digital host because, in this mode, there is no data clock output synchronous to the data (D±) to allow the digital host to acquire the data output.

Synchronization of the D± data to the digital host's acquisition clock is accomplished by using one state machine per AD7626 device. For example, using a state machine that runs at the same speed as CLK± incorporates three phases of this clock frequency (120° apart). Each phase acquires the data D± as output by the ADC.

The AD7626 data captured on each phase of the state machine clock is then compared. The location of the 1 in the header in each set of data acquired allows the user to choose the state machine clock phase that occurs during the data valid window of D±.

The self-clocked mode data capture method allows the digital host to adapt its result capture timing to accommodate variations in propagation delay through any AD7626.For example, where data is captured from multiple AD7626s sharing a common input clock.

Conversions are initiated by a CNV± pulse. The CNV± pulse must be returned low (t_{CNVH} maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After the time, t_{MSB}, elapses, the host begins to burst the CLK± signal to the AD7626. All 18 CLK± pulses are to be applied in the time window framed by t_{MSB} and the subsequent t_{CLKL}. The required 18 CLK± pulses must finish before t_{CLKL} (referenced to the next conversion phase) elapses. Otherwise, the data is lost because it is overwritten by the next conversion result.

Set CLK± to idle high between bursts of 18 CLK± pulses. The header bit and conversion data of the next ADC result are output on subsequent falling edges of CLK± during the next burst of the CLK± signal.

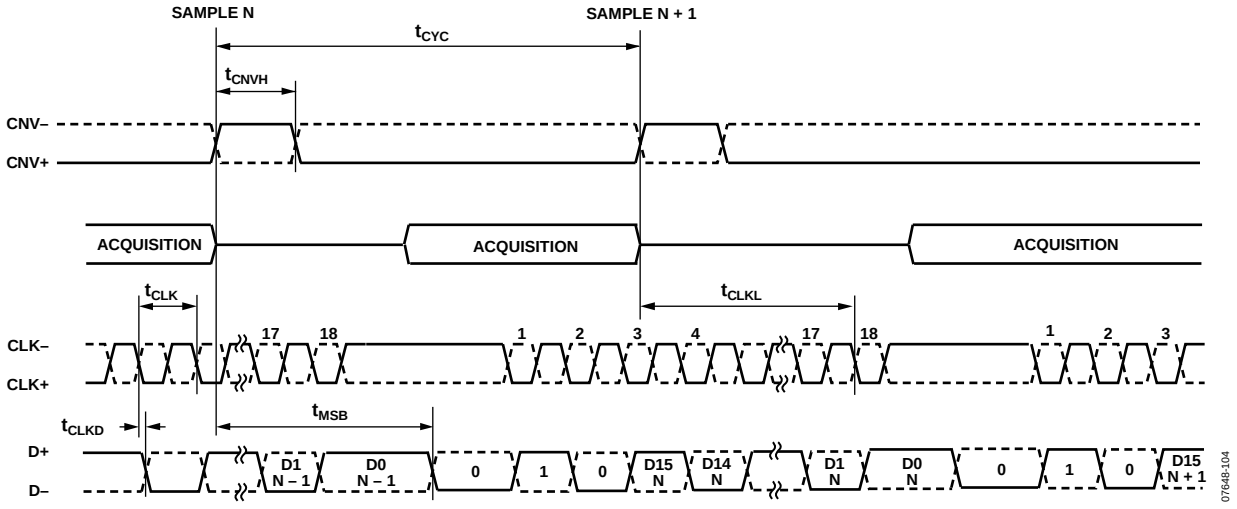


Figure 42. Self-Clocked Interface Mode Timing Diagram

APPLICATIONS INFORMATION

LAYOUT, DECOUPLING, AND GROUNDING

When laying out the printed circuit board (PCB) for the AD7626, follow the practices described in this section to obtain the maximum performance from the converter.

Exposed Paddle

The AD7626 has an exposed paddle on the underside of the package.

- Solder the paddle directly to the PCB.
- Connect the paddle to the ground plane of the board using multiple vias, as shown in Figure 43.
- Decouple all supply pins except for Pin 12 (VIO) directly to the paddle, minimizing the current return path.
- Pin 13 and Pin 24 can be connected directly to the paddle. Use vias to ground at the point where these pins connect to the paddle.

VDD1 Supply Routing and Decoupling

The VDD1 supply is connected to Pin 1, Pin 19, and Pin 20. Decouple the supply using a 100 nF capacitor at Pin 1. The user can connect this supply trace to Pin 19 and Pin 20. Use a series ferrite bead to connect the VDD1 supply from Pin 1 to Pin 19 and Pin 20. The ferrite bead isolates any high frequency noise or ringing on the VDD1 supply. Decouple the VDD1 supply to Pin 19 and Pin 20 using a 100 nF capacitor decoupled to ground at the exposed paddle.

VIO Supply Decoupling

Decouple the VIO supply applied to Pin 12 to ground at Pin 13.

Layout and Decoupling of Pin 25 to Pin 32

Connect the outputs of Pin 25, Pin 26, and Pin 28 together and decouple them to Pin 27 using a 10 µF capacitor with low ESR and low ESL.

Reduce the inductance of the path connecting Pin 25, Pin 26, and Pin 28 by widening the PCB traces connecting these pins.

Take a similar approach in the connections used for the reference pins of the AD7626. Connect Pin 29, Pin 30, and Pin 32 together using widened PCB traces to reduce inductance. In internal or external reference mode, a 4.096 V reference voltage is output on Pin 29, Pin 30, and Pin 32. Decouple these pins to Pin 31 using a 10 µF capacitor with low ESR and low ESL.

Figure 43 shows an example of the recommended layout for the underside of the AD7626 device. Note the extended signal trace connections and the outline of the capacitors decoupling the signals applied to the REF pins (Pin 29, Pin 30, and Pin 32) and to the CAP2 pins (Pin 25, Pin 26, and Pin 28).

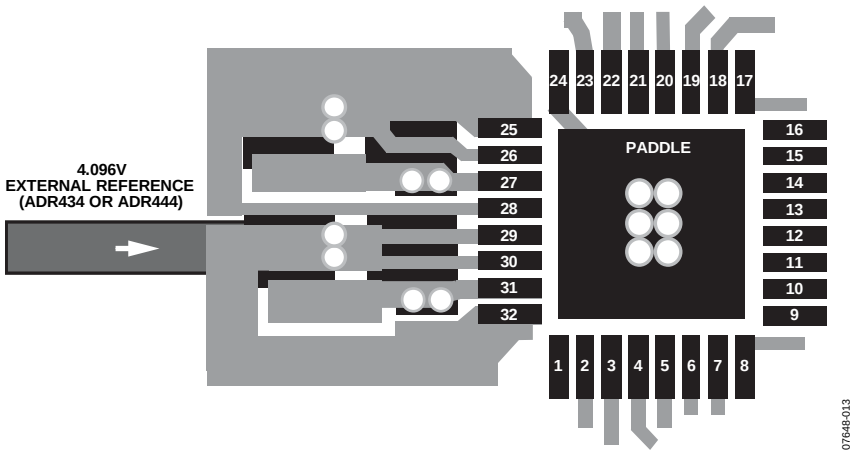


Figure 43. PCB Layout and Decoupling Recommendations for Pin 24 to Pin 32

OUTLINE DIMENSIONS

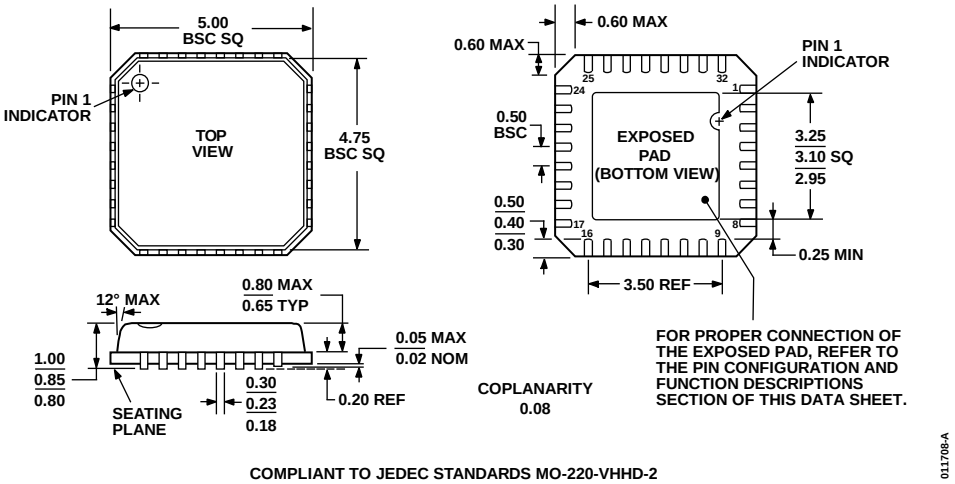


Figure 44. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7626BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD7626BCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
EVAL-AD7626EDZ[2]		Evaluation Board	
EVAL-CED1Z[3]		Converter Evaluation and Development Board	

[1] Z = RoHS Compliant Part.
[2] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CEDIZ for evaluation/demonstration purposes.
[3] This board allows the PC to control and communicate with all Analog Devices evaluation boards with model numbers ending with the ED designator.

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