- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(ON)}$ Specified at VGS=4V & 5V
- 150℃ Operating Temperature
- Fast Switching
- Ease of paralleling

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The To-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@ Tc=25℃	Continuous Drain Current, V_{GS}@5.0V	9.0	A
I_D@ Tc=100℃	Continuous Drain Current, V_{GS} @ 5.0V	5.7	
I_{DM}	Pulsed Drain Current ①	36	
P_D@ Tc=25℃	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/℃
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	250	mJ
I_{AR}	Avalanche Current ①	9.0	A
E_{AR}	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	℃
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

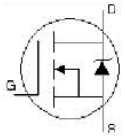
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\Theta JC}$	Junction-to-Case	-	-	1.7	℃/W
R_{QCS}	Case-to-Sink, Flat, Greased Surface	-	0.50	-	
R_{QJA}	Junction-to-Ambient	-	-	62	

Electrical Characteristics @ T_J=25℃ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	-	0.27	-	V/°C	Reference to 25°C, I_D=1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	-	-	0.40	Ω	V_{GS}=5.0V, I_D=5.4A
		-	-	0.50		V_{GS}=4.0V, I_D=4.5A
$V_{GS(th)}$	Gate Threshold Voltage	1.0	-	2.0	V	V_{DS}=V_{GS}, I_D=250μA
gfs	Forward Transconductance	4.8	-	-	s	V_{DS}=50V, I_D=5.4A
I_{DSS}	Drain-to-Source Leakage Current	-	-	25	μA	V_{DS}=200V, V_{GS}=0V
		-	-	250		V_{DS}=160V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	-	-	100	nA	V_{GS}=10V
	Gate-to-Source Reverse Leakage	-	-	-100		V_{GS}=-10V
Qg	Total Gate Charge	-	-	40	nC	I_D=9.0A
Qgs	Gate-to-Source Charge	-	-	5.5		V_{DS}=160V
Qgd	Gate-to-Drain (“Miller”) Charge	-	-	24		V_{GS}=10V, See Fig.6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	-	8.0	-	ns	V_{DD}=100V
tr	Rise Time	-	57	-		I_D=9.0A
$t_{d(off)}$	Turn-Off Delay Time	-	38	-		R_G=6.0Ω
tf	Fall Time	-	33	-		R_D=11Ω, See Fig. 10④
L_D	Internal Drain Inductance	-	4.5	-	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	-	7.5	-		
Ciss	Input Capacitance	-	1100	-	pF	V_{GS}=0V
Coss	Output Capacitance	-	220	-		V_{DS}=25V
Crss	Reverse Transfer Capacitance	-	70	-		f=1.0MHz, See Fig.5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
Is	Continuous Source Current(Body Diode)	-	-	9.0	A	MOSFET symbol showing the integral reverse p-n junction diode 
I_{SM}	Pulsed Source Current (Body Diode) ①	-	-	36		
V_{SD}	Diode Forward Voltage	-	-	2.0	V	T_J=25°C, I_S=9.0A, V_{GS}=0V ④
trr	Reverse Recovery Time	-	230	350	ns	TJ=25°C, IF=9.0A
Qrr	Reverse Recovery Charge	-	1.7	2.6	μC	di/dt=100A/μs ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L s+L_D)				

Notes:

① Repetitive rating; Pulse width Limited by max. junction temperature. (See fig. 11)

② V_{DD}=25V, starting T_J=25°C, L=4.6mH R_G=25Ω, I_{AS}=9.0A. (See Figure 12)

③ I_{SD}≤9.0A, di/dt ≤120A/μs, V_{DD}≤$V_{(BR)DSS}$,T_J≤150°C

④Pulse width ≤300μs; duty cycle ≤2%.

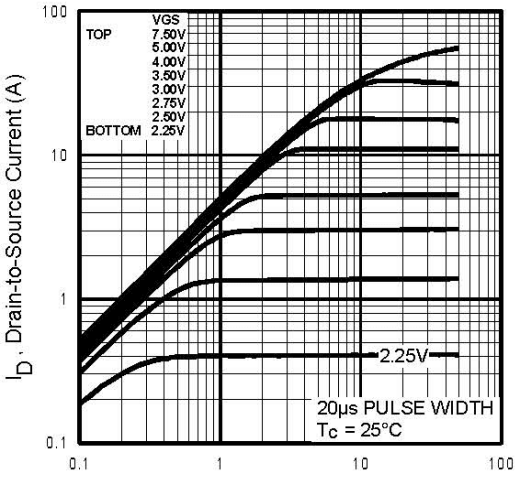


Fig 1. Typical Output Characteristics, T_C=25°C

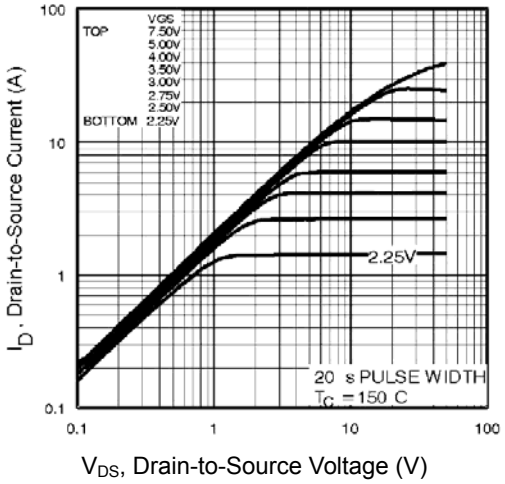


Fig 2. Typical Output Characteristics, Tc=150°C

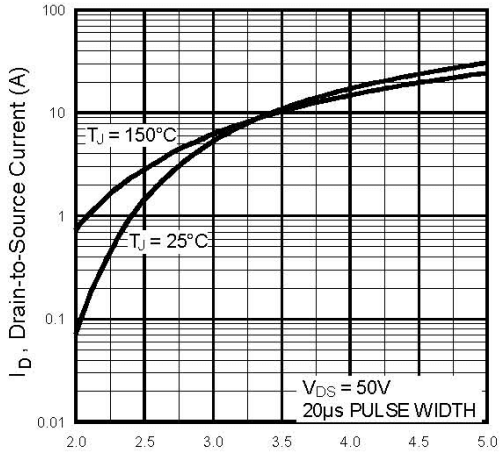


Fig 3. Typical Transfer Characteristics

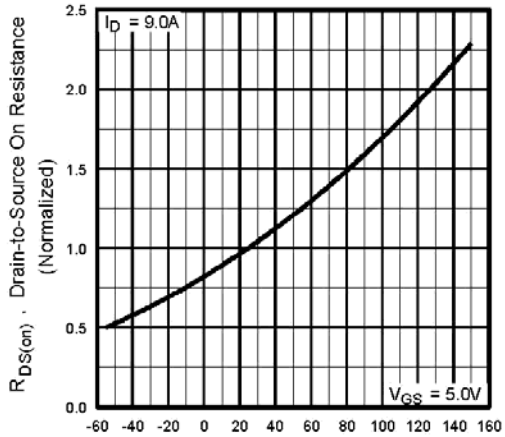


Fig 4. Normalized On-Resistance Vs. Temperature

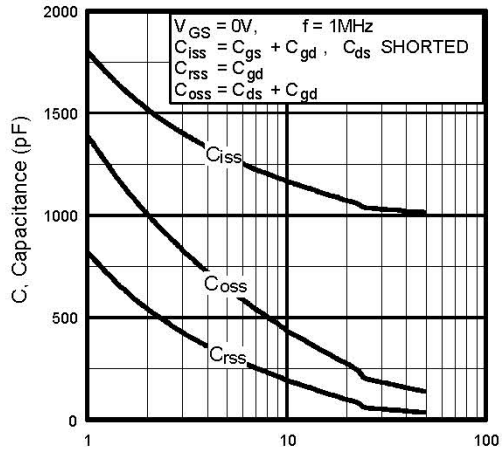


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

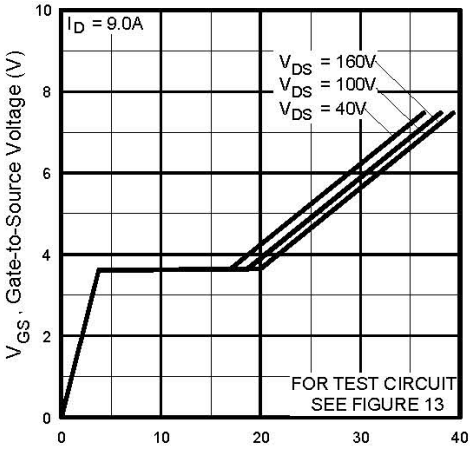
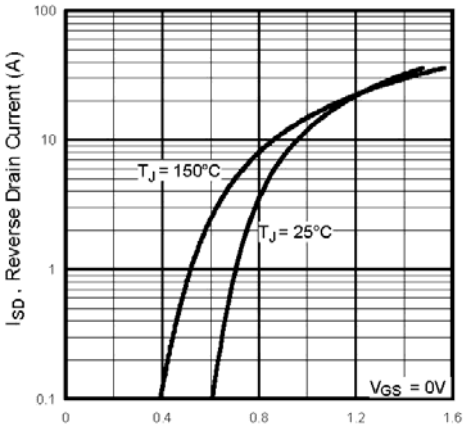


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage

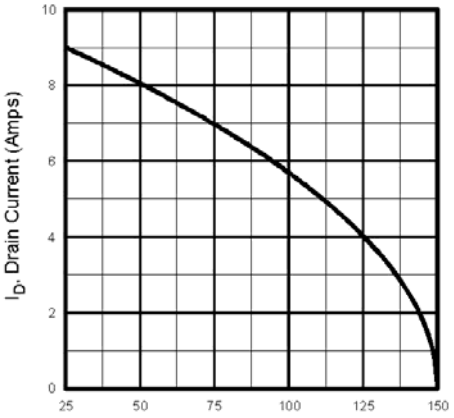
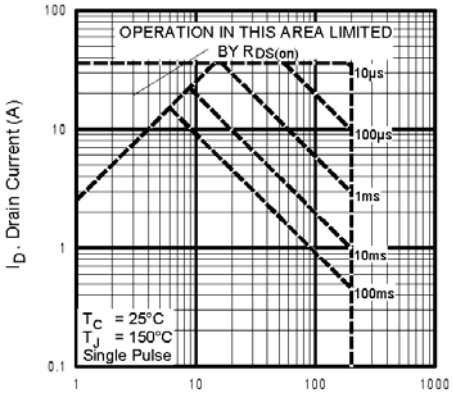


Fig 9. Maximum Drain Current Vs. Case Temperature



V_{DS}, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

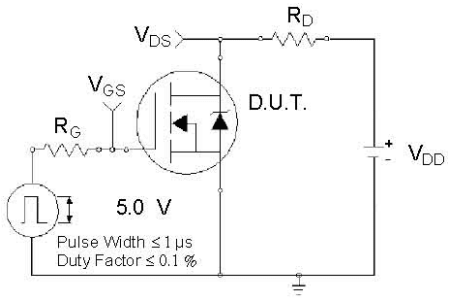


Fig 10a. Switching Time Test Circuit

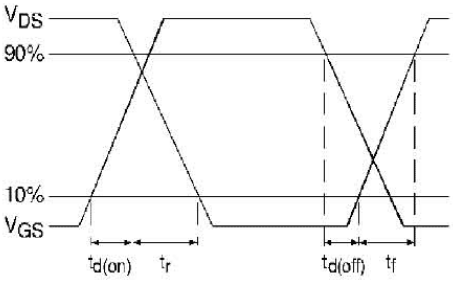
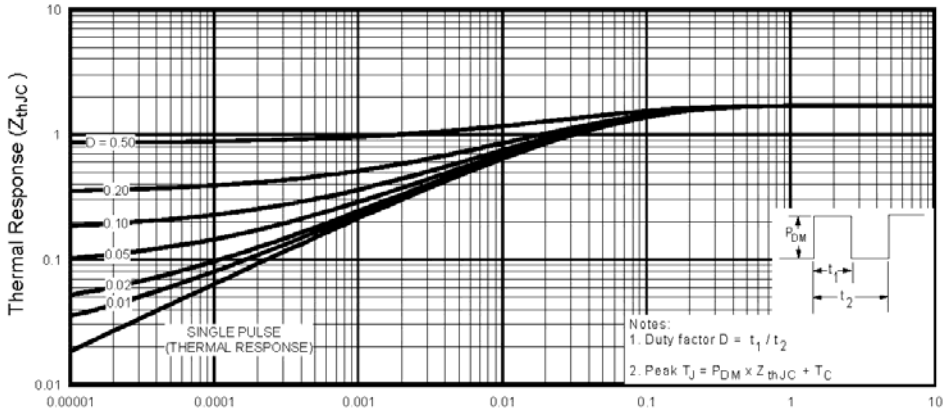


Fig 10b, Switching Time Waveforms



t1, Rectangular Pulse Duration (sec)

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

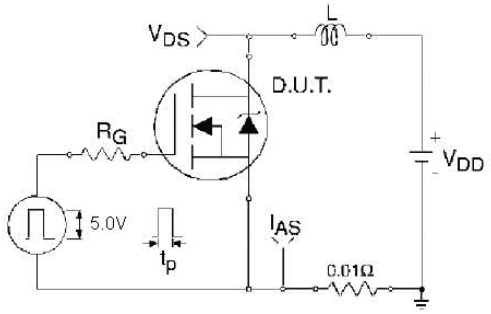


Fig 12a. Unclamped Inductive Test Circuit

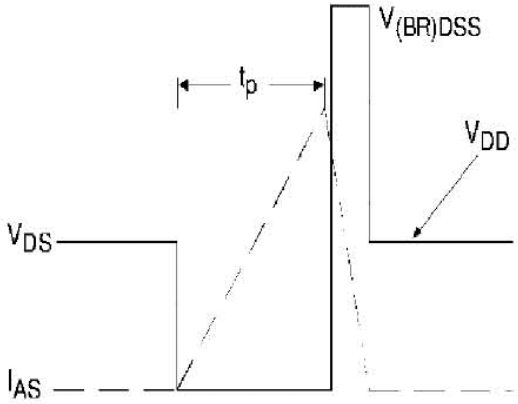


Fig 12b. Unclamped Inductive Waveforms

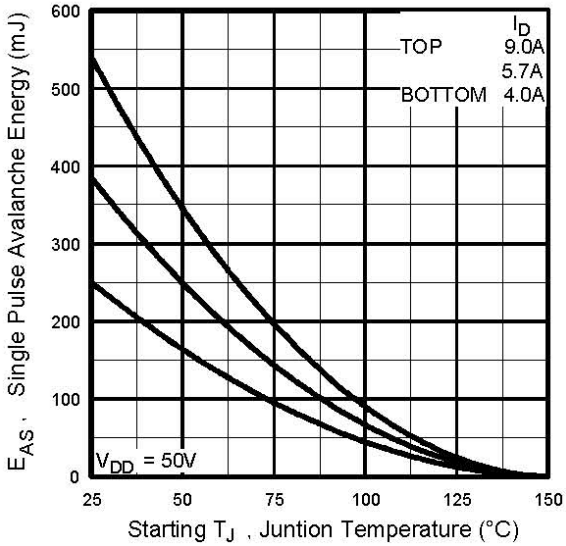


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

5.0V

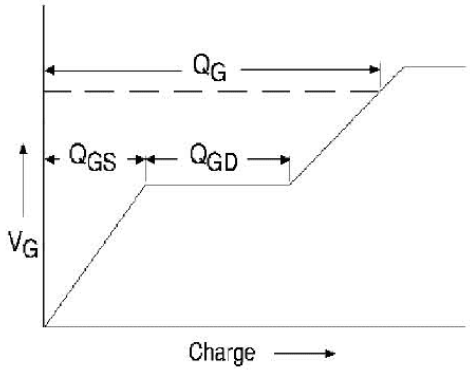


Fig 13a. Basic Gate Charge Waveform

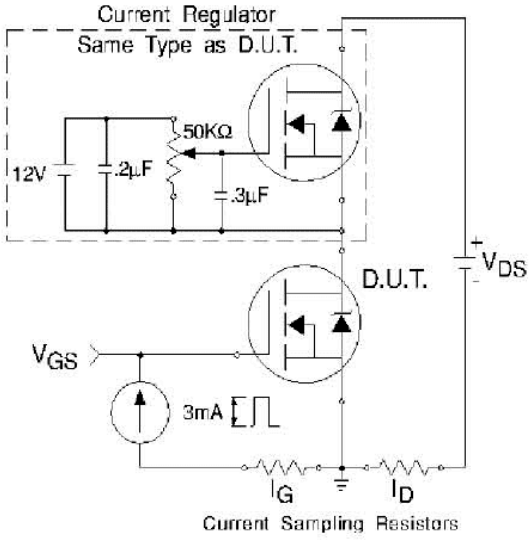
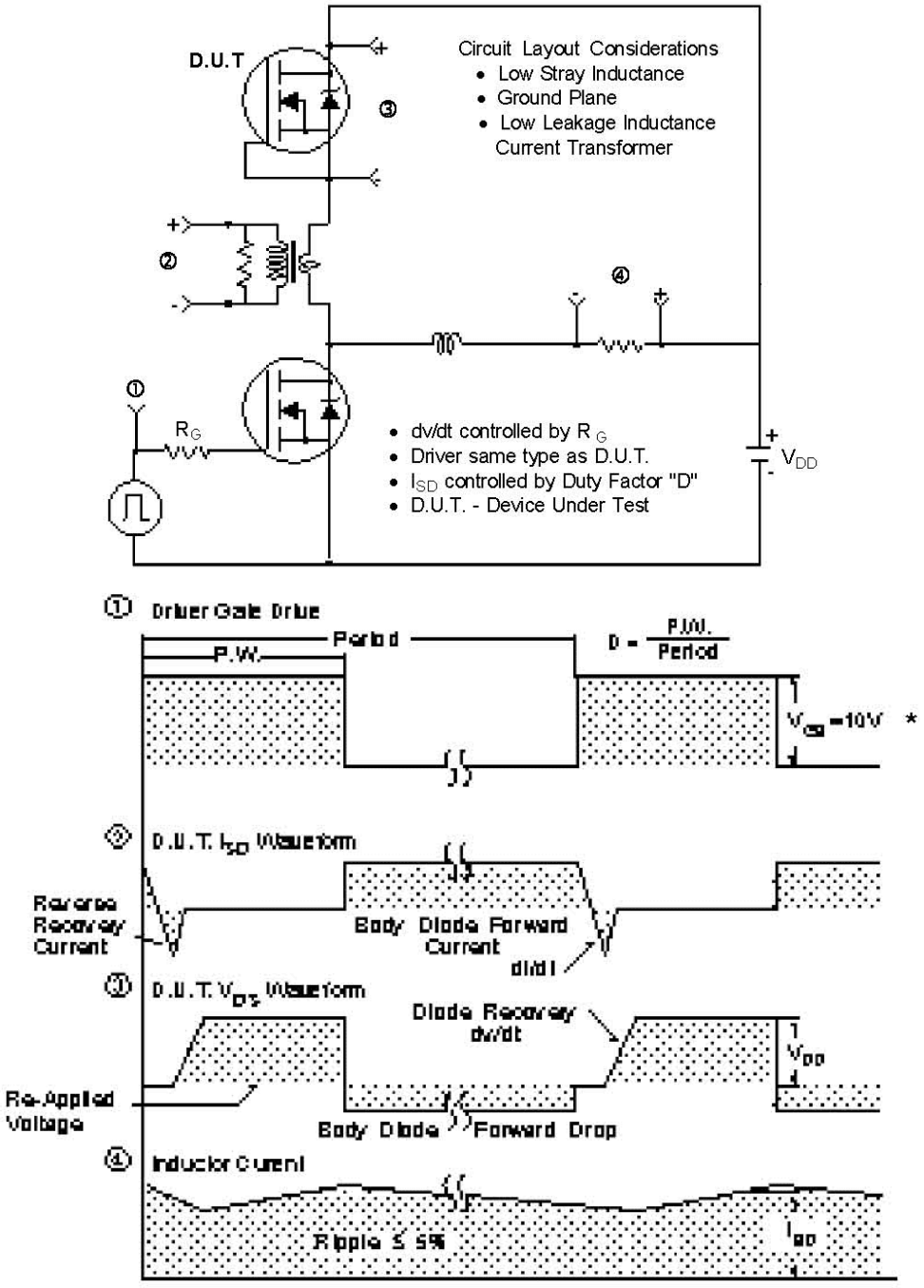


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

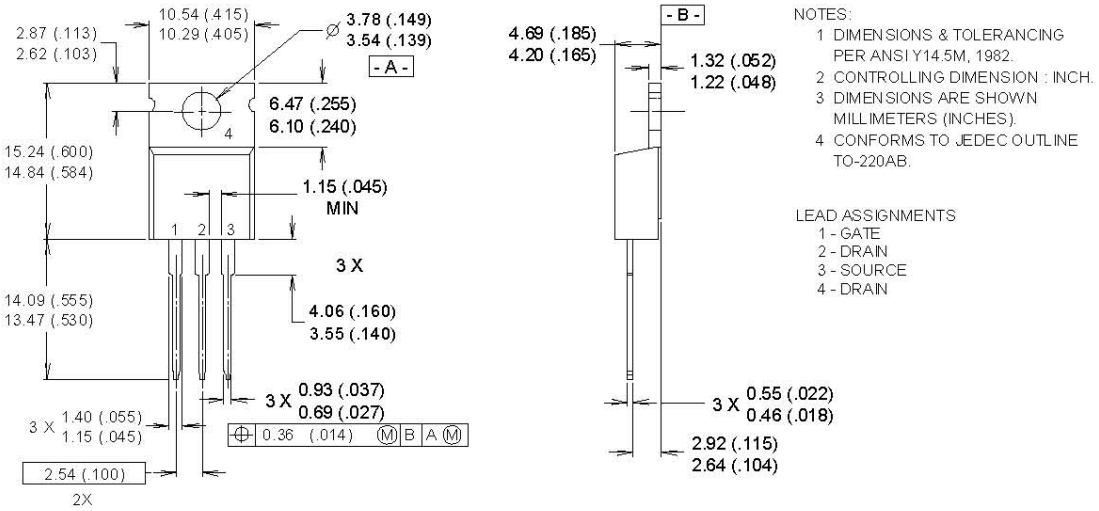


* VGS = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline



CONFORMS TO JEDEC OUTLINE TO-220AB

Dimensions in Millimeters and (Inches)