G-LINK Technology

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GLT41116

64k x 16 CMOS Dynamic RAM with Fast Page Mode

Features

- 65,536 words by 16 bits organization.
- Fast access time and cycle time.
- Dual $\overline{CAS}$ input.
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 256 refresh cycles per 4ms.
- Available in 40-Pin 400 mil SOJ, and 40/44-Pin TSOP (Type II).
- Single 5.0V±10% Power Supply.
- All inputs and Outputs are TTL compatible.
- Fast Page Mode operation.

General Description

The GLT41116 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41116 offers Fast Page mode, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT41116 has symmetric address and accepts 256-cycle refresh in 4ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256x16 bits, within a page, with cycle times as short as 18ns.

The GLT41116 is best suited for graphics, and DSP applications requiring high performance memories.

Functional Block Diagram

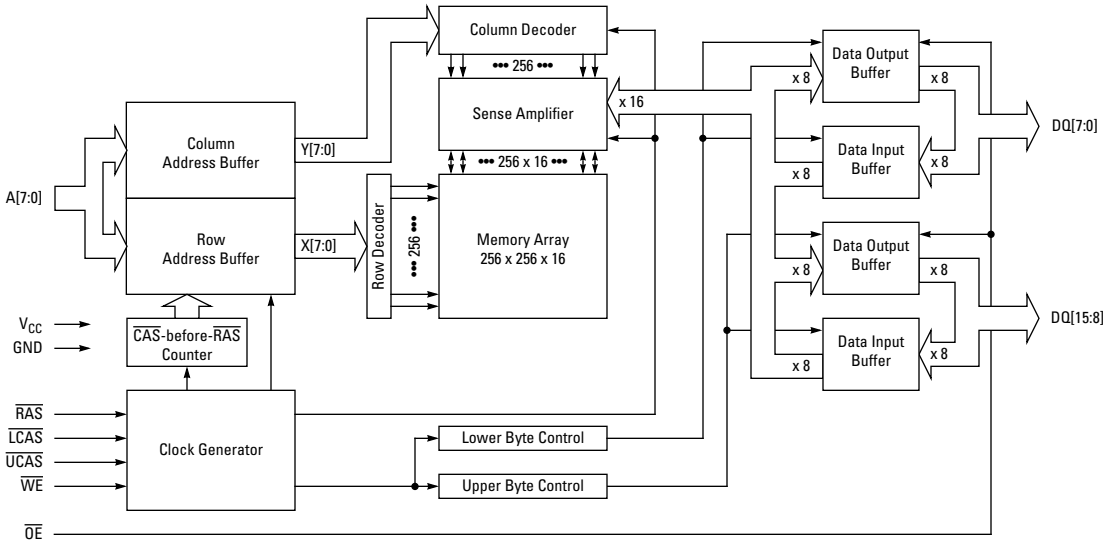


Figure 1. GLT41116 64 x 16 CMOS

Signal Descriptions

Symbol	Type	Description
A0 - A7	Input	Address Inputs
$\overline{RAS}$	Input	Row address strobe
$\overline{UCAS}$	Input	Column address strobe/upper byte control
$\overline{LCAS}$	Input	Column address strobe/lower byte control
$\overline{WE}$	Input	Write enable
$\overline{OE}$	Input	Output enable
DQ[15:0]	Input	Data inputs/outputs
V_{CC}	Input	+5V power supply
V_{SS}	Input	Ground
NC	Input	No connection

Truth Table

Function		Address	$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	DQ	Notes
Stand By			H	H → X	H → X	X	X	High-Z	
Read: Word		Row/Col	L	L	L	H	I	Data Out	
Read: Lower Byte		Row/Col	L	L	H	H	L	Lower Byte, Data-Out Upper Byte, High-Z	
Read: Upper Byte		Row/Col	L	H	L	H	L	Lower Byte, High-Z Upper Byte, Data Out	
Write: Word (Early Write)		Row/Col	L	L	L	L	X	Data-In	
Write: Lower Byte (Early)		Row/Col	L	L	H	L	X	Lower Byte, Data-In Upper Byte, High-Z	
Write: Upper Byte (Early)		Row/Col	L	H	L	L	X	Lower Byte, High-Z Upper Byte, Data-In	
Read Write		Row/Col	L	L	L	H → L	L → H	Data-Out, Data-In	[1] [2]
Fast-Page Mode Read	1st Cycle	Row/Col	L	H → L	H → L	H	L	Data-Out	[1]
	2nd Cycle	Col	L	H → L	H → L	L	X	Data-Out	[1]
Fast-Page Mode Write	1st Cycle	Row/Col	L	H → L	H → L	L	X	Data-In	[2]
	2nd Cycle	Col	L	H → L	H → L	L	X	Data-In	[2]
Fast-Page Mode Read-Write	1st Cycle	Row/Col	L	H → L	H → L	H → L	L → H	Data-Out, Data-In	[1] [2]
	2nd Cycle	Col	L	H → L	H → L	H → L	L → H	Data-Out, Data-In	[1] [2]
Hidden Refresh	Read	Row/Col	L → H → L	L	L	H	L	Data-Out	[1]
	Write	Row/Col	L → H → L	L	L	L	X	Data-In	[2] [3]
$\overline{RAS}$-Only Refresh		Row	L	H	H	X	X	High-Z	
CBR Refresh			H → L	L	L	X	X	High-Z	[4]

1. These READ cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
3. EARLY WRITE Only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{UCAS}$ or $\overline{LCAS}$).

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Parameter	Rating
Operating Temperature, T_A (ambient)	-0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Voltage Relative to V_{SS}	-1.0V to +7.0V
Short Circuit Output Current'	50 mA
Power Dissipitation	1.0 W

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance [1]

Symbol	Parameter	Max	Units
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

1. Capacitance is sampled and not 100% tested

DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise specified)

			-30		-35		-40		-45			
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	-10	+10	-10	+10	-10	+10	-10	+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{OUT} ≤ 5.5V Output is disabled (Hiz)		+10		+10		+10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)		180		170		160		150	mA	[1] [2]
I_{CC2}	Standby Current, (TTL)	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} other inputs ≥ V_{SS}		2		2		2		2	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{RAS}$ cycling, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} t_{RC} = t_{RC} (min.)		180		170		160		150	mA	[2]
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at $\overline{VIL}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{PC} = t_{PC} (min.)		180		170		160		150	mA	[1] [2]
I_{CC5}	Refresh Current, $\overline{CAS}$-before-$\overline{RAS}$	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{RC} = t_{RC} (min.)		180		170		160		150	mA	[1]
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥ V_{CC} -0.2V, $\overline{UCS}$ ≥ V_{CC} -0.2V, $\overline{LCAS}$ ≥ V_{CC} -0.2V, All other inputs ≥ V_{CC}		2		2		2		2	mA	
V_{IL}	Input Low Voltage		-1	+0.8	-1	+0.8	-1	+0.8	-1	+0.8	V	[3]
V_{IH}	Input High Voltage		2.4	V_{CC} +1	2.4	V_{CC} +1	2.4	V_{CC} +1	2.4	V_{CC} +1	V	
V_{OL}	Output Low Voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		2.4		2.4		2.4		V	

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified I_{CC} (max) is measured with a maximum of one transition per address cycle in random READ/WRITE and Fast-Page Mode.
3. Specified V_{IL} (min) is steady state operation. During transitions V_{IL} (min) may undershoot to -1.0V for a period not to exceed 20 ns. All AC parameter are measured with V_{IL} (min) ≥ VSS and V_{IH} (max) ≤ V_{CC}.

AC Characteristics (0 °C ≤ T_A ≤ 70 °C, V_{CC} = 5.0V ± 10%) [1] [2]

Parameter	Symbol	-30		-35		-40		-45		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{RC}	65	–	70	–	75	–	80	–	ns	
Read Modify Write Cycle Time	t_{RWC}	80	–	99	–	105	–	110	–	ns	
Access Time for $\overline{RAS}$	t_{RAC}	–	30	–	35	–	40	–	45	ns	[3] [4]
Access Time for $\overline{CAS}$	t_{CAC}	–	10	11	–	12	–	–	12	ns	[3] [4]
Access TIme from Column Address	t_{AA}	–	15	–	18	–	20	–	22	ns	[3] [4]
$\overline{CAS}$ to output ion Low-Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	[3]
Output buffer turn-off delay from $\overline{CAS}$	t_{OFF}	3	8	3	8	3	8	3	8	ns	[5]
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	[2]
$\overline{RAS}$ Precharge Time	t_{RP}	25	–	25	–	25	–	25	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	30	100k	35	100k	40	100k	45	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	–	12	–	12	–	13	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	30	–	36	–	40	–	46	–	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	12	10k	12	10k	13	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	13	20	17	24	18	28	18	33	ns	[4]
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	10	15	12	17	13	20	12	23	ns	[4]
$\overline{CAS}$ To $\overline{RAS}$ Precharge Time	t_{CPRP}	5	–	5	–	5	–	5	–	ns	[6]
Row Address Setup TIme	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	6	–	6	–	6	–	6	–	ns	
Column Address Setup Time	t_{ASC}	26	–	30	–	34	–	39	–	ns	
Column Address Hold Time	t_{CAH}	15	–	18	–	20	–	23	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	26	–	30	–	34	–	39	–	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	15	–	18	–	20	–	23	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	[7]
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	[7]
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	6	–	6	–	6	–	6	–	ns	[8]
Write Command Hold time Referenced to $\overline{RAS}$	t_{WCR}	26	–	30	–	34	–	39	–	ns	[9]
$\overline{WE}$ Pulse Width	t_{WP}	6	–	6	–	6	–	6	–	ns	[8]
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	–	11	–	12	–	12	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	11	–	12	–	12	–	ns	
Data-In Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	[10]
Data-In Hold Time	t_{DH}	7	–	6	–	8	–	8	–	ns	[10]
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	27	–	31	–	36	–	41	–	ns	[11]
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	[9]
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	47	–	58	–	63	–	68	–	ns	[9]
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	24	–	29	–	30	–	30	–	ns	[9]
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	29	–	36	–	38	–	40	–	ns	[9]
$\overline{CAS}$ Setup TIme ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	t_{CPT}	20	–	20	–	20	–	20	–	ns	
Access Time From $\overline{CAS}$ Precharge	t_{CPA}	–	18	–	21	–	23	–	25	ns	[3]
Fast Page Mode Read/Write Cycle Time	t_{PC}	18	–	21	–	23	–	25	–	ns	

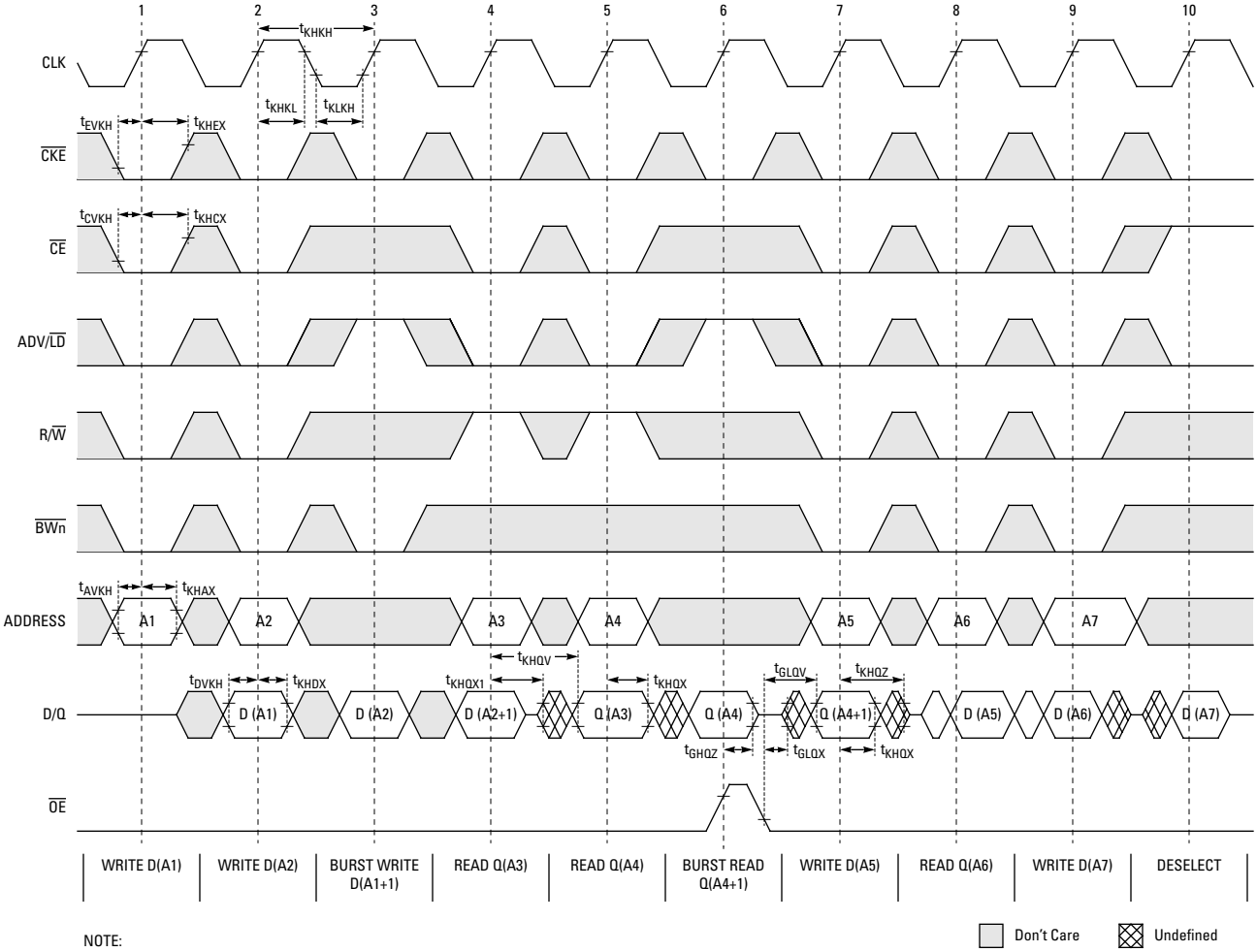
AC Characteristics (0 °C ≤ T_A ≤ 70 °C, V_{CC} = 5.0V ± 10%) [1] [2]

Parameter	Symbol	-30		-35		-40		-45		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	48	–	60	–	53	–	65	–	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	6	–	6	–	7	–	7	–	ns	
$\overline{RAS}$ Pulse Width (Fast PAge Mode)	t_{RASP}	30	100k	35	100k	40	100k	45	100k	ns	
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	25	–	25	–	25	–	30	–	ns	
Access Time From $\overline{OE}$	t_{OEA}	–	10	–	11	–	12	–	12	ns	
$\overline{OE}$ to Delay Time	t_{OED}	8	–	8	–	8	–	8	–	ns	
Output Buffer Turn-off Delay Time From $\overline{OE}$	t_{OEZ}	3	–	3	8	3	8	3	8	ns	[5]
$\overline{OE}$ Hold Time	t_{OEH}	6	–	6	–	7	–	7	–	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	–	15	–	15	–	15		ns	
Refresh Time (256 Cycles)	t_{REF}	–	4	–	4	–	4	–	4	ms	

1. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycles to initialize the internal circuit.
2. V_{IH} (min) and V_{IL} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), AC measurements assume t_T = 3 ns.
3. Measured with an equivalent to 2 TTL loads and 100 pF.
4. For read cycles, the access time is defined as follows:

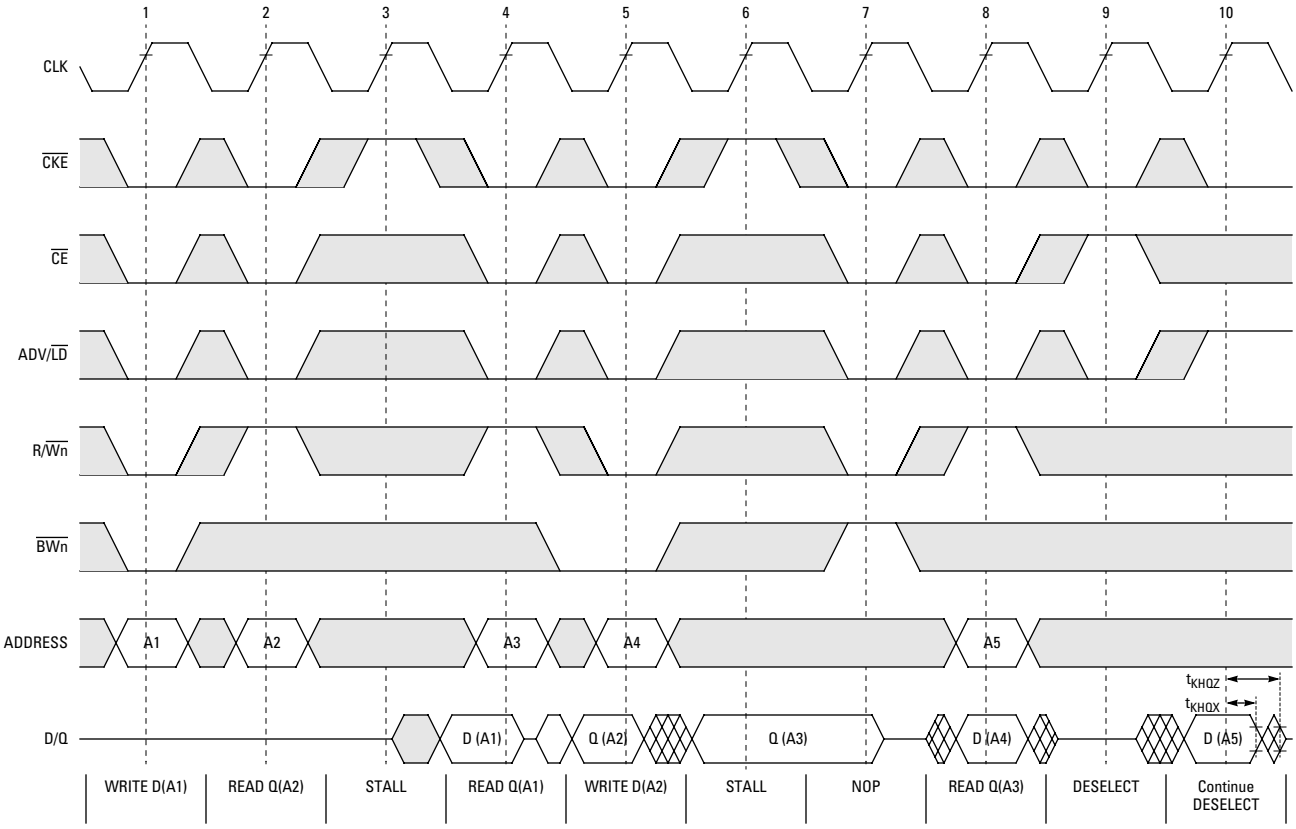
Input Conditions	Access Time
$t_{RAD} \leq t_{RAD}$ (max.) and $t_{RCD} \leq t_{RCD}$ (max.)	t_{RAC} (Max.)
t_{RAD} (max.) < t_{RAD} and $t_{RCD} \leq t_{RCD}$ (max.)	t_{AA} (Max.)
t_{RCD} (max). < t_{RCD}	t_{CAC} (Max.)

   t_{RAD} (max.) and t_{RCD} (max.) indicate the points which the access time changes and are not the limits of operation.
5. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
6. t_{CRP} (min.) requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycle preceded by any cycles.
7. Either t_{RCH} (min.) or t_{RRH} (min) must be satisfied for a read cycle.
8. t_{WP} (min.) is applicable for late write cycle or read modify write cycle. In early write cycles, t_{WCH} (min.) should be satisfied.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
10. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write orr read modify write cycles.
11. t_{AR}, t_{WCR}, and t_{DHR} are referenced to t_{RAD}(max.).



NOTE:
1. For this waveform, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE represents three signals. When $\overline{CE}$ = 0, it represents $\overline{CE}$ = 0, $\overline{CE2}$ = 0, $\overline{CE2}$ = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

Figure 2. Read/Write Timing



NOTE:
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates $\overline{CKE}$ being used to create a "pause." A WRITE is not performed during this cycle.
2. For this waveform, ZZ and $\overline{OE}$ are tied LOW.
3. $\overline{CE}$ represents three signals. When $\overline{CE}$ = 0, it represents $\overline{CE}$ = 0, $\overline{CE2}$ = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

Figure 3. NOP, STALL and DESELECT Timing

PACKAGING INFORMATION

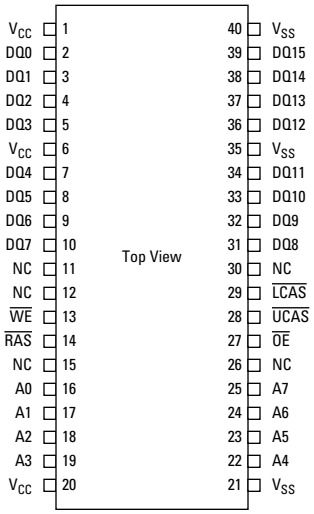


Figure 4. 40-Pin 400 mil Plastic SOJ Pin Assignment

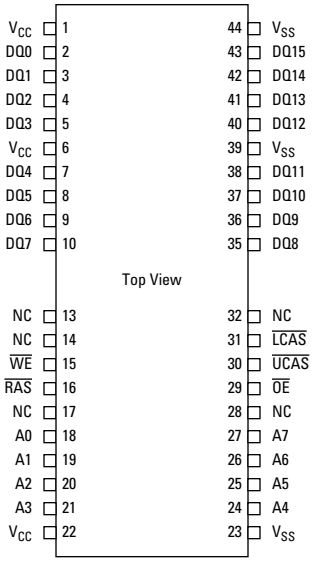
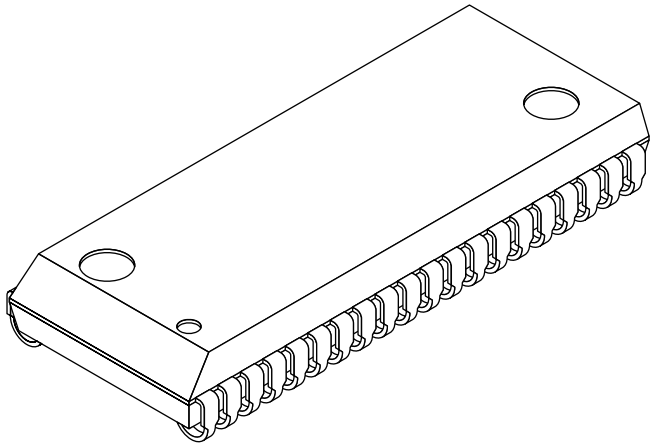


Figure 5. 44/40-Pin 400 mil TSOP (TypeII) Pin Assignment



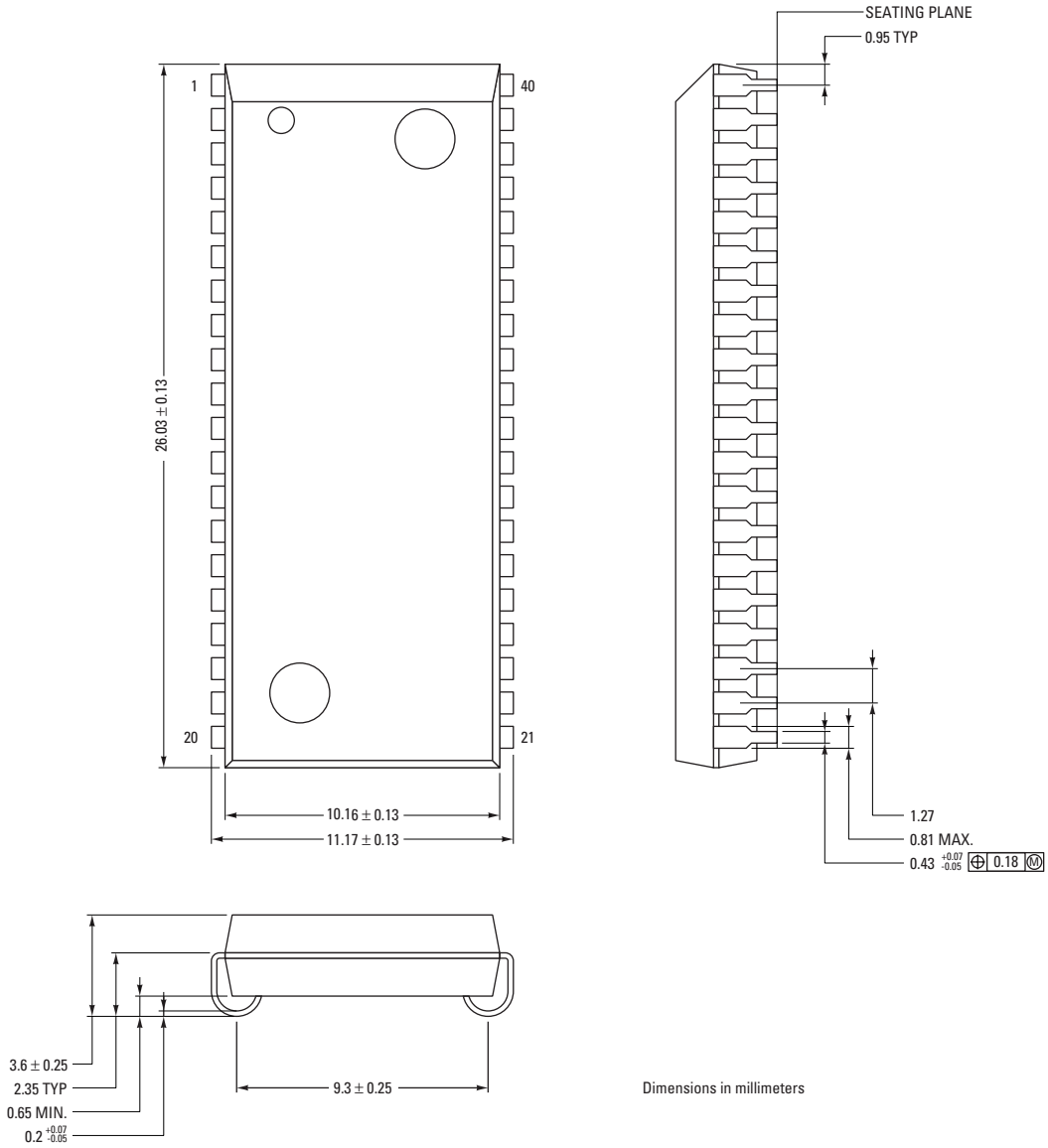
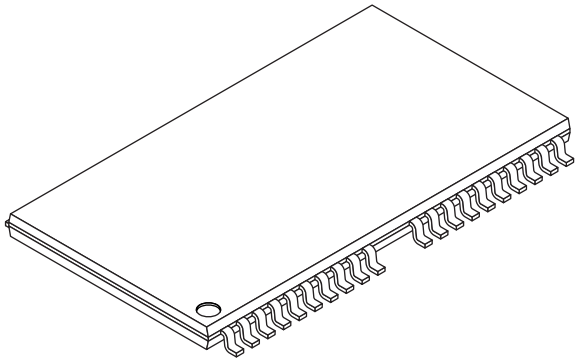


Figure 6. 40-Pin 400 mil SOJ Package Dimensions



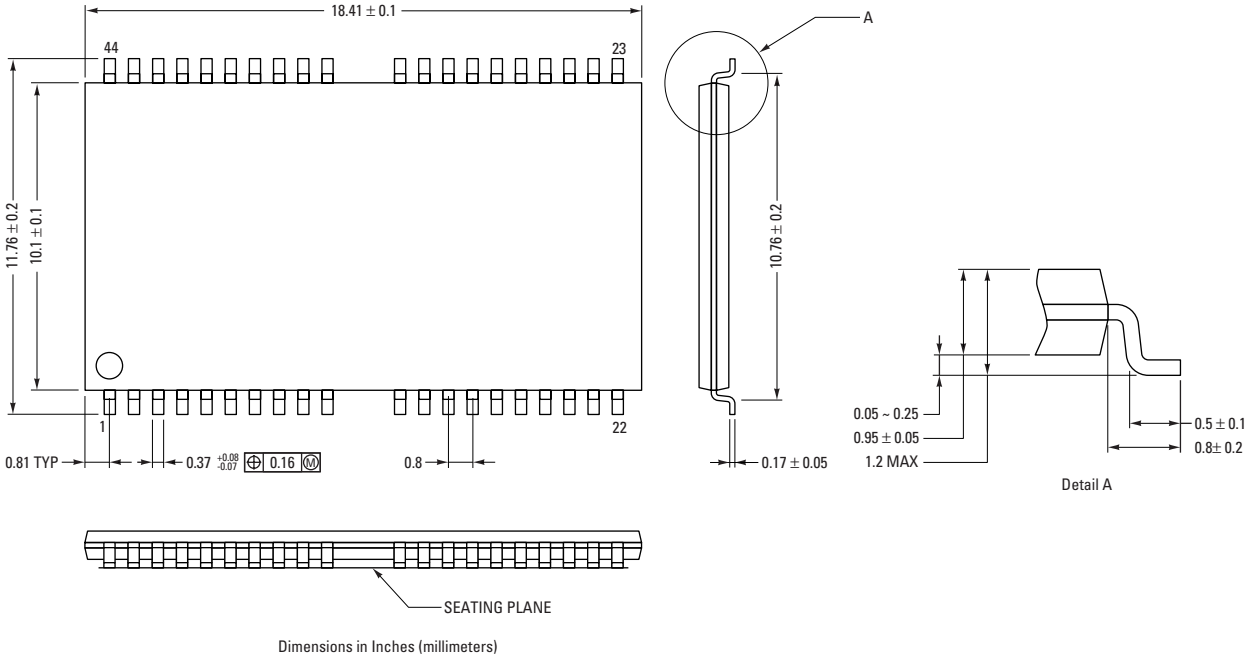


Figure 7. 40/44-Pin TSOP (Type II) Package Dimensions

Ordering Info

Part Number	Speed	Power	Feature	Package
GLT4116-30J4	30 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT4116-35J4	35 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT4116-40J4	40 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT4116-45J4	45 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT4116-30TC	30 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT4116-35TC	35 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT4116-40TC	40 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT4116-45TC	45 ns	Normal	FPM	44-Pin 400 mil TSOP

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Printed in USA