

## Features

- Double-conversion superhet architecture for high degree of image rejection
- FSK for digital data and FM reception for analog signal transmission
- FSK/FM demodulation with phase-coincidence demodulator
- Low current consumption in active mode and very low standby current
- Switchable LNA gain for improved dynamic range
- RSSI allows signal strength indication and ASK detection

## Ordering Information

### Part No.

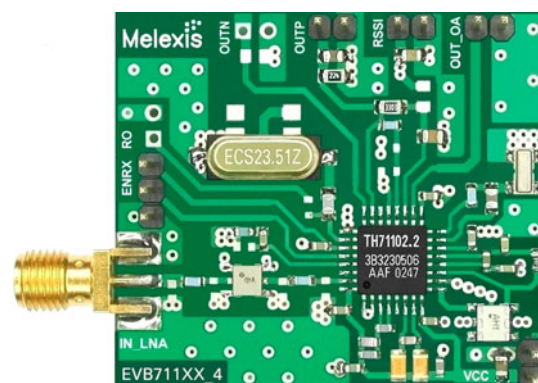
EVB71102-433-FSK-C  
EVB71102-433-ASK-C

EVB71102-315-FSK-C  
EVB71102-315-ASK-C

## Application Examples

- General digital data transmission
- Tire Pressure Monitoring Systems (TPMS)
- Remote Keyless Entry (RKE)
- Wireless access control
- Alarm and security systems
- Garage door openers
- Remote Controls
- Home and building automation
- Low-power telemetry systems

## Evaluation Board



## General Description

The TH71102 FSK/FM/ASK double-conversion superheterodyne receiver IC is designed for applications in the European 433 MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 260 MHz to 510 MHz (e.g. for applications to FCC part 15 and ARIB STD-T67).

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## 1 Theory of Operation

### 1.1 General

With the TH71102 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can also be constituted by a ceramic discriminator with a varactor diode to create an AFC circuit. In ASK configuration, the RSSI signal is fed to an ASK detector, which is constituted by the operational amplifier.

The superheterodyne configuration is double conversion where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a high degree of image rejection, achieved in conjunction with an RF front-end filter. Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

A single-conversion variant, called TH71101, is also available. Both Receiver ICs have the same die. At the TH71101 the second mixer MIX2 operates as an amplifier.

The TH71102 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2, parts of the PLL SYNTH are: the high-frequency VCO1, the feedback dividers DIV\_8 and DIV\_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
- Second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
- IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

### 1.2 EVB Technical Data Overview

- |   |   |
|---|---|
| <input type="checkbox"/> Input frequency range: 260 MHz to 510 MHz                            | <input type="checkbox"/> Range of first IF2: 400 kHz to 22 MHz  |
| <input type="checkbox"/> Power supply range: 2.3 V to 5.5 V @ ASK<br>2.7 V to 5.5 V @ FSK     | <input type="checkbox"/> Maximum input level: -10 dBm @ ASK<br>0 dBm @ FSK  |
| <input type="checkbox"/> Temperature range: -40 °C to +85 °C                                  | <input type="checkbox"/> Image rejection: > 65 dB (e.g. with 433.92 MHz SAW front-end filter and at 10.7 MHz IF2) |
| <input type="checkbox"/> Standby current: 50 nA   | <input type="checkbox"/> Spurious emission: < -70 dBm   |
| <input type="checkbox"/> Operating current: 6.5 mA @ low gain mode<br>8.2 mA @ high gain mode | <input type="checkbox"/> Input frequency acceptance range: up to $\pm 100$ kHz                                    |
| <input type="checkbox"/> Sensitivity: -110 dBm @ ASK 1)<br>-104 dBm @ FSK 2)                  | <input type="checkbox"/> RSSI range: 70 dB  |
| <input type="checkbox"/> Range of first IF1: 10 MHz to 80 MHz                                 | <input type="checkbox"/> FM/FSK deviation range: $\pm 2.5$ kHz to $\pm 80$ kHz                                    |
|   | <input type="checkbox"/> Maximum analog modulation frequency: 15 kHz  |

- 1) at 4 kbps NRZ, BER =  $3 \cdot 10^{-3}$ , 180 kHz IF filter BW, incl. 3 dB SAW front-end-filter loss
- 2) at 4 kbps NRZ, BER =  $3 \cdot 10^{-3}$ ,  $\pm 20$  kHz FSK deviation, 180 kHz IF filter BW, incl. 3 dB SAW front-end-filter loss

For more detailed information, please refer to the latest TH71102 data sheet revision

### 1.3 Block Diagram

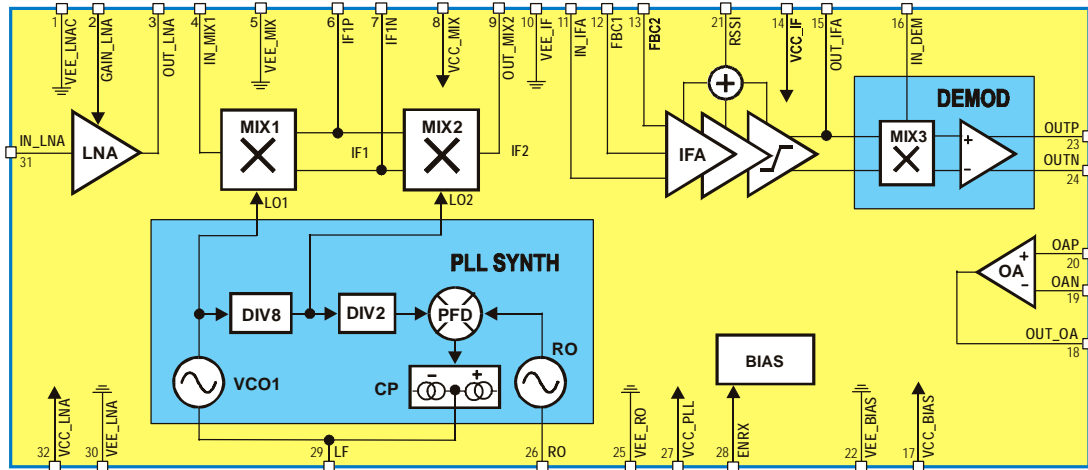


Fig. 1: TH71102 block diagram

### 1.4 Mode Configurations

ENRX	Mode	Description
0	RX standby	RX disabled
1	RX active	RX enable

**Note:** ENRX are pulled down internally

### 1.5 LNA GAIN Control

V <sub>GAIN_LNA</sub>	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain
> 1.4 V	LOW GAIN	LNA set to low gain

**Note:** hysteresis between gain modes to ensure stability

### 1.6 Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that can be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver's double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH71102 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of  $N1 = 8$  (DIV\_8) and  $N2 = 2$  (DIV\_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (low-low), LO1 low-side and LO2 high-side (low-high), LO1 high-side and LO2 low-side (high-low) or LO1 and LO2 high-side (high-high). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

Injection type	high-high	low-low	high-low	low-high
REF	$(RF - IF2)/14$	$(RF - IF2)/18$	$(RF + IF2)/14$	$(RF + IF2)/18$
LO1	$16 \bullet REF$	$16 \bullet REF$	$16 \bullet REF$	$16 \bullet REF$
IF1	$LO1 - RF$	$RF - LO1$	$LO1 - RF$	$RF - LO1$
LO2	$2 \bullet REF$	$2 \bullet REF$	$2 \bullet REF$	$2 \bullet REF$
IF2	$LO2 - IF1$	$IF1 - LO2$	$IF1 - LO2$	$LO2 - IF1$

### 1.6.1 Selected Frequency Plans

The following table depicts crystal, LO and image signals considering the examples of 315 MHz and 433.92 MHz RF reception at  $IF2 = 10.7$  MHz. The columns in bold depict the selected frequency plans to receive at 315 MHz and 433.92 MHz, respectively.

Signal type	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 433.92 MHz	RF = 433.92 MHz	RF = 433.92 MHz	RF = 433.92 MHz
Injection type	high-high	low-low	<b>high-low</b>	low-high	high-high	<b>low-low</b>	high-low	low-high
REF / MHz	21.73571	16.90556	<b>23.26429</b>	18.09444	30.23000	<b>23.51222</b>	31.75857	24.70111
LO1 / MHz	347.77143	270.48889	<b>372.22857</b>	289.51111	483.68000	<b>376.19556</b>	508.13714	395.21778
IF1 / MHz	32.77143	44.51111	<b>57.22857</b>	25.48889	49.76000	<b>57.72444</b>	74.21714	38.70222
LO2 / MHz	43.47143	33.81111	<b>46.52857</b>	36.18889	60.46000	<b>47.02444</b>	63.51714	49.40222
RF image/MHz	380.54286	225.97778	<b>429.45714</b>	264.02222	533.44000	<b>318.47112</b>	582.35428	356.51556
IF1 image/MHz	54.17143	23.11111	<b>35.82857</b>	46.88889	71.16000	<b>36.32444</b>	52.81717	60.10222

### 1.6.2 Maximum Frequency Coverage

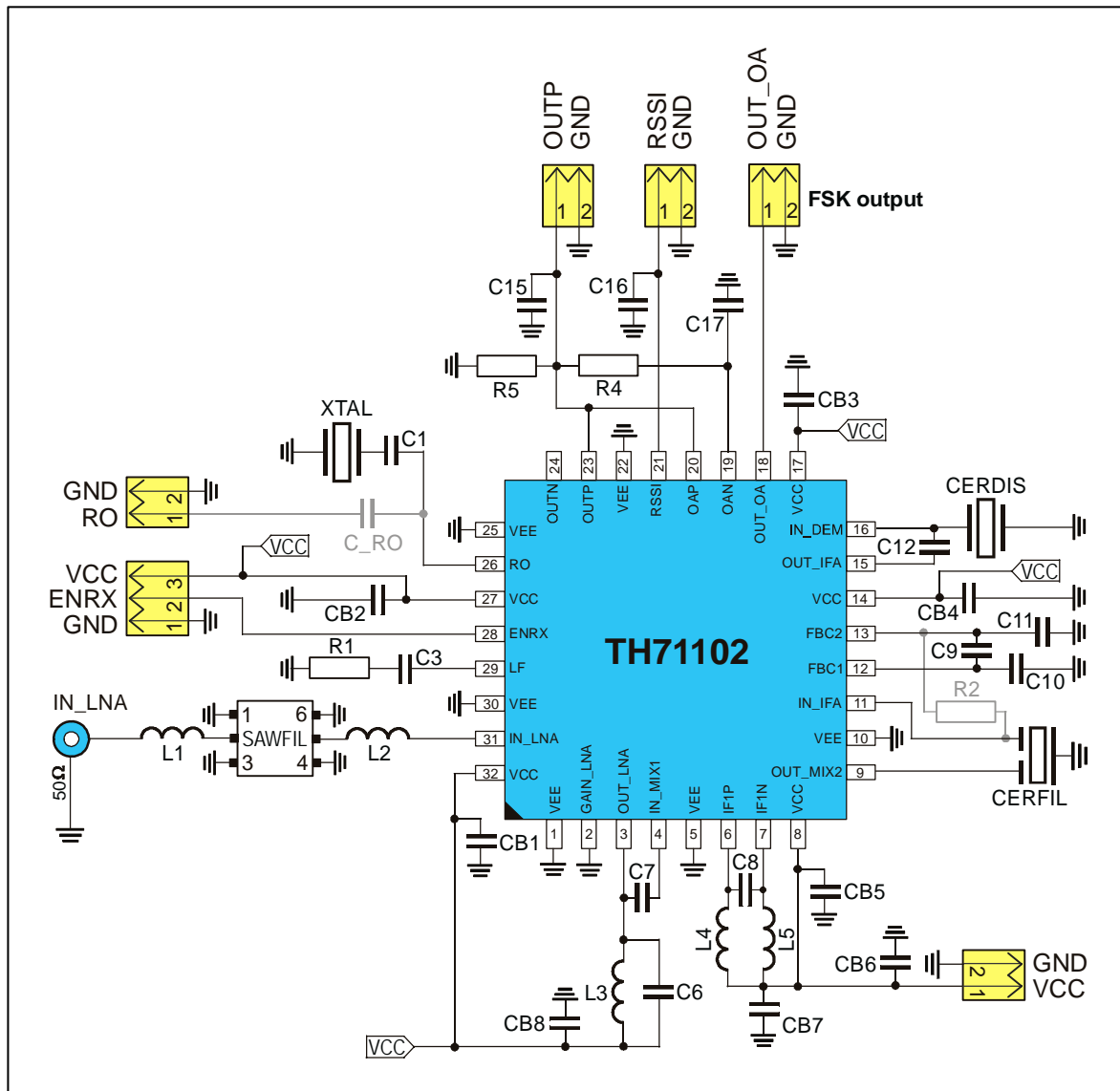
Parameter	$f_{min}$	$f_{max}$
Injection type	high-low	low-low
RF / MHz	251.8	516.95
REF / MHz	18.75	28.125
LO1 / MHz	300	450
IF1 / MHz	48.2	66.95
LO2 / MHz	37.5	56.25
IF2 / MHz	10.7	10.7

The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 300 MHz to 450 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection.

## 2 Application Circuits

### 2.1 FSK Application Circuit

#### 2.1.1 Circuit Diagram for FSK Reception



#### Circuit Features

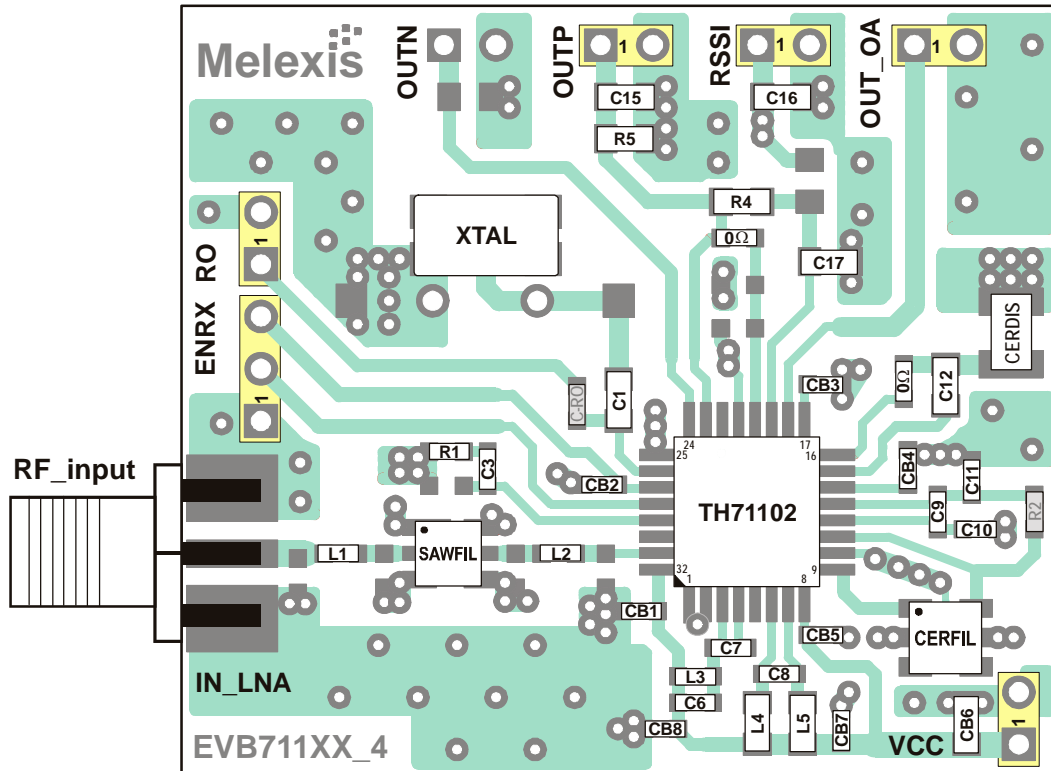
- Tolerates input frequency variations
- Well-suited for NRZ, Manchester and similar codes

### 2.1.2 Board Component Values for FSK

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Tolerance	Description
C1	0805	27 pF	27 pF	±5%	crystal series capacitor
C3	0603	1 nF	1 nF	±10%	loop filter capacitor
C6	0603	6.8 pF	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.7 pF	2.2 pF	±5%	MIX1 input matching capacitor
C8	0603	27 pF	27 pF	±5%	IF1 tank capacitor
C9	0603	33 nF	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C12	0805	10 pF	10 pF	±5%	DEMODO phase-shift capacitor
C15	0805	100 pF	100 pF	±5%	demodulator output low-pass capacitor, this value for data rates < 20 kbps NRZ, for higher data rates decrease the value
C16	0805	1.5 nF	1.5 nF	±10%	RSSI output low-pass capacitor
C17	0805	10 nF	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ, for lower data rates increase the value
CB1 to CB5 CB7 to CB8	0603	330 pF	330 pF	±10%	de-coupling capacitor
CB6	0805	33 nF	33 nF	±10%	de-coupling capacitor
C_RO	0603	330 pF	330 pF	±5%	optional capacitor, to couple external RO signal
R1	0805	10 kΩ	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	330 kΩ	±5%	data slicer resistor
R5	0805	220 kΩ	220 kΩ	±5%	loading resistor
L1	0603	0 Ω	68 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	33 nH	82 nH	±5%	
L3	0603	22 nH	15 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L4	0603	100 nH	100 nH	±5%	IF1 tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L5	0603	100 nH	100 nH	±5%	
XTAL	SMD 6x3.5	23.26429 MHz @ RF = 315 MHz	23.51222 MHz @ RF = 433.92 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon (HEX22 series) or equivalent part
	HC49 SMD				fundamental-mode crystal, C <sub>load</sub> = 10 pF to 15pF, C <sub>0,max</sub> = 7 pF, R <sub>1,max</sub> = 50 Ω
SAWFIL	SMD 3x3		SAFCC433MBL0X00 (f <sub>0</sub> = 433.92 MHz)	B <sub>3dB</sub> = 840 kHz	low-loss SAW filter from Murata or equivalent part
		SAFDC315MSM0T00 (f <sub>0</sub> = 315.00 MHz)		B <sub>3dB</sub> = 5MHz	
CERFIL	SMD 3.45x3.1	SFECF10M7HA00		B <sub>3dB</sub> = 180 kHz	ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA135			ceramic discriminator from Murata, or equivalent part

2.1.3 Component Arrangement Top Side for FSK Reception

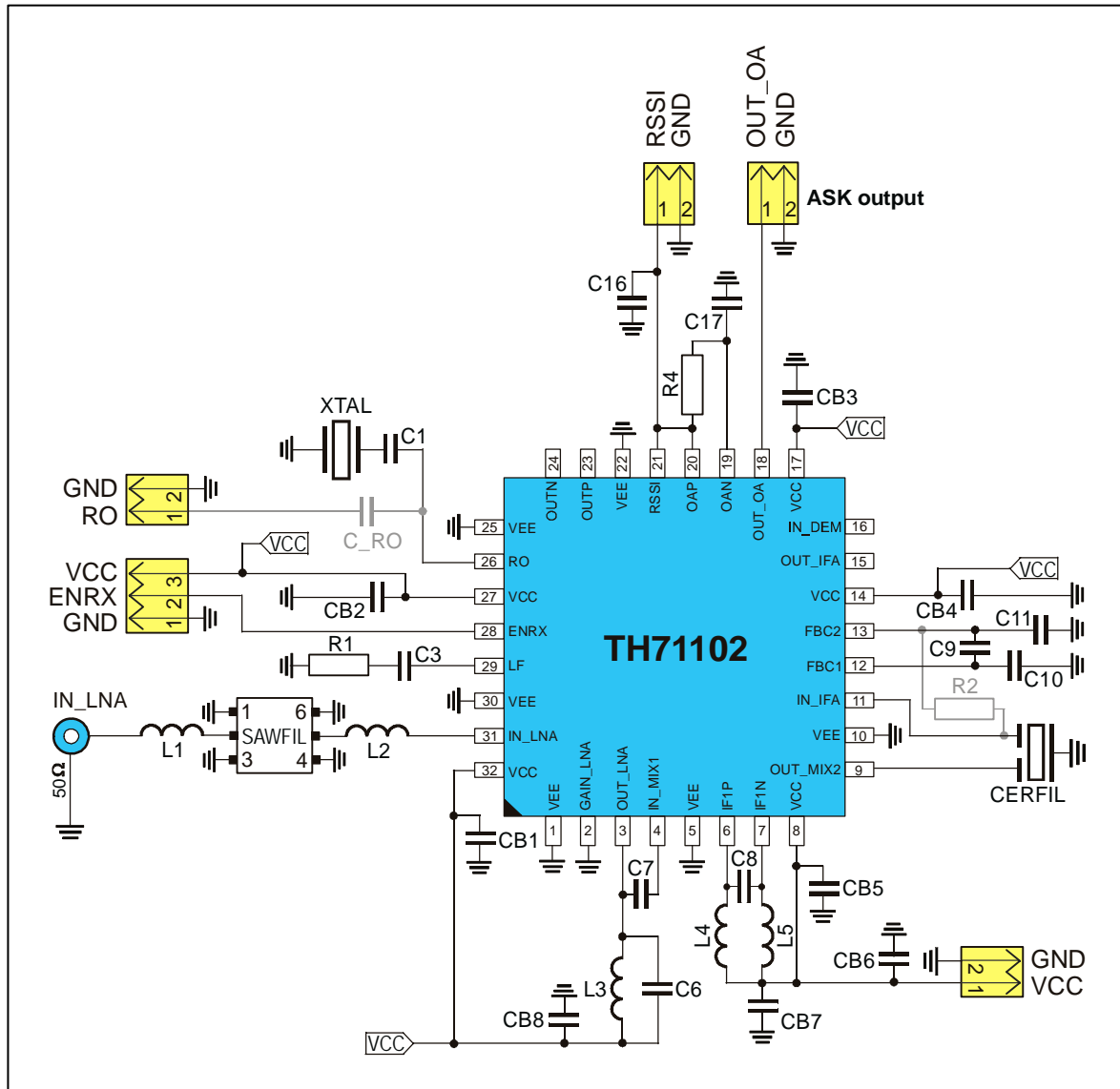
Board size is 42.7mm x 37.5mm





## 2.2 ASK Application Circuit

### 2.2.1 Circuit Diagram for ASK Reception

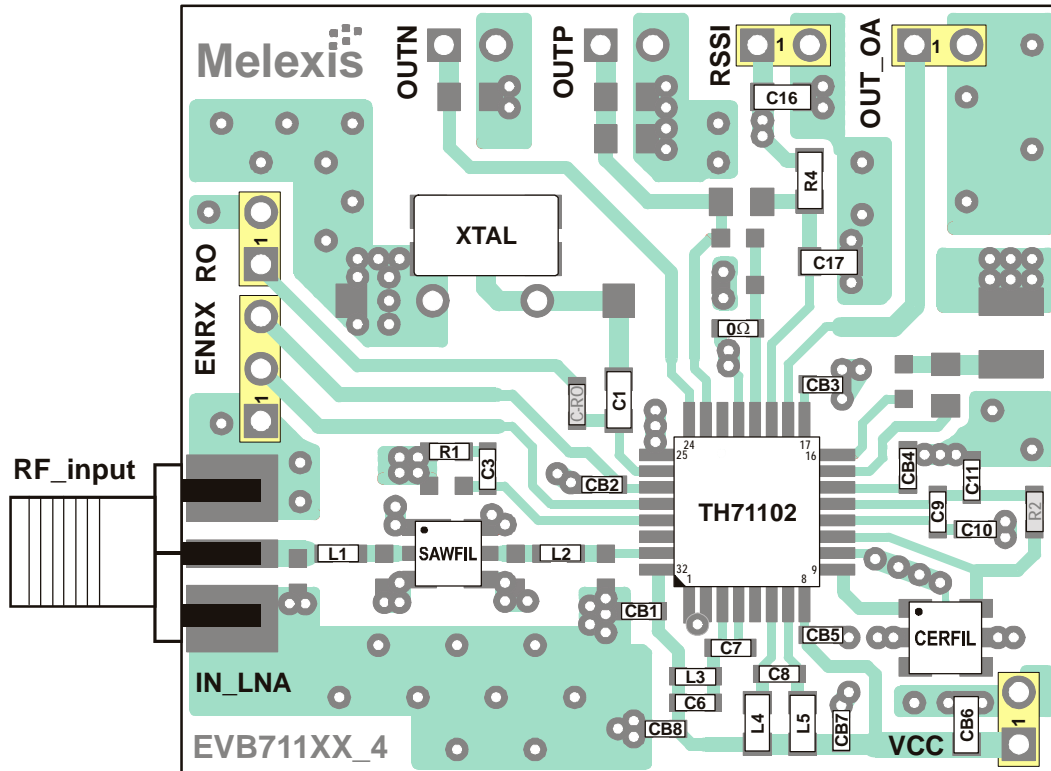


### 2.2.2 Board Component Values for ASK

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Tolerance	Description
C1	0805	27 pF	27 pF	±5%	crystal series capacitor
C3	0603	1 nF	1 nF	±10%	loop filter capacitor
C6	0603	6.8 pF	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.7 pF	2.2 pF	±5%	MIX1 input matching capacitor
C8	0603	27 pF	27 pF	±5%	IF1 tank capacitor
C9	0603	33 nF	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C16	0805	1.5 nF	1.5 nF	±10%	RSSI output low-pass capacitor, this value for data rates < 10 kbps NRZ, for higher data rates decrease the value
C17	0805	10 nF	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ, for lower data rates increase the value
CB1 to CB5 CB7 to CB8	0603	330 pF	330 pF	±10%	de-coupling capacitor
CB6	0805	33 nF	33 nF	±10%	de-coupling capacitor
C_RO	0603	330 pF	330 pF	±5%	optional capacitor, to couple external RO signal
R1	0805	10 kΩ	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	330 kΩ	±5%	data slicer resistor
L1	0603	0 Ω	68 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	33 nH	82 nH	±5%	
L3	0603	22 nH	15 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L4	0603	100 nH	100 nH	±5%	IF1 tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L5	0603	100 nH	100 nH	±5%	
XTAL	SMD 6x3.5	23.26429 MHz @ RF = 315 MHz	23.51222 MHz @ RF = 433.92 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon (HEX22 series) or equivalent part
	HC49 SMD				fundamental-mode crystal, C <sub>load</sub> = 10 pF to 15pF, C <sub>0, max</sub> = 7 pF, R <sub>1, max</sub> = 50 Ω
SAWFIL	SMD 3x3		SAFCC433MBLOX00 (f <sub>0</sub> = 433.92 MHz)	B <sub>3dB</sub> = 840 kHz	low-loss SAW filters from Murata or equivalent part
		SAFDC315MSM0T00 (f <sub>0</sub> = 315.00 MHz)		B <sub>3dB</sub> = 5MHz	
CERFIL	SMD 3.45x3.1	SFECF10M7HA00		B <sub>3dB</sub> = 180 kHz	ceramic filter from Murata, or equivalent part


2.2.3 Component Arrangement Top Side for ASK Reception

Board size is 42.7mm x 37.5mm





### 5 Package Description

 The device TH71102 is RoHS compliant.

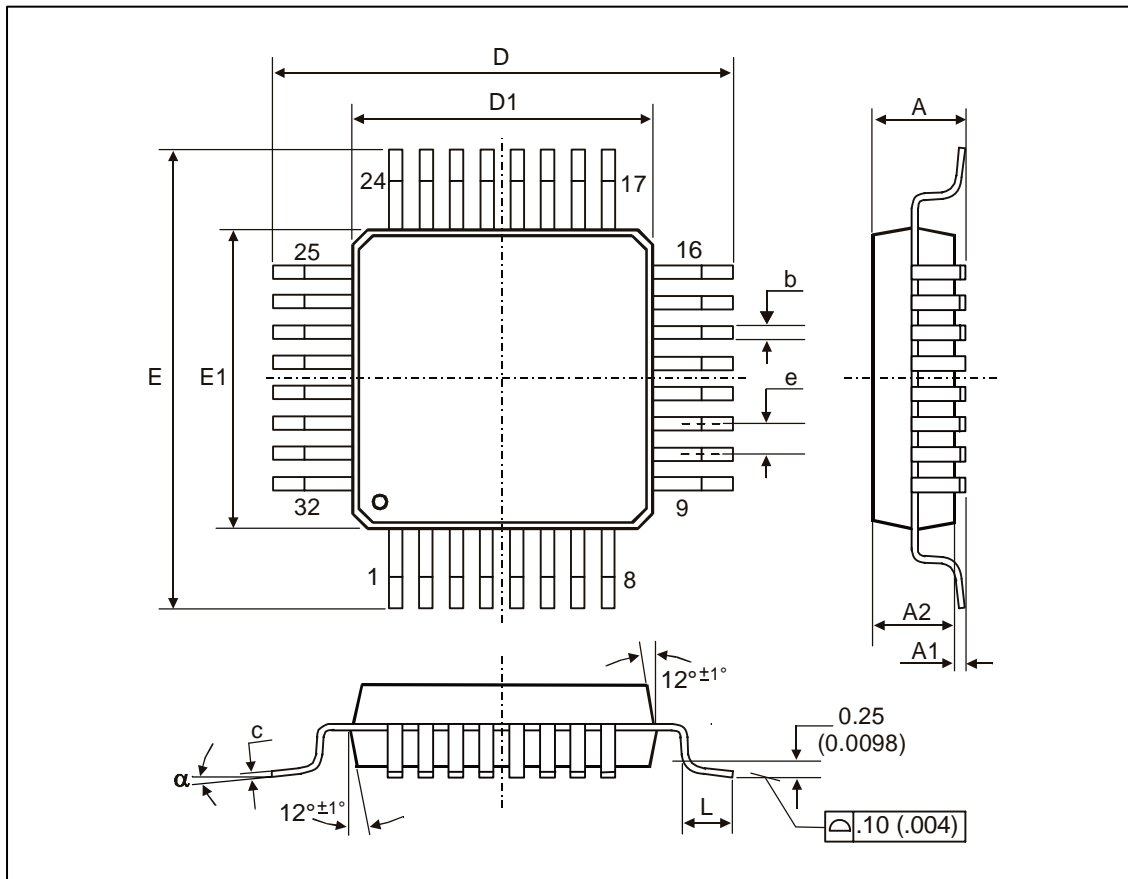


Fig. 2: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	E, D	A	A1	A2	e	b	c	L	$\alpha$
min	7.00	9.00	1.40	0.05	1.35	0.8	0.30	0.09	0.45	0°
max			1.60	0.15	1.45		0.45	0.20	0.75	7°
All Dimension in inch, coplanarity < 0.004"										
min	0.276	0.354	0.055	0.002	0.053	0.031	0.012	0.0035	0.018	0°
max			0.063	0.006	0.057		0.018	0.0079	0.030	7°

#### 5.1 Soldering Information

- The device TH71102 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-2.

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