DLP2010 (0.2 WVGA DMD)

1 Features

- 0.2-Inch (5.29-mm) Diagonal Micromirror Array
  - 854 × 480 Array of Aluminum Micrometer-Sized Mirrors, in an Orthogonal Layout
  - 5.4 – Micron Micromirror Pitch
  - ±17° Micromirror Tilt (Relative to Flat Surface)
  - Side Illumination for Optimal Efficiency and Optical Engine Size
  - Polarization Independent Aluminum Micromirror Surface
- 4-Bit SubLVDS Input Data Bus
- 15.9-mm × 5.3-mm × 4-mm Package Size
- Dedicated DLPC3430 or DLPC3435 Display Controller and DLPA2000 PMIC/LED Driver for Reliable Operation

2 Applications

- Embedded Projector:
  - Smart Phone
  - Tablet
  - Camera
  - Camcorder
  - Laptop
- Battery Powered Mobile Accessory
- Wearable (Near–Eye) Display
- Interactive Display
- Low Latency Gaming Display
- Digital Signage

3 Description

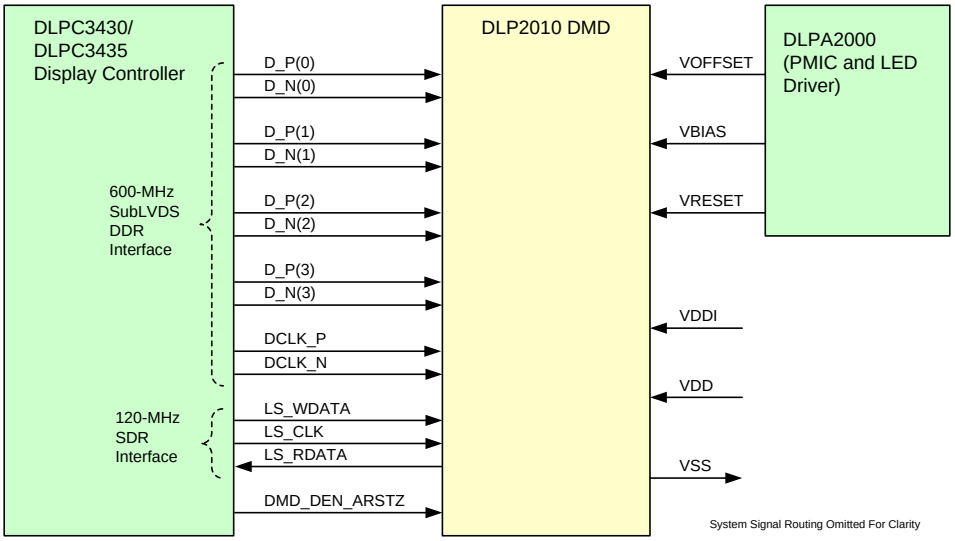
The DLP2010 digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP2010 DMD displays a very crisp and high quality image or video. DLP2010 is part of the chipset comprising of the DLP2010 DMD, DLPC3430 or DLPC3435 display controller and DLPA2000 PMIC/LED driver. The compact physical size of the DLP2010 is well-suited for portable equipment where small form factor and low power is important. The compact package compliments the small size of LEDs to enable highly efficient, robust light engines.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP2010	CLGA (40)	15.90 × 5.30 × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DLP® DLP2010 (0.2 WVGA) Chipset



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

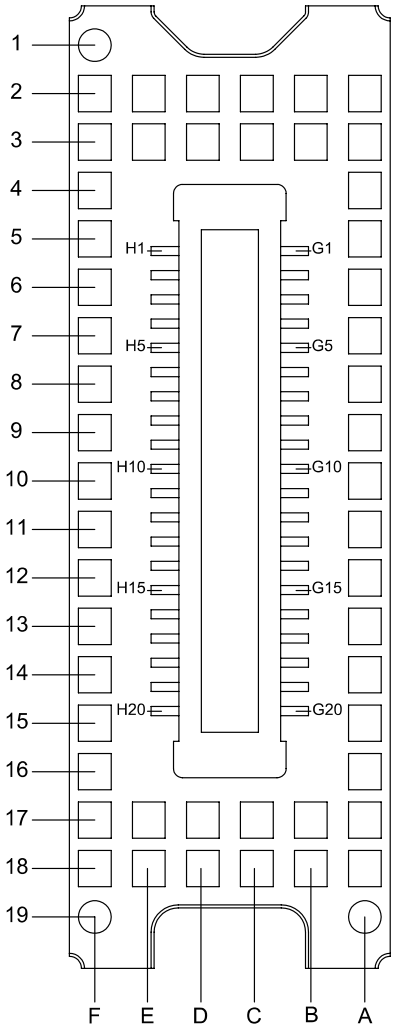
Changes from Original (July 2014) to Revision A **Page**

- All VSS pins changed from Power to GND. ... 4
- Added Storage Conditions table. ... 6
- Updated the VID spec to align with .3 720p. ... 7
- Lowered minimum delay time ... 31

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5 Pin Configuration and Functions

FQJ Package
40-Pin CLGA
Bottom View



Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	G4	I	SubLVDS	Double	Data, Negative	7.03
D_P(0)	G3	I	SubLVDS	Double	Data, Positive	7.03
D_N(1)	G8	I	SubLVDS	Double	Data, Negative	7.03
D_P(1)	G7	I	SubLVDS	Double	Data, Positive	7.03
D_N(2)	H5	I	SubLVDS	Double	Data, Negative	7.02
D_P(2)	H6	I	SubLVDS	Double	Data, Positive	7.02

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQJ ceramic package is 9.8.
Propagation speed = 11.8 / sqrt(9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

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Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
D_N(3)	H1	I	SubLVDS	Double	Data, Negative	7.00
D_P(3)	H2	I	SubLVDS	Double	Data, Positive	7.00
DCLK_N	H9	I	SubLVDS	Double	Clock, Negative	7.03
DCLK_P	H10	I	SubLVDS	Double	Clock, Positive	7.03
CONTROL INPUTS						
DMD_DEN_ARSTZ	G12	I	LPSDR[1]		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	5.72
LS_CLK	G19	I	LPSDR	Single	Clock for low-speed interface	3.54
LS_WDATA	G18	I	LPSDR	Single	Write data for low-speed interface	3.54
LS_RDATA	G11	O	LPSDR	Single	Read data for low-speed interface	8.11
POWER						
VBIAS[3]	H17	Power			Supply voltage for positive bias level at micromirrors	
VOFFSET[3]	H13	Power			Supply voltage for HVCMOS core logic. Includes: supply voltage for stepped high level at micromirror address electrodes and supply voltage for offset level at micromirrors	
VRESET[3]	H18	Power			Supply voltage for negative reset level at micromirrors	
VDD[3]	G20	Power			Supply voltage for micromirror low voltage CMOS core logic includes supply voltage for LPSDR inputs and supply voltage for normal high level at micromirror address electrodes.	
VDD	H14	Power				
VDD	H15	Power				
VDD	H16	Power				
VDD	H19	Power				
VDD	H20	Power				
VDDI[3]	G1	Power			Supply voltage for SubLVDS receivers	
VDDI	G2	Power				
VDDI	G5	Power				
VDDI	G6	Power				
VSS[3]	G9	Ground			Ground. Common return for all power.	
VSS	G10	Ground				
VSS	G13	Ground				
VSS	G14	Ground				
VSS	G15	Ground				
VSS	G16	Ground				
VSS	G17	Ground				
VSS	H3	Ground				
VSS	H4	Ground				
VSS	H7	Ground				
VSS	H8	Ground				
VSS	H11	Ground				
VSS	H12	Ground				

(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

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Pin Functions – Test Pads

NUMBER	SYSTEM BOARD	NUMBER	SYSTEM BOARD
A2	Do not connect	D2	Do not connect
A3	Do not connect	D3	Do not connect
A4	Do not connect	D17	Do not connect
A5	Do not connect	D18	Do not connect
A6	Do not connect		
A7	Do not connect	E2	Do not connect
A8	Do not connect	E3	Do not connect
A9	Do not connect	E17	Do not connect
A10	Do not connect	E18	Do not connect
A11	Do not connect		
A12	Do not connect	F1	Do not connect
A13	Do not connect	F2	Do not connect
A14	Do not connect	F3	Do not connect
A15	Do not connect	F4	Do not connect
A16	Do not connect	F5	Do not connect
A17	Do not connect	F6	Do not connect
A18	Do not connect	F7	Do not connect
A19	Do not connect	F8	Do not connect
		F9	Do not connect
B2	Do not connect	F10	Do not connect
B3	Do not connect	F11	Do not connect
B17	Do not connect	F12	Do not connect
B18	Do not connect	F13	Do not connect
		F14	Do not connect
C2	Do not connect	F15	Do not connect
C3	Do not connect	F16	Do not connect
C17	Do not connect	F17	Do not connect
C18	Do not connect	F18	Do not connect
		F19	Do not connect

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6 Specifications

6.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic(2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers(2)	–0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode(2)(3)	–0.5	10.6	V
	VBIAS	Supply voltage for micromirror electrode(2)	–0.5	19	V
	VRESET	Supply voltage for micromirror electrode(2)	–15	0.3	V
	| VDDI–VDD |	Supply voltage delta (absolute value)(4)		0.3	V
	| VBIAS–VOFFSET |	Supply voltage delta (absolute value)(5)		11	V
	| VBIAS–VRESET |	Supply voltage delta (absolute value)(6)		34	V
Input voltage	Input voltage for other inputs LPSDR(2)		–0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS(2)(7)		–0.5	VDDI + 0.5	V
Input pins	| VID |	SubLVDS input differential voltage (absolute value)(7)		810	mV
	IID	SubLVDS input differential current		8.1	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational(8)	–20	90	°C
		Temperature – non-operational(8)	–40	90	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(9)		30	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operation Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated by the *Micromirror Array Temperature Calculation)*, or of any point along the Window Edge as defined in Figure 18. The locations of thermal test points TP2 and TP3 in Figure 18 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 18. The window test points TP2 and TP3 shown in Figure 18 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable before the DMD is installed in the final product.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	-40	85	°C
T_{DP}	Storage dew point - long-term(1)		24	
	Storage dew point - short-term(2)		28	

(1) Long-term is defined as the usable life of the device.
(2) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

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6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE (4)					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (5)	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
|VDDI–VDD|	Supply voltage delta (absolute value) (6)			0.3	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value) (7)			10.5	V
|VBIAS–VRESET|	Supply voltage delta (absolute value) (8)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK (9)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK (10)	300		600	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE (10)					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) Figure 8 , Figure 9	150	250	350	mV
V_{CM}	Common mode voltage Figure 8 , Figure 9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage Figure 8, Figure 9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance Figure 10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

(1) **Recommended Operating Conditions** are applicable after the DMD is installed in the final product.
(2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the **Recommended Operating Conditions**. No level of performance is implied when operating the device above or below the **Recommended Operating Conditions** limits.
(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(4) All voltage values are with respect to the ground pins (VSS).
(5) VOFFSET supply transients must fall within specified max voltages.
(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(10) Refer to the SubLVDS timing requirements in *Timing Requirements*.

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(11)(12)(13)	0		40 to 70(13)	°C
	Array Temperature – short-term operational(12)(14)	–20		75	
T_{WINDOW}	Window temperature – operational(11)(15)			90	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (16)			30	°C
ILL_{UV}	Illumination wavelengths < 400 nm (11)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 400 nm and 700 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths >700 nm			10	mW/cm^2

(11) Simultaneous exposure of the DMD to the maximum **Recommended Operating Conditions** for temperature and UV illumination will reduce device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 18 and the **Package Thermal Resistance** using *Micromirror Array Temperature Calculation*.
(13) Per Figure 1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(14) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours for temperatures between long-term maximum and 75°C, less than 500 hours for temperatures between 0°C and -10°C, and less than 25 hours for temperatures between -10°C and -20°C.
(15) Window temperature is the highest temperature on the window edge shown in Figure 18. The locations of thermal test points TP2 and TP3 in Figure 18 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 18 . The window test points TP2 and TP3 shown in Figure 18 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

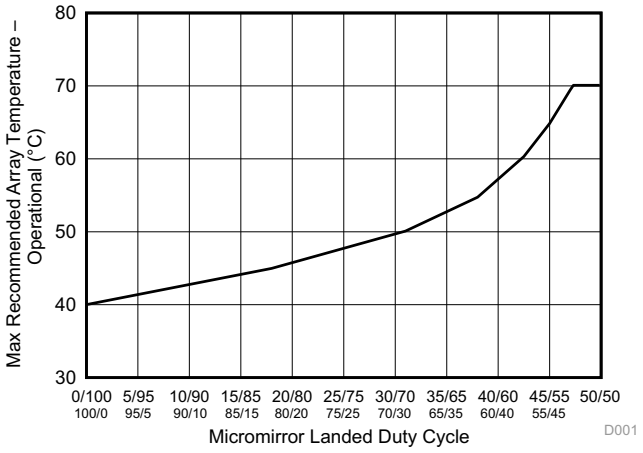


Figure 1. Max Recommended Array Temperature – Derating Curve

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6.5 Thermal Information

THERMAL METRIC[1]	FQJ (CLGA) 40 PINS			UNIT
	MIN	TYP	MAX	
Thermal resistance Active area to test point 1 (TP1)[1]			7.9	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the **Recommended Operating Conditions**. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD[3][4]	VDD = 1.95 V			34.7	mA
		VDD = 1.8 V		27.5		
I_{DDI}	Supply current: VDDI[3][4]	VDDI = 1.95 V			9.4	mA
		VDD = 1.8 V		6.6		
I_{OFFSET}	Supply current: VOFFSET[5][6]	VOFFSET = 10.5 V			1.7	mA
		VOFFSET = 10 V		0.9		
I_{BIAS}	Supply current: VBIAS[5][6]	VBIAS = 18.5 V			0.4	mA
		VBIAS = 18 V		0.2		
I_{RESET}	Supply current: VRESET[6]	VRESET = –14.5 V			2	mA
		VRESET = –14 V		1.2		
POWER[7]						
P_{DD}	Supply power dissipation: VDD[3][4]	VDD = 1.95 V			67.7	mW
		VDD = 1.8 V		49.5		
P_{DDI}	Supply power dissipation: VDDI[3][4]	VDDI = 1.95 V			18.3	mW
		VDD = 1.8 V		11.9		
P_{OFFSET}	Supply power dissipation: VOFFSET[5][6]	VOFFSET = 10.5 V			17.9	mW
		VOFFSET = 10 V		9		
P_{BIAS}	Supply power dissipation: VBIAS[5][6]	VBIAS = 18.5 V			7.4	mW
		VBIAS = 18 V		3.6		
P_{RESET}	Supply power dissipation: VRESET[6]	VRESET = –14.5 V			29	mW
		VRESET = –14 V		16.8		
P_{TOTAL}	Supply power dissipation: Total			90.8	140.3	mW
LPSDR INPUT[8]						
$V_{IH(DC)}$	DC input high voltage[9]		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage[9]		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage[9]		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage[9]		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	Figure 10	0.1 × VDD		0.4 × VDD	V

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate* (LPDDR) JESD209B.

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (480 × 108) micromirrors	95		113	pF

(10) LPSDR specification is for pin LS_RDATA.

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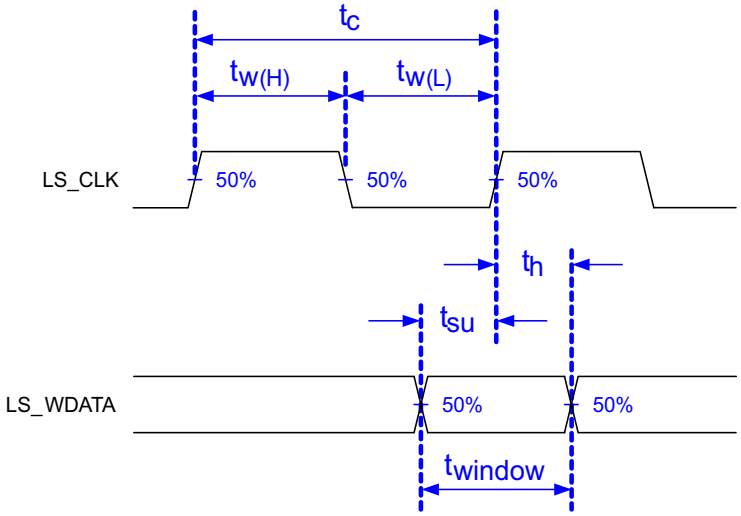
6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_R	Rise slew rate(1)	(30% to 80%) × VDD, Figure 3	1		3	V/ns
t_V	Fall slew rate(1)	(70% to 20%) × VDD, Figure 3	1		3	V/ns
t_R	Rise slew rate(2)	(20% to 80%) × VDD, Figure 3	0.25			V/ns
t_F	Fall slew rate(2)	(80% to 20%) × VDD, Figure 3	0.25			V/ns
t_C	Cycle time LS_CLK,	Figure 2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points,Figure 2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, Figure 2	3.1			ns
t_{SU}	Setup time	LS_WDATA valid before LS_CLK ↑, Figure 2	1.5			ns
t_H	Hold time	LS_WDATA valid after LS_CLK ↑, Figure 2	1.5			ns
t_{WINDOW}	Window time(1)(3)	Setup time + Hold time, Figure 2	3			ns
$t_{DERATING}$	Window time derating(1)(3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, Figure 5		0.35		ns
SubLVDS						
t_R	Rise slew rate	20% to 80% reference points, Figure 4	0.7	1		V/ns
t_F	Fall slew rate	80% to 20% reference points, Figure 4	0.7	1		V/ns
t_C	Cycle time LS_CLK,	Figure 6	1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, Figure 6	0.71			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, Figure 6	0.71			ns
t_{SU}	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, Figure 6				
t_H	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, Figure 6				
t_{WINDOW}	Window time	Setup time + Hold time, Figure 6,Figure 7			0.3	ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

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A. Low-speed interface is LPSDR and adheres to the *Electrical Characteristics* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 2. LPSDR Switching Parameters

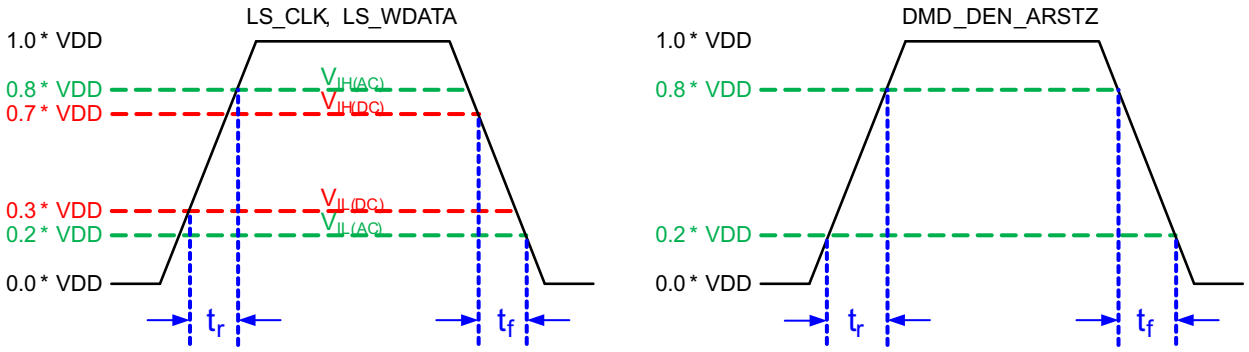


Figure 3. LPSDR Input Rise and Fall Slew Rate

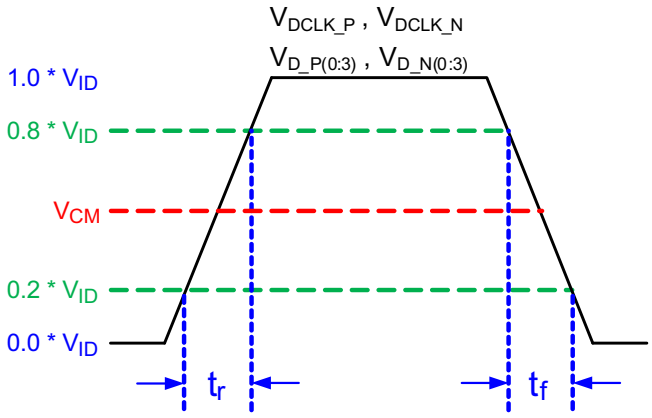


Figure 4. SubLVDS Input Rise and Fall Slew Rate

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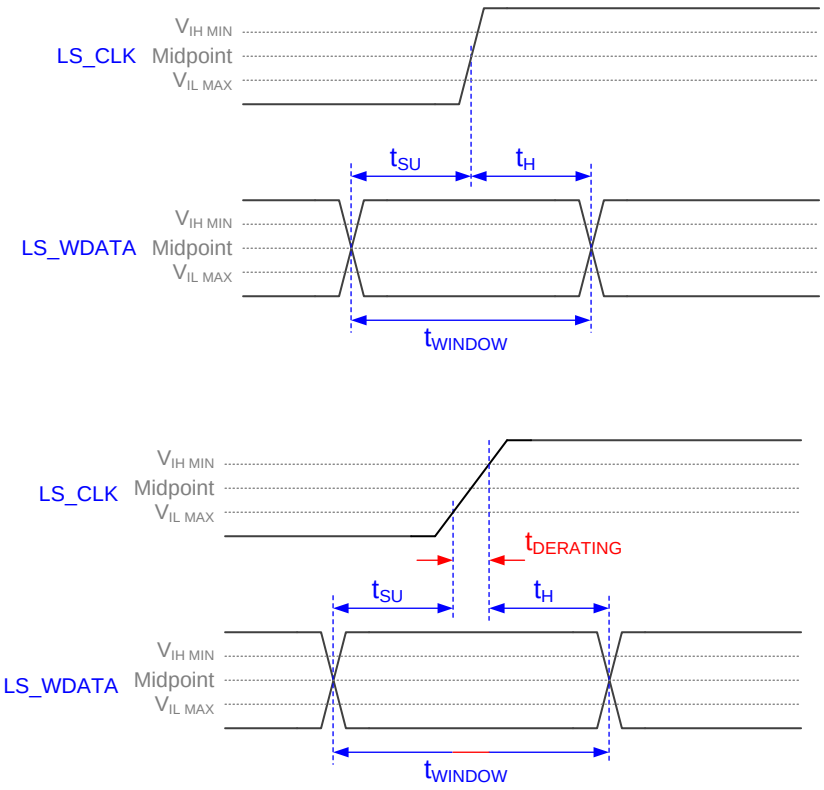


Figure 5. Window Time Derating Concept

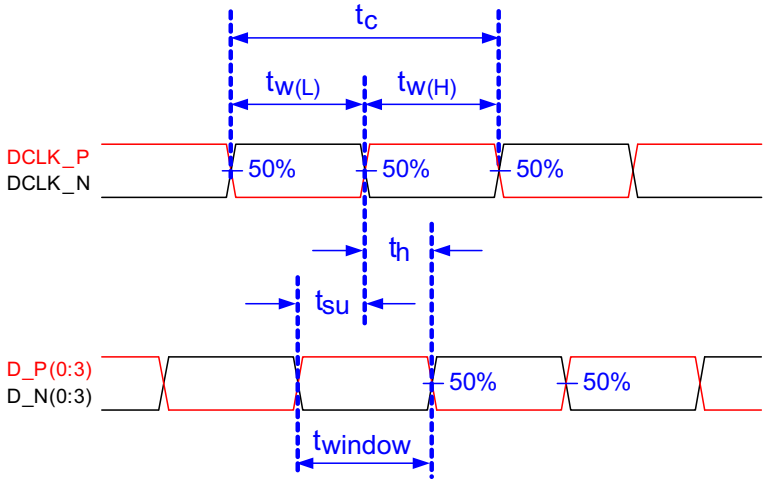
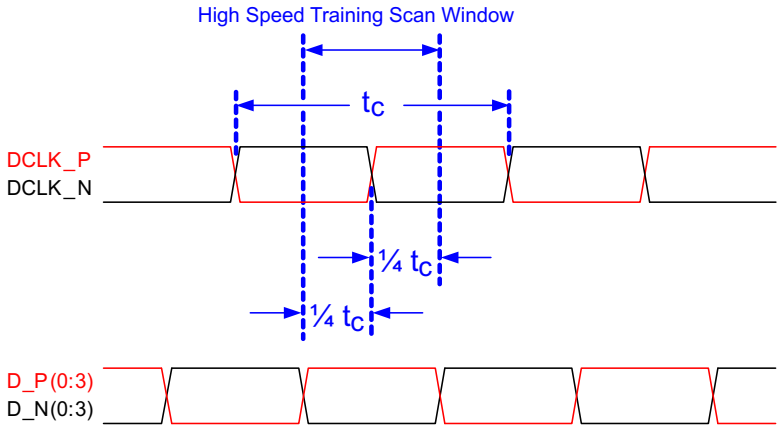


Figure 6. SubLVDS Switching Parameters



Note: Refer to *High-Speed Interface* for details.

Figure 7. High-Speed Training Scan Window

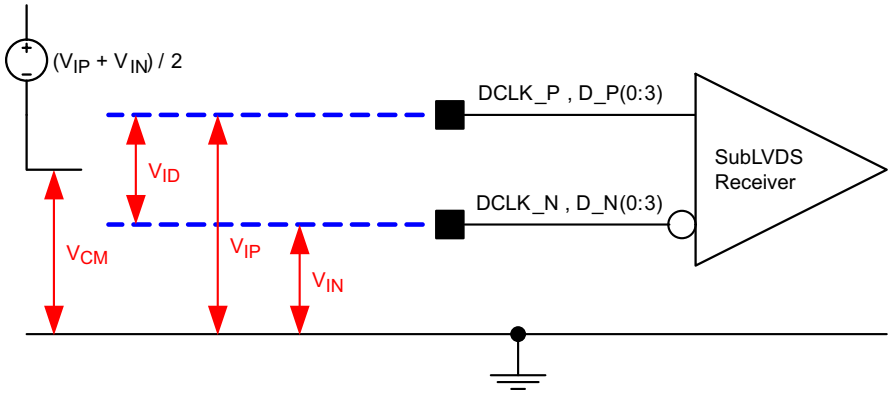


Figure 8. SubLVDS Voltage Parameters

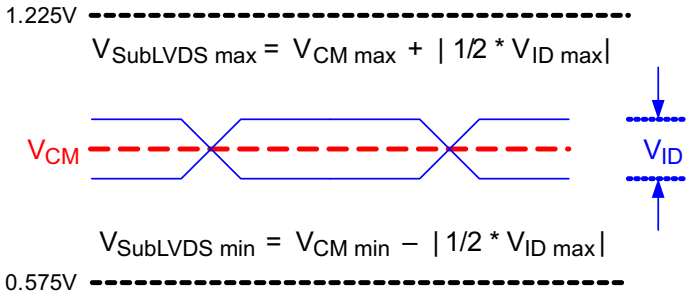


Figure 9. SubLVDS Waveform Parameters

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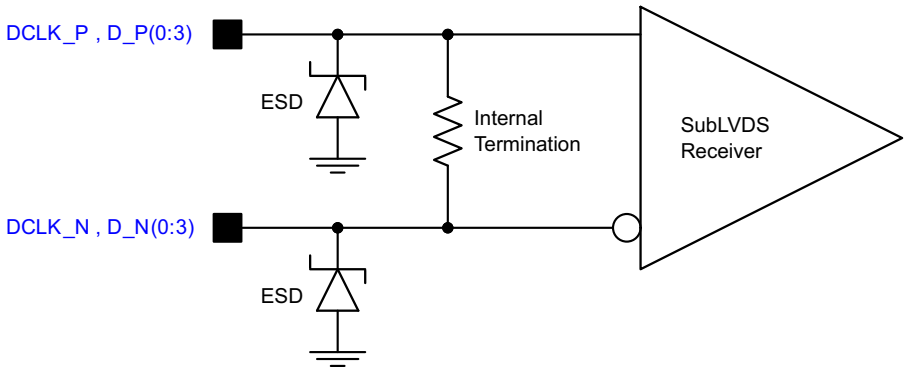


Figure 10. SubLVDS Equivalent Input Circuit

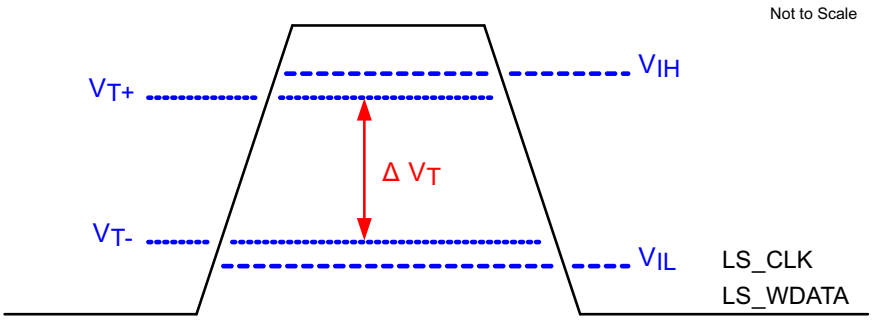


Figure 11. LPSDR Input Hysteresis

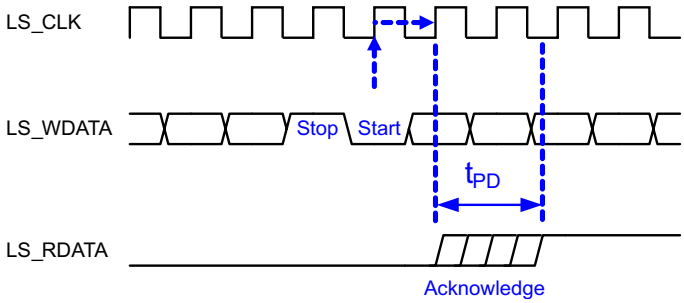
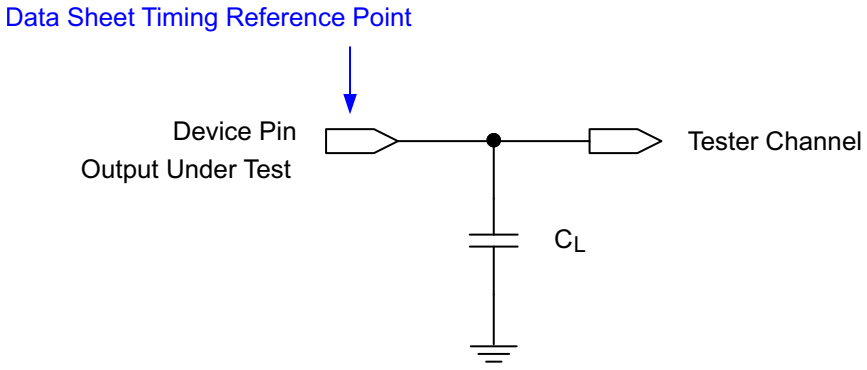


Figure 12. LPSDR Read Out



A. See *Timing* for more information.

Figure 13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. Figure 12	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over **Recommended Operating Conditions** unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Connector area (see Figure 14)			45	N
• DMD mounting area uniformly distributed over 4 areas (see Figure 14)			100	N

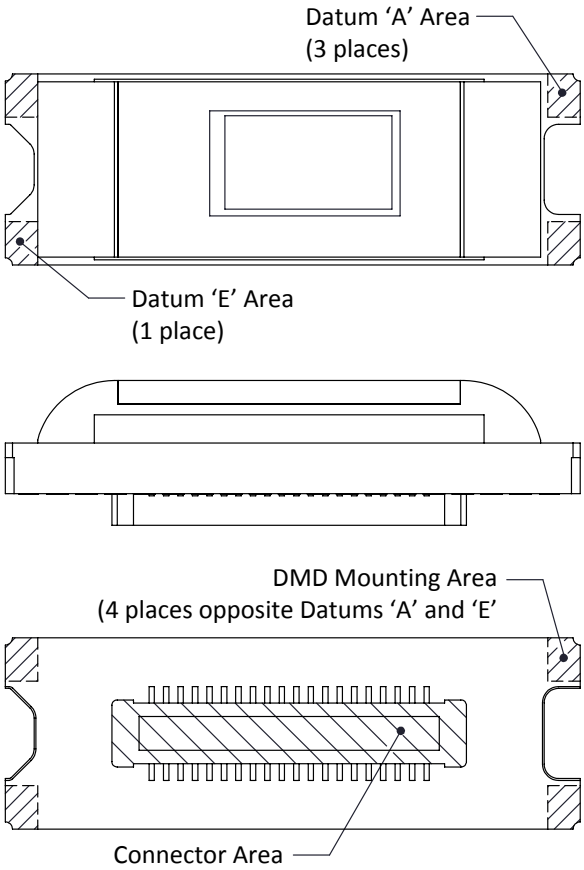


Figure 14. System Interface Loads

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6.10 Physical Characteristics of the Micromirror Array

PARAMETER			VALUE	UNIT
	Number of active columns	See Figure 15	854	micromirrors
	Number of active rows	See Figure 15	480	micromirrors
ε	Micromirror (pixel) pitch	See Figure 16	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 15	4.6116	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 15	2.592	mm
	Micromirror active border	Pond of micromirror (POM) (1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

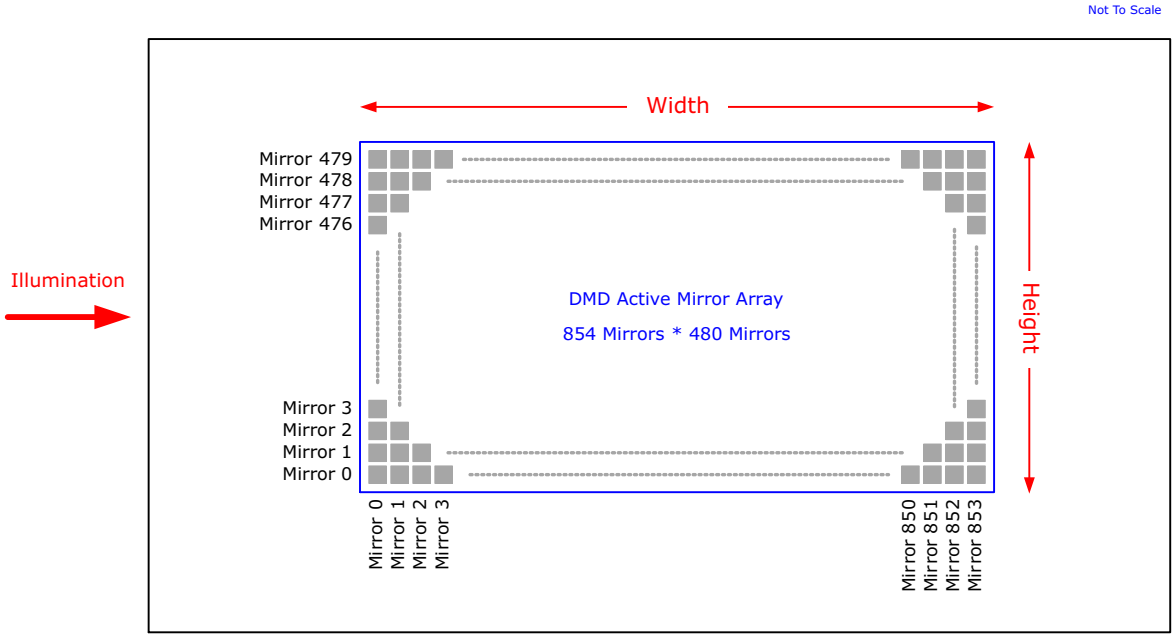


Figure 15. Micromirror Array Physical Characteristics

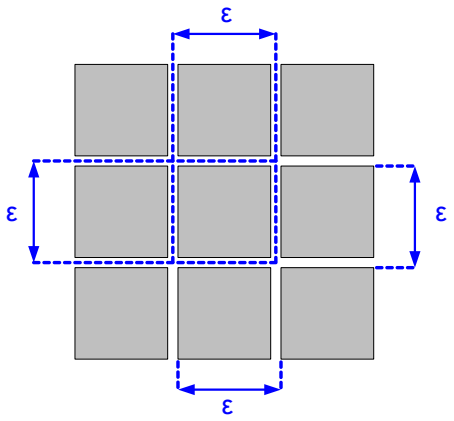


Figure 16. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		17		°
Micromirror tilt angle tolerance(2)(3)(4)(5)		–1		1	°
Micromirror tilt direction(6)(7)	Landed ON state		180		°
	Landed OFF state		270		
Micromirror crossover time	Typical Performance		1.5	4	µs
Micromirror switching time	Typical Performance			6	
Number of out-of-specification micromirrors(8)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.

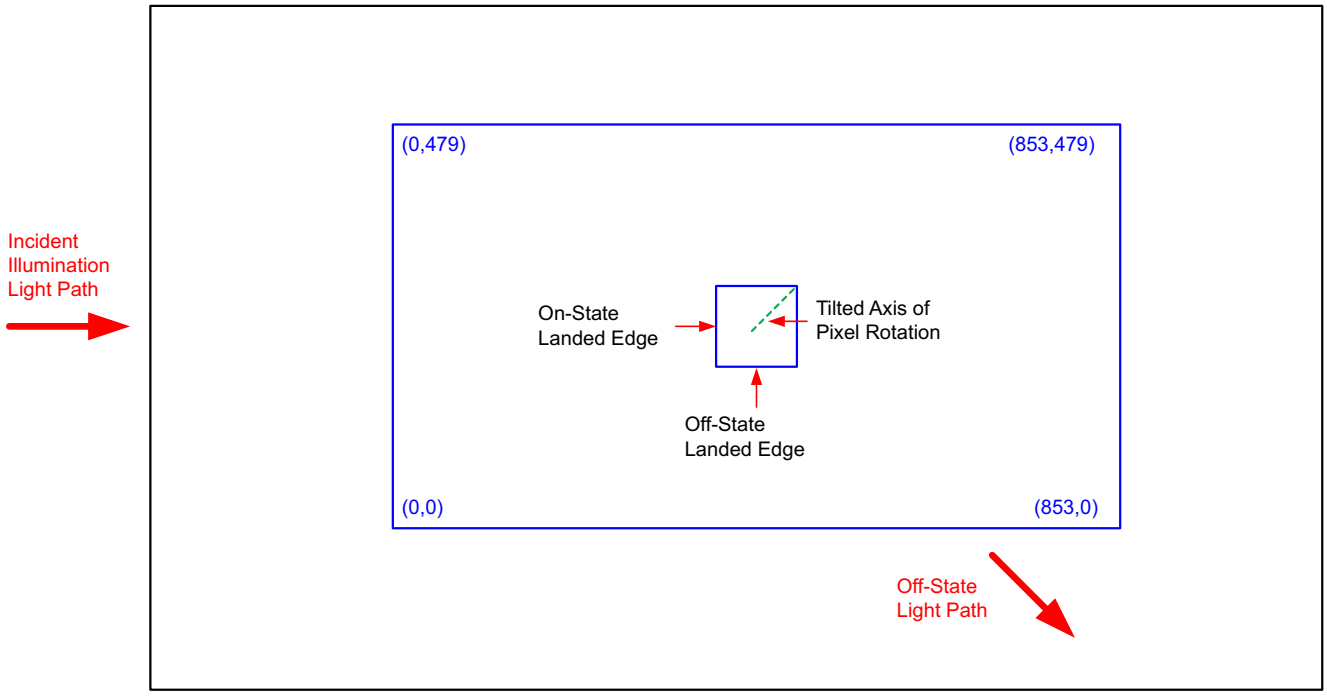


Figure 17. Landed Pixel Orientation and Tilt

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6.12 Window Characteristics

PARAMETER[1]		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture[2]				See [2]	
Illumination overfill[3]				See [3]	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP2010 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

The DLP2010 is a component of one or more DLP chipsets. Reliable function and operation of the DLP2010 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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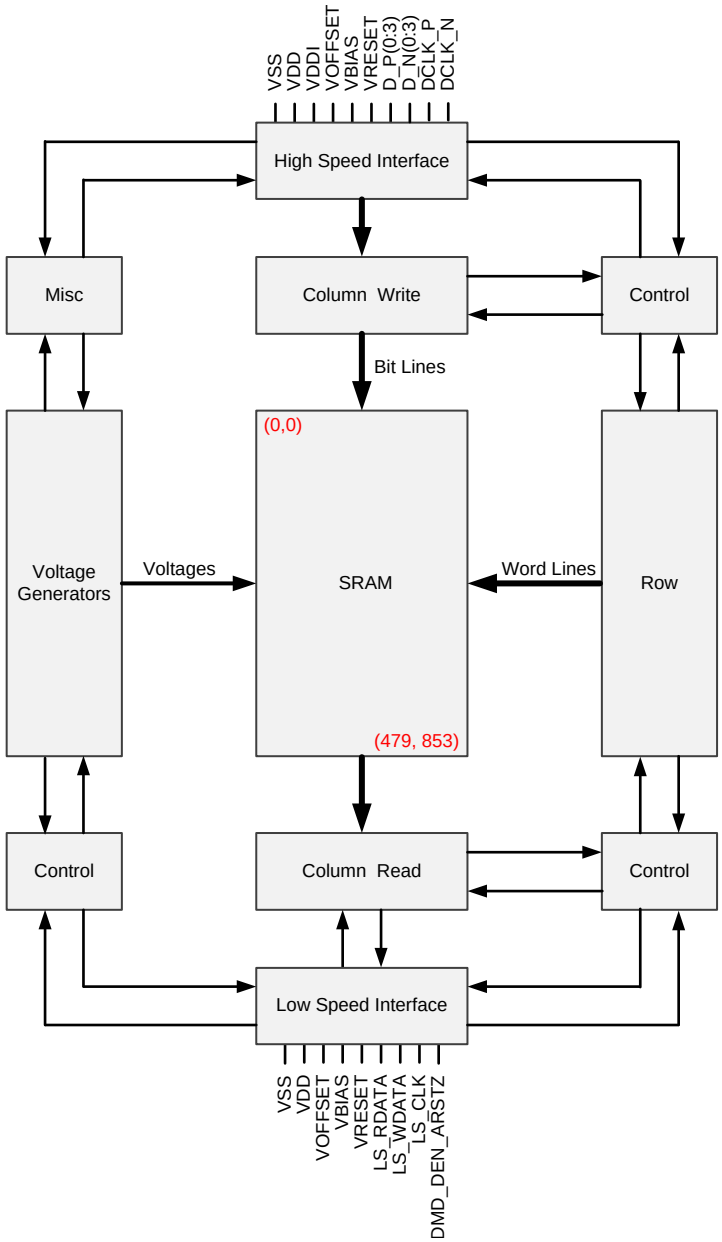
7 Detailed Description

7.1 Overview

The DLP2010 is a 0.2 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 854 columns by 480 rows in a square grid pixel arrangement. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

DLP2010 is part of the chipset comprising of the DLP2010 DMD, DLPC3430 or DLPC3435 display controller and DLPA2000 PMIC/LED driver. To ensure reliable operation, DLP2010 DMD must always be used with DLPC3430 or DLPC3435 display controller and DLPA2000 PMIC/LED driver.

7.2 Functional Block Diagram



Details omitted for clarity.

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7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA2000, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC3430 or DLPC3435 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3430 or DLPC3435 controller. See the DLPC3430 or DLPC3435 controller data sheet or contact a TI applications engineer.

7.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections:

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

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Window Characteristics and Optics (continued)

7.5.1.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

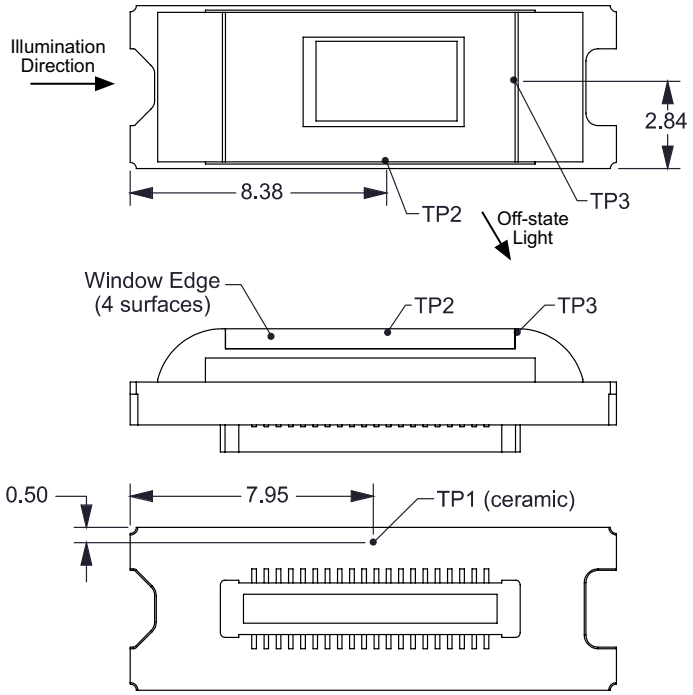


Figure 18. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL)$$

where

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 18
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in *Thermal Information*

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Micromirror Array Temperature Calculation (continued)

- Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics*, plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W), specified in *Electrical Characteristics*
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. Refer to the specifications in *Electrical Characteristics*. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

Sample Calculation for typical projection application:

$T_{CERAMIC}$ = 55°C, assumed system measurement; see *Recommended Operating Conditions* for specification limits

SL = 150 lm

$Q_{ELECTRICAL}$ = 0.0908 W; See the table notes in *Recommended Operating Conditions* for details.

CL2W = 0.00266 W/lm

Q_{ARRAY} = 0.0908 + (0.00266 × 150) = 0.489 W

T_{ARRAY} = 55°C + (0.489 W × 7.9°C/W) = 58.9°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time), whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

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Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 2.

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Table 2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the Landed Duty Cycle is any applied image processing. Within the DLP Controller DLPC3430/DLPC3435, the two functions which affect Landed Duty Cycle are Gamma and IntelliBright™.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC3430/DLPC3435 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 19.

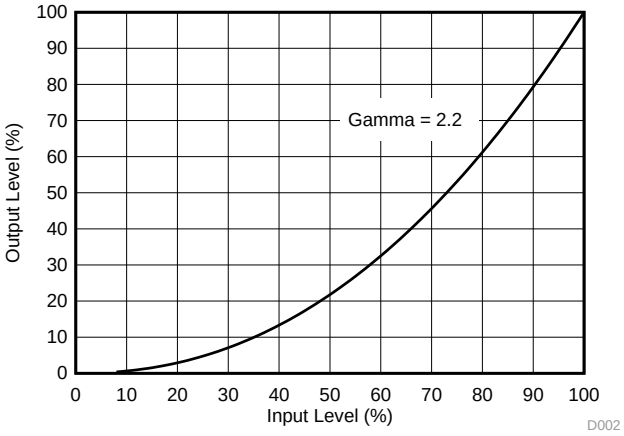


Figure 19. Example of Gamma = 2.2

From Figure 19, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

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But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3430 or DLPC3435 controller.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3430/DLPC3435 controller. The new high tilt pixel in the side illuminated DMD increases brightness performance and enables a smaller system electronics footprint for thickness constrained applications. Applications of interest include projection embedded in display devices like smartphones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery powered mobile accessory, interactive display, low-latency gaming display, and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA2000. Refer to *Power Supply Recommendations* for power-up and power-down specifications. DLP2010 DMD reliability is only specified when used with DLPC3430/DLPC3435 controller and DLPA2000 PMIC/LED Driver.

8.2 Typical Application

A common application when using the DLP2010 chipset is for creating a pico-projector embedded in a handheld product. For example, a pico-projector may be embedded in a smart phone, a tablet, a camera, or camcorder. The DLPC3430 controller in the pico-projector embedded module typically receives images/video from a host processor within the product. DLPC3430 controller then drives the DLP2010 DMD synchronized with the R, G, B LEDs in the optical engine to display the image/video as output of the optical engine.

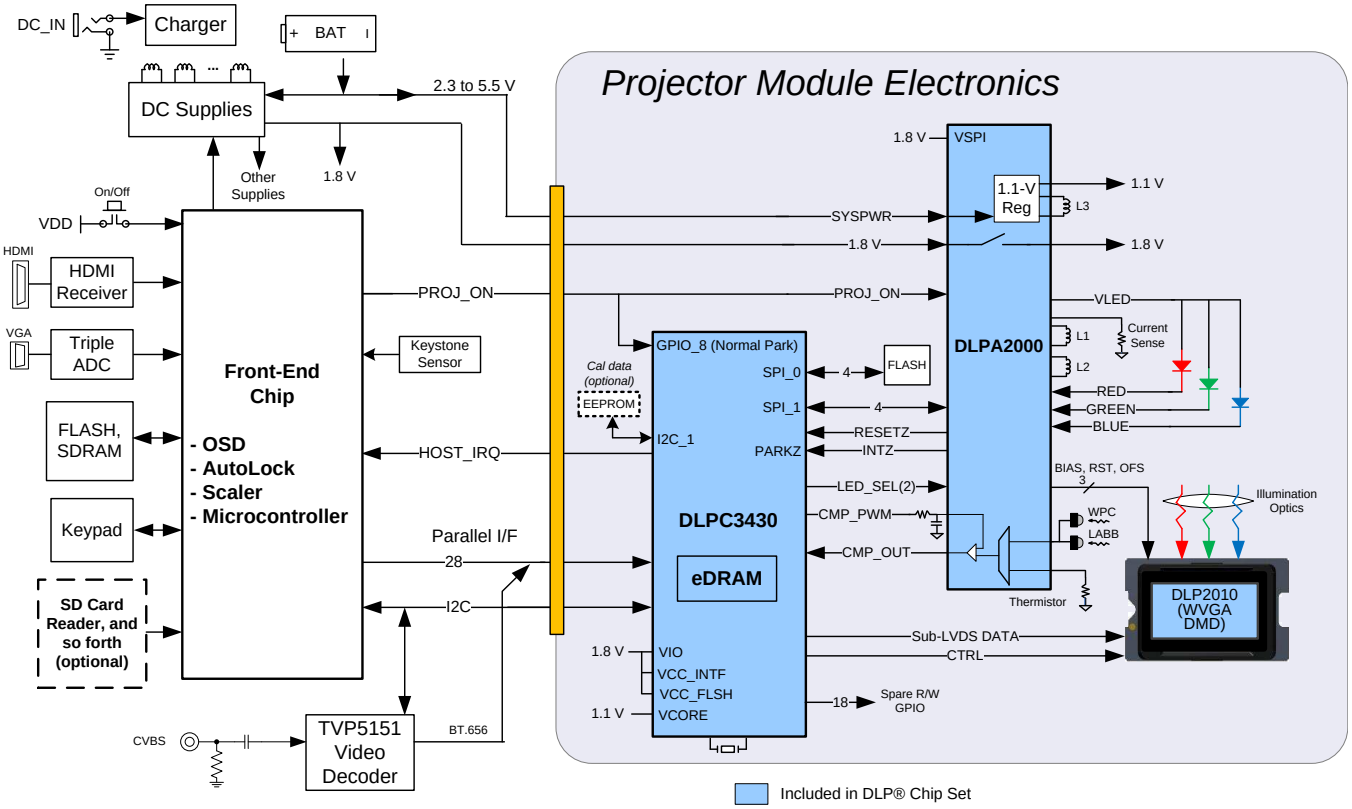


Figure 20. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of a DLP2010 DMD, DLPC3430 or DLPC3435 controller and DLPA2000 PMIC/LED driver. The DLPC3430 or DLPC3435 controller does the digital image processing, the DLPA2000 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips may be needed. At a minimum, a flash part is needed to store the software and firmware to control the DLPC3430 or DLPC3435.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

Parallel interface is used for connecting the DLPC3430 or DLPC3435 to the host processing for receiving images. When the parallel interface is used, I^2C should be connected to the host processor for sending commands to the DLPC3430 or DLPC3435.

The only power supplies needed external to the projector are the battery (SYSPWR) and a regulated 1.8-V supply.

8.2.2 Detailed Design Procedure

For connecting together the DLPC3430 or DLPC3435, the DLPA2000, and the DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

A miniature stepper motor can optionally be added to the optical engine for creating a motorized focus. Direct control and driving of the motor can be done by the DLPA2000, and software commands sent over I^2C to the DLPC3430 or DLPC3435 are available to move the motor to the desired position.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 21. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue.

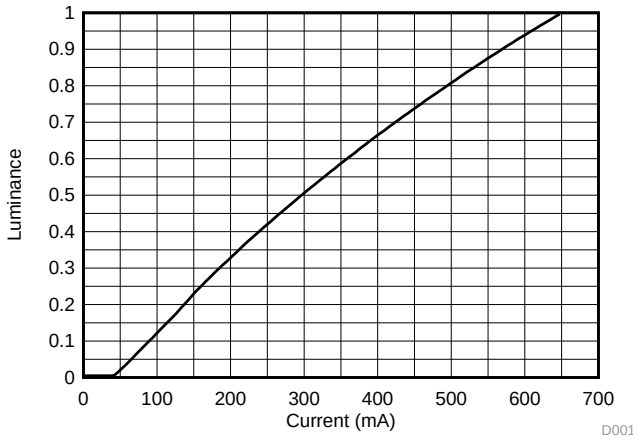


Figure 21. Luminance vs Current

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9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET. DMD power-up and power-down sequencing is strictly controlled by the DLPA2000 or DLPA2005 device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 23. VSS must also be connected.

9.1 Power Supply Power-Up Procedure

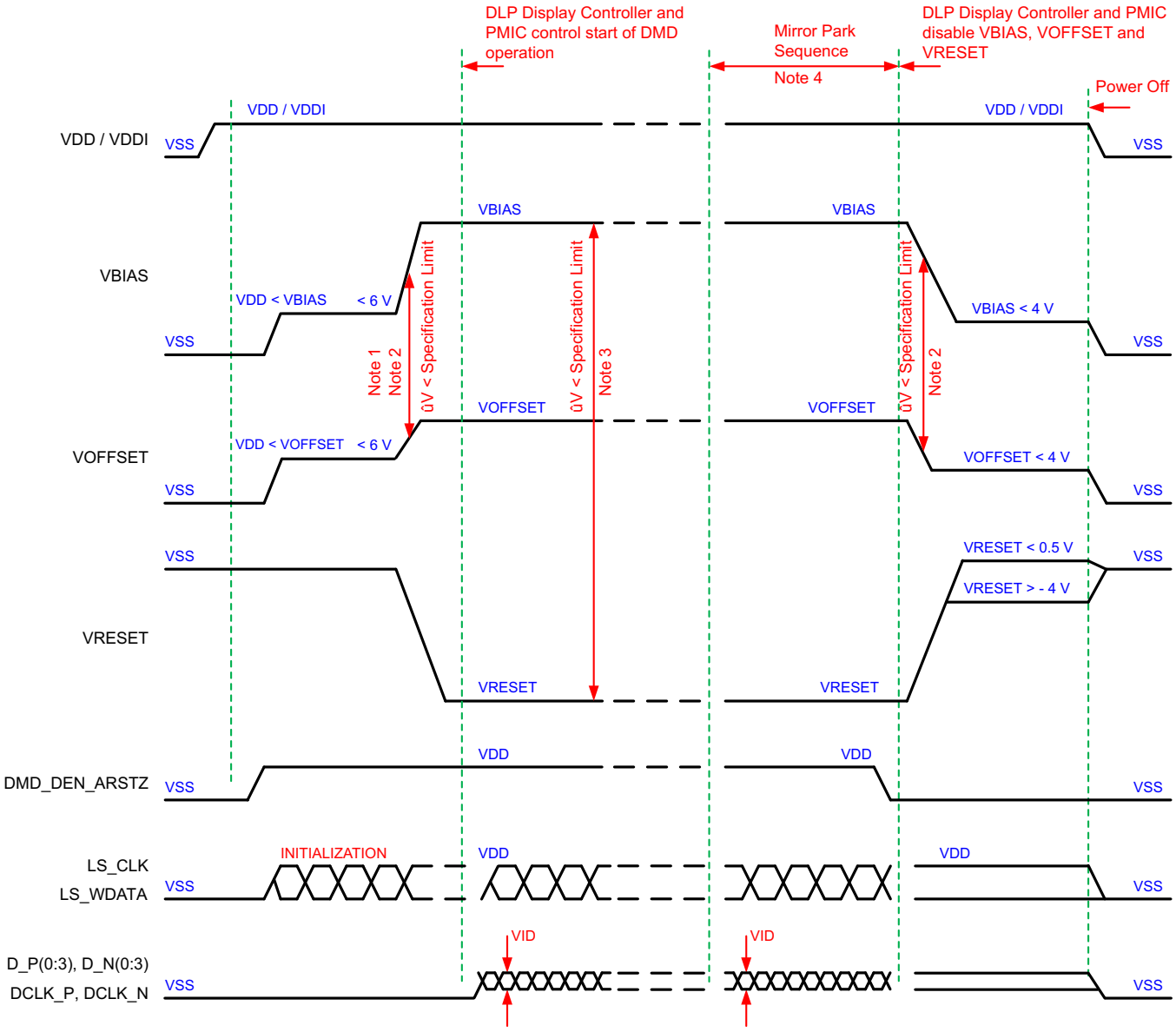
- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. Refer to Table 3 and the *Layout Example* for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions* (Refer to Note 2 for Figure 22).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

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9.3 Power Supply Sequencing Requirements



(1) Refer to Table 3 and Figure 23 for critical power-up sequence delay requirements.

(2) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Refer to Table 3 and Figure 23 for power-up delay requirements

(3) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit shown in *Recommended Operating Conditions*.

(4) When system power is interrupted, the ASIC driver initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the Micromirror Park Sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the Micromirror Park Sequence through software control.

(5) Drawing is not to scale and details are omitted for clarity.

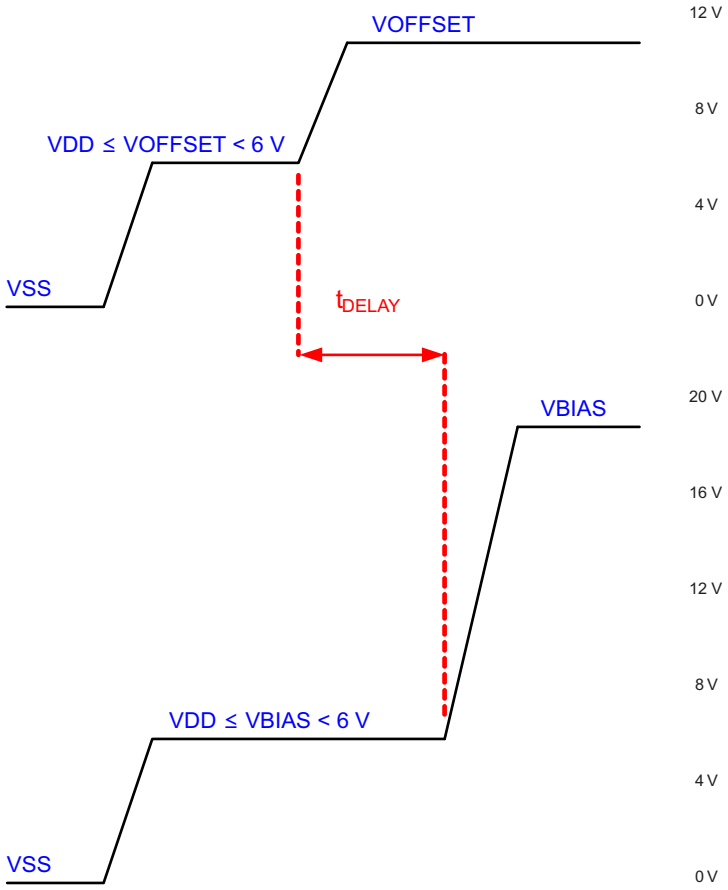
Figure 22. Power Supply Sequencing Requirements (Power Up and Power Down)

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Power Supply Sequencing Requirements (continued)

Table 3. Power-Up Sequence Delay Requirement

PARAMETER		MIN	UNIT
t_{DELAY}	Delay requirement from VOFFSET power up to VBIAS power up	2	ms
V_{OFFSET}	Supply voltage level during power–up sequence delay (see Figure 23)	6	V
V_{BIAS}	Supply voltage level during power–up sequence delay (see Figure 23)	6	V



A. Refer to Table 3 for VOFFSET and VBIAS supply voltage levels during power-up sequence delay.

Figure 23. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and Ctrl signals between the DLPC343x controller and the DLP2010 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Figure 24.
- Minimum of 100-nF decoupling capacitor close to VBIAS. Capacitor C4 in Figure 25.
- Minimum of 100-nF decoupling capacitor close to VRST. Capacitor C6 in Figure 25.
- Minimum of 220-nF decoupling capacitor close to VOFS. Capacitor C7 in Figure 25.
- Optional minimum 200- to 220-nF decoupling capacitor to meet the ripple requirements of the DMD. C5 in Figure 25.
- Minimum of 100-nF decoupling capacitor close to Vcci. Capacitor C1 in Figure 25.
- Minimum of 100-nF decoupling capacitor close to both groups of Vcc pins, for a total of 200 nF for Vcc. Capacitor C2/C3 in Figure 25.

10.2 Layout Example

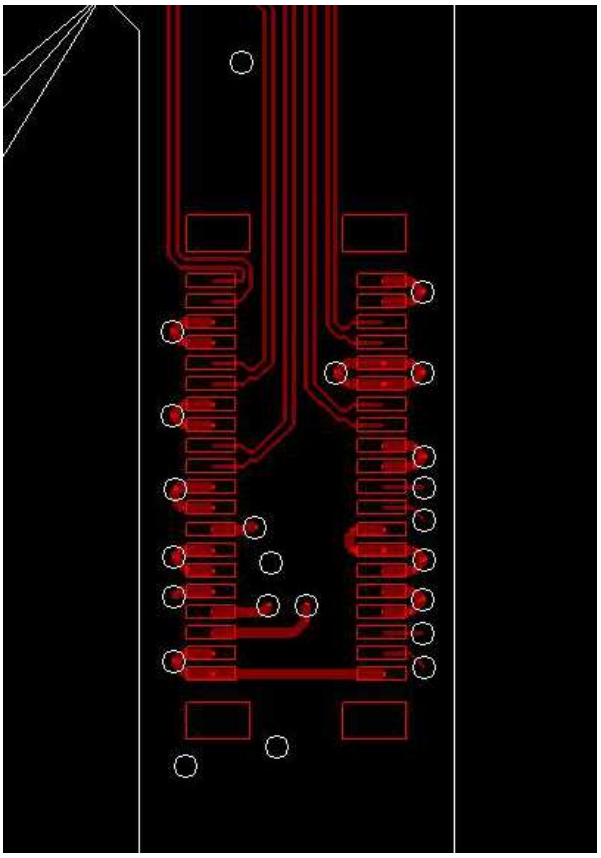


Figure 24. High-Speed (HS) Bus Connections

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Layout Example (continued)

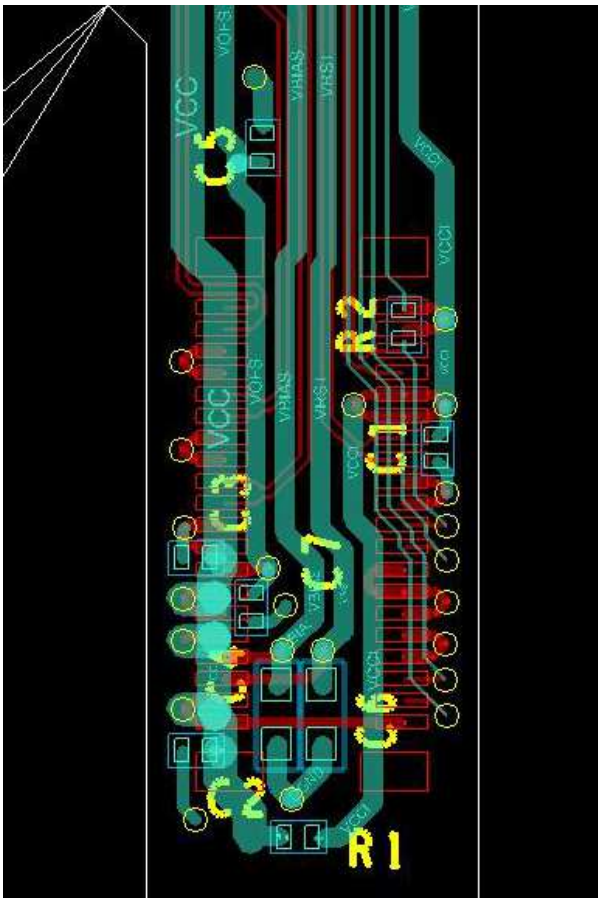


Figure 25. Power Supply Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

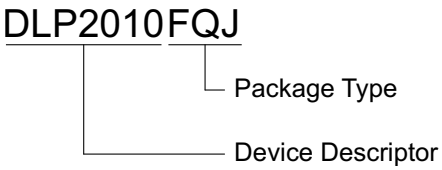


Figure 26. Part Number Description

11.1.2 Device Markings

Device Marking will include the human–readable character string GHJJJJK VVVV on the electrical connector. GHJJJJK is the lot trace code. VVVV is a 4 character encoded device part number

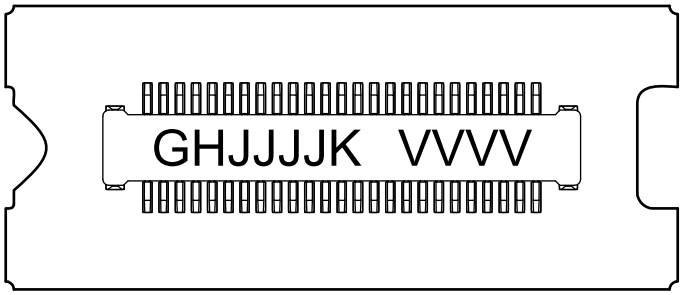


Figure 27. DMD Marking

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPC3430	Click here	Click here	Click here	Click here	Click here
DLPC3435	Click here	Click here	Click here	Click here	Click here
DLPA2000	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

IntelliBright is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP2010FQJ	ACTIVE	CLGA	FQJ	40	120	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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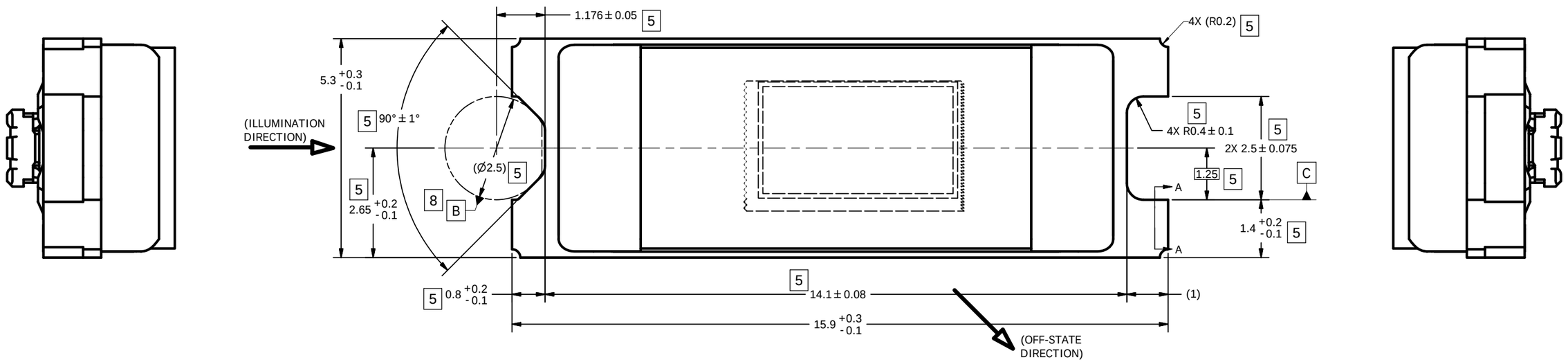
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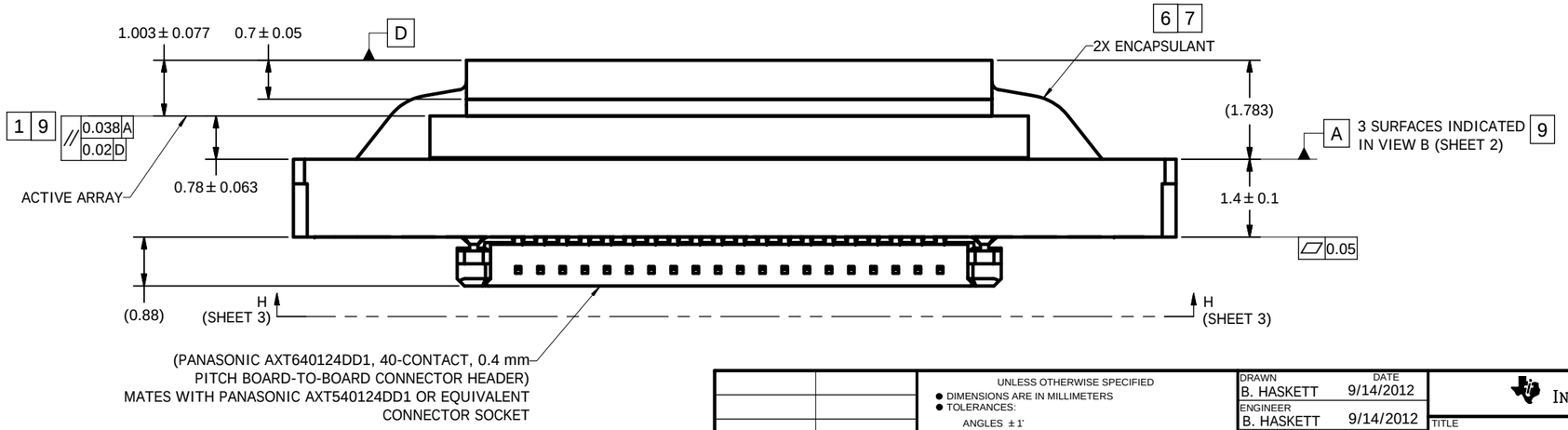
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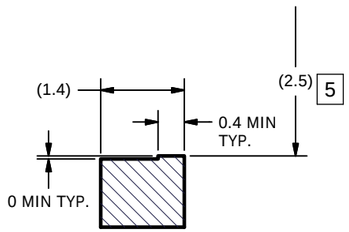
REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2127544: INITIAL RELEASE	9/14/2012	BMH
B	ECO 2129552: ENLARGE APERTURE ON RIGHT SIDE; MOVE ACTIVE ARRAY Y-LOCATION DIM, SH. 3	12/10/2012	BMH
C	ECO 2131252: ENLARGE APERTURE ALONG BOTTOM EDGE	2/20/2013	BMH
D	ECO 2135244: CORRECT WINDOW THK TOL, ZONE B6	8/5/2013	BMH
E	ECO 2138016: INCREASE WINDOW THK NOMINAL	11/21/2013	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR IN CONNECTOR RECESS.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
7. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
8. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
9. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.







SECTION A-A
NOTCH OFFSETS

0314DA	
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1'
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL UNITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	9/14/2012
ENGINEER	B. HASKETT	9/14/2012
QA/CE	P. KONRAD	9/26/2012
CM	F. ARMSTRONG	9/26/2012
	M. DORAK	9/18/2012
APPROVED	M. SOUCEK	9/18/2012

TEXAS INSTRUMENTS
Dallas Texas

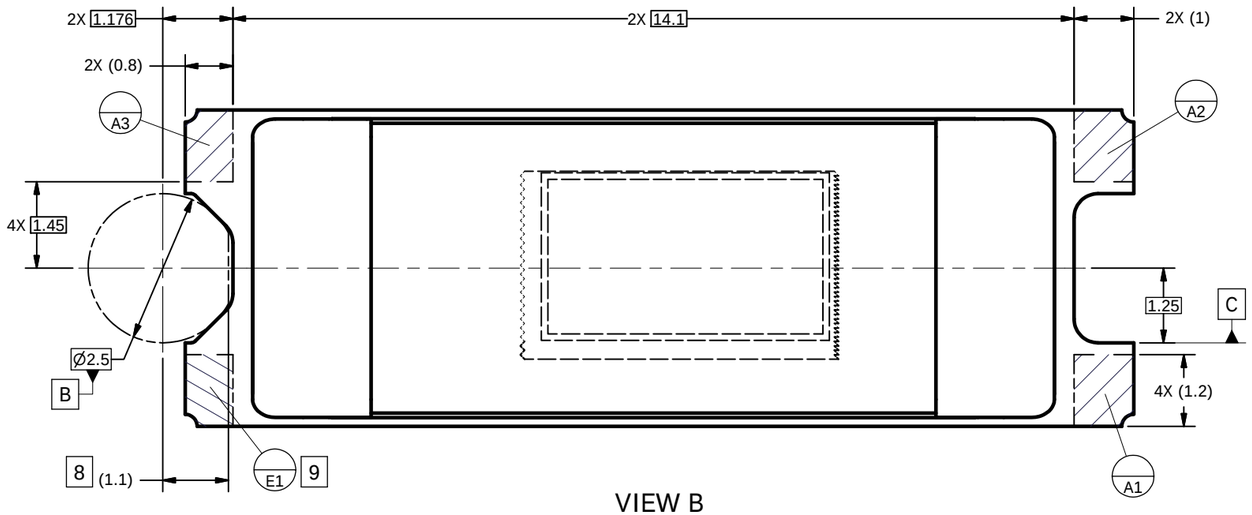
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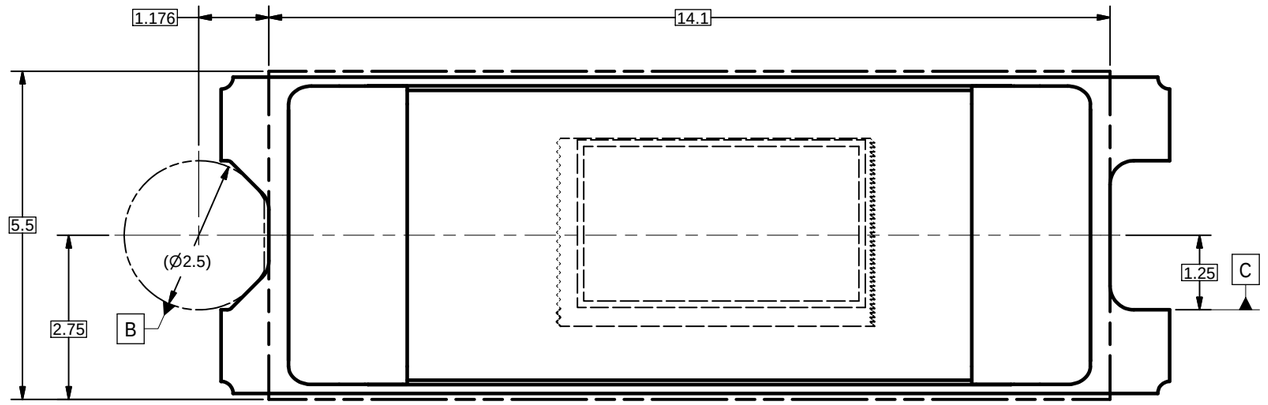
SCALE 20:1 SHEET 1 OF 3

DWG NO. 2512515 SH 1

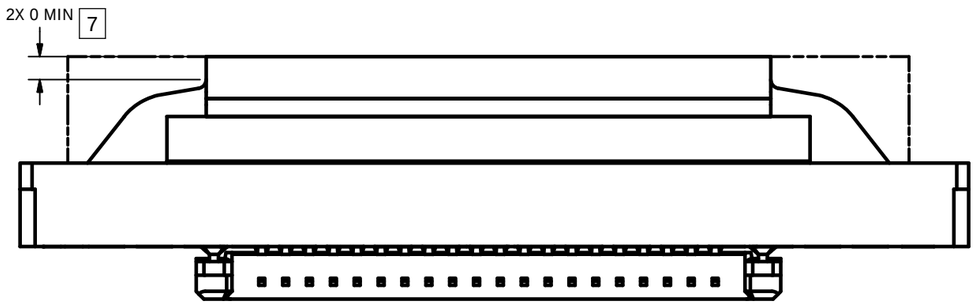
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



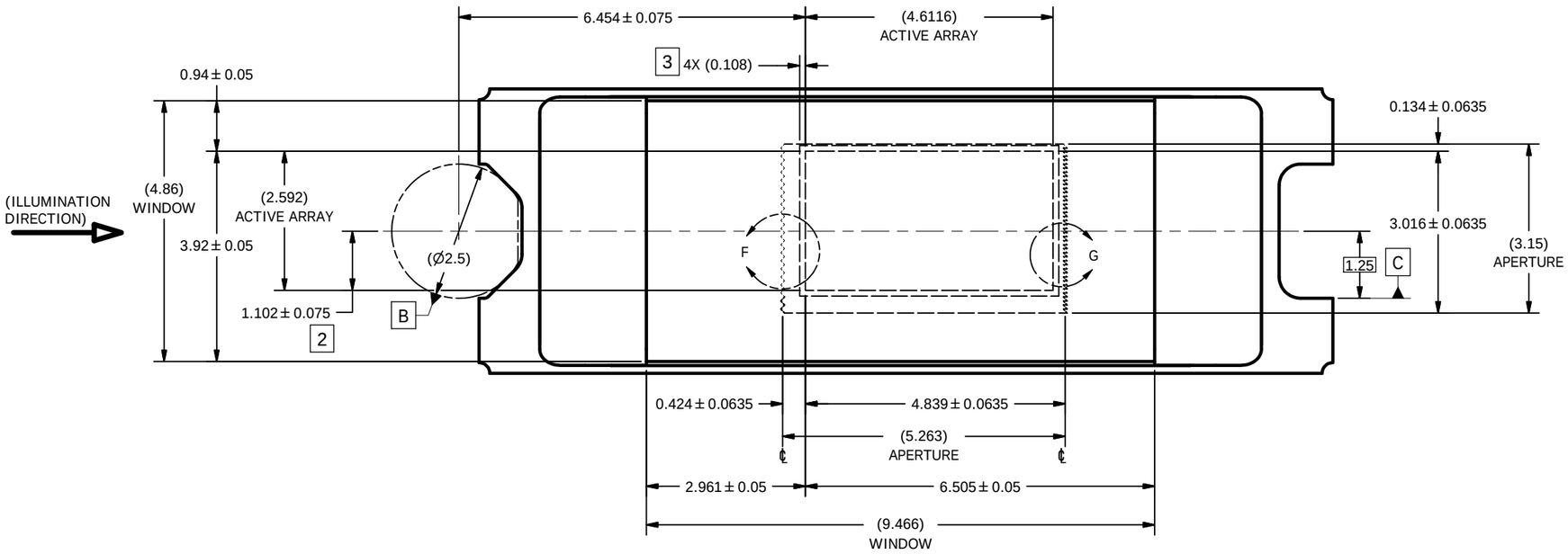
VIEW C 6
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



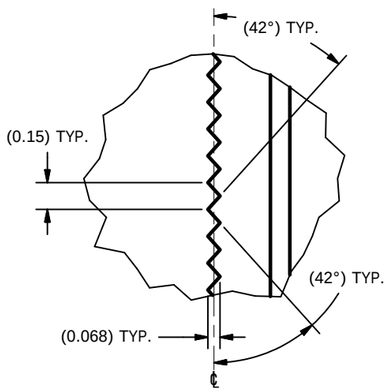
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 9/14/2012	SIZE D	DWG NO 2512515	REV E
			SCALE	SHEET 2 OF 3	

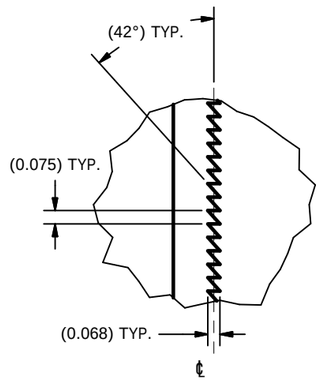
INV11-2006a



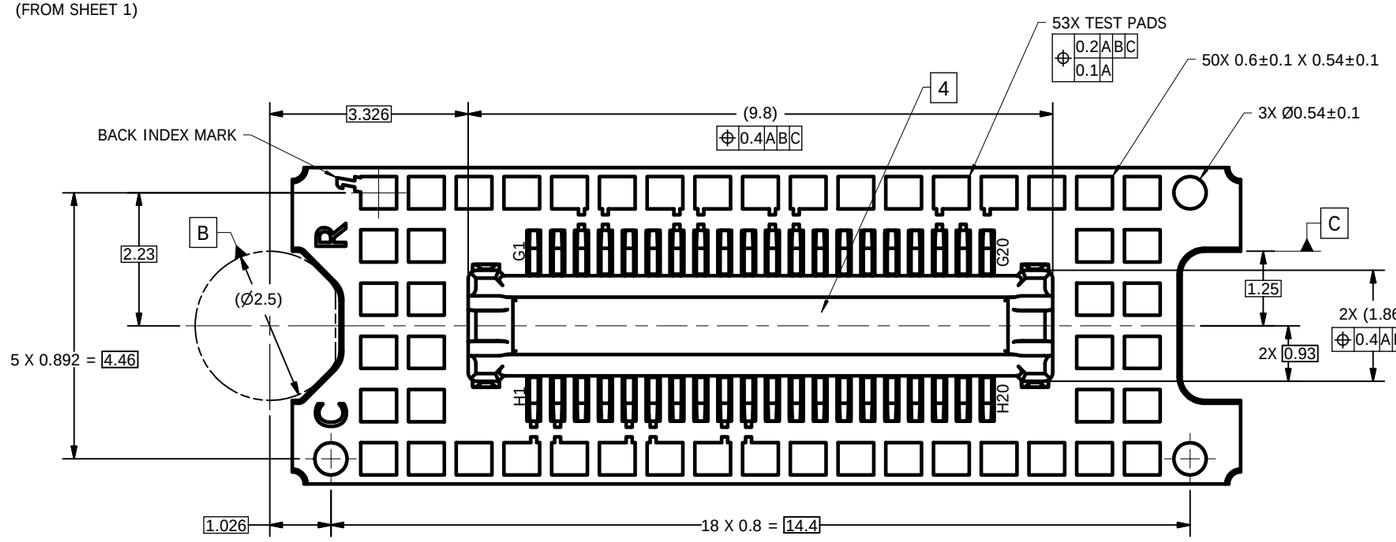
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
(POND OF MIRRORS OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW H-H
TEST PADS AND CONNECTOR
(FROM SHEET 1)

Texas Instruments Dallas Texas	DRAWN B. HASKETT	DATE 9/14/2012	SIZE D		DWG NO 2512515	REV E
			SCALE		SHEET 3 OF 3	

INV11-2006a

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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