DESCRIPTION

The A34C04 is a 512-byte EEPROM device designed to operate the SMBus bus in the 1.7V - 3.6V voltage range, with a maximum of 1 MHz.

The A34C04 includes a 4-Kbit serial EEPROM organized as two banks of 256 bytes each, or 512 bytes of total memory. Each bank is composed of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write-protected in one or more memory blocks.

Individually locking a 128-byte block may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input A0. By sending the device a specific SMBus sequence, each block may be protected from writes until the write protection is electrically reversed using a separate SMBus sequence which also requires V_{HV} on input A0. The write protection for all four blocks is cleared simultaneously

The A34C04 is available in DFN8 package.

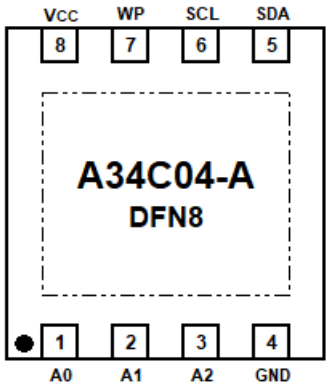
ORDERING INFORMATION

Package Type	Part Number	
DFN8 SPQ: 3,000pcs/Reel	J8	A34C04J8R-Z
		A34C04J8VR-Z
Note	Z: Pin Type A: Type A B: Type B V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

FEATURES

- 512-byte Serial Presence Detect EEPROM compatible with JEDEC EE1004 specification
- Compatible with SMBus serial interface:
  -up to 1 MHz transfer rate
- Memory array:
  -4-Kbit organized as two banks of 256 bytes each
  -Each page is composed of two 128-byte blocks
- Software data protection for each 128-byte block
- Hardware write protection
- Write:
  -Byte Write within 3 ms
  -16 bytes Page Write within 3 ms
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Single supply voltage:
  -1.7 V to 3.6 V
- High-reliability
  -Endurance: 1 Million Write Cycles
  -Data Retention: 100 Years
- Enhanced ESD/latch-up protection
  -HBM 6000V
- Available in DFN8 package

PIN DESCRIPTION



Type A - Top View



Type B - Top View

Pin # DFN8 Type A	Pin # DFN8 Type B	Symbol	I/O	Function
1	1	A0	I	Address Inputs
2	2	A1	I	Address Inputs
3	3	A2	I	Address Inputs
4	4	GND	P	Ground
5	5	SDA	I/O	Serial Data
6	6	SCL	I	Serial Clock Input
7	-	WP	I	Write Protect
-	7	NC	-	No Connection
8	8	V_{CC}	P	Power Supply

ABSOLUTE MAXIMUM STRESS RATINGS

DC Supply Voltage	-0.5V ~ 6.5V
Input / Output Voltage	GND-0.3V ~ V_{CC}+0.3V
Voltage on Pin A0	-0.5V ~ 10V
Operating Ambient Temperature	-40°C ~ +130°C
Storage Temperature	-65°C ~ +150°C
Electrostatic pulse (Human Body model)	6000V

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

Applicable over recommended operating range form: T_A = 25℃, f = 1.0MHz, V_{CC} = +1.7V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input/Output Capacitance (SDA)	$C_{I/O}$	V_{IO}=0V	-	-	8	pF
Input Capacitance (A0, A1, A2, SCL)	C_{IN}	V_{IN}=0V	-	-	6	pF

DC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range form: T_A = 0℃ to +95℃, V_{CC} = +1.7V to +5.5V, unless otherwise noted

Parameter	Symbol	Test condition (in addition to those in AC Electrical Characteristics)	Min	Max	Unit
Input Leakage Current (SCL, SDA, A0, A1, A2)	I_{LI}	V_{IN} = GND or V_{CC}	-	± 2	μA
Output Leakage Current	I_{LO}	SDA in Hi-Z, external voltage applied on SDA: GND or V_{CC}	-	± 2	μA
Supply Current (read)	I_{CC}	f_c = 400kHz or 1MHz	-	1	mA
Supply Current (write)	I_{CC0}	During t_W, V_{IN} = GND or V_{CC}	-	1NOTE1	mA
Standby Supply Current	I_{CC1}	Device not selectedNOTE2, V_{IN} = GND or V_{CC}, V_{CC} ≥ 2.2V	-	2	μA
		Device not selectedNOTE2, V_{IN} = GND or V_{CC}, V_{CC} < 2.2V	-	1	μA
Input Low Voltage (SCL, SDA, WP)	V_{IL}		-0.45	0.3xV_{CC}	V
Input High Voltage (SCL, SDA, WP)	V_{IH}		0.7xV_{CC}	V_{CC}+1V	V
A0 High Voltage Detect	V_{HV}	V_{CC} < 2.2V	7	10	V
		V_{CC} ≥ 2.2V	V_{CC}+4.8V	10	V
Output Low Voltage	V_{OL}	I_{OL} = 0.15mA	-	0.2	V
		I_{OL} = 3mA	-	0.4	V
Power On Reset Threshold	V_{POR}		-	1.4NOTE1	V
Power Down Reset Threshold	V_{PDR}		0.7NOTE2	-	V

NOTE1: Measured during characterization, not tested in production.

NOTE2: The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write command).

AC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range form: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, C_L = 1 TTL Gate and 100 pF, unless otherwise noted

Parameter	Symbol		V_{CC} < 2.2V		V_{CC} ≥ 2.2V				Unit
			100kHz		400kHz		1000kHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency	f_{SCL}	f_C	10	100	10	400	10	1000	kHz
Clock Pulse Width High Time	t_{HIGH}	t_{CHCL}	4000	-	600	-	260	-	ns
Clock Pulse Width Low Time	t_{LOW}[NOTE1]	t_{CLCH}	4700	-	1300	-	500	-	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$[NOTE2]		25	35	25	35	25	35	ms
SDA Rise Time	t_R[NOTE3]	t_{XH1XH2}	-	1000	20	300	-	120	ns
SDA(out) Fall Time	t_F[NOTE3]	t_{QL1QL2}	-	300	20	300	-	120	ns
Data In Setup Time	$t_{SU:DAT}$	t_{DXCH}	250	-	100	-	50	-	ns
Data In Hold Time	$t_{HD:DI}$	t_{CLDX}	0	-	0	-	0	-	ns
Data Out Hold Time	$t_{HD:DAT}$	t_{CLQX}	200	3450	200	900	0	350	ns
Start Condition Setup Time	$t_{SU:STA}$[NOTE4]	t_{CHDL}	4700	-	600	-	260	-	ns
Stop Condition Hold Time	$t_{HD:STA}$	t_{DLCL}	4000	-	600	-	260	-	ns
Stop Condition Setup Time	$t_{SU:STO}$	t_{CHDH}	4000	-	600	-	260	-	ns
Time between Stop Condition and next Start Condition	t_{BUF}	t_{DHDL}	4700	-	1300	-	500	-	ns
Write Time	t_W		-	3	-	3	-	3	ms
Time ensuring a Reset when V_{CC} drops below $V_{PDR(min)}$	t_{POFF}[NOTE3]		100	-	100	-	100	-	μs
Time from $V_{CC(min)}$ to the first command	t_{INIT}[NOTE3]		0	-	0	-	0	-	μs

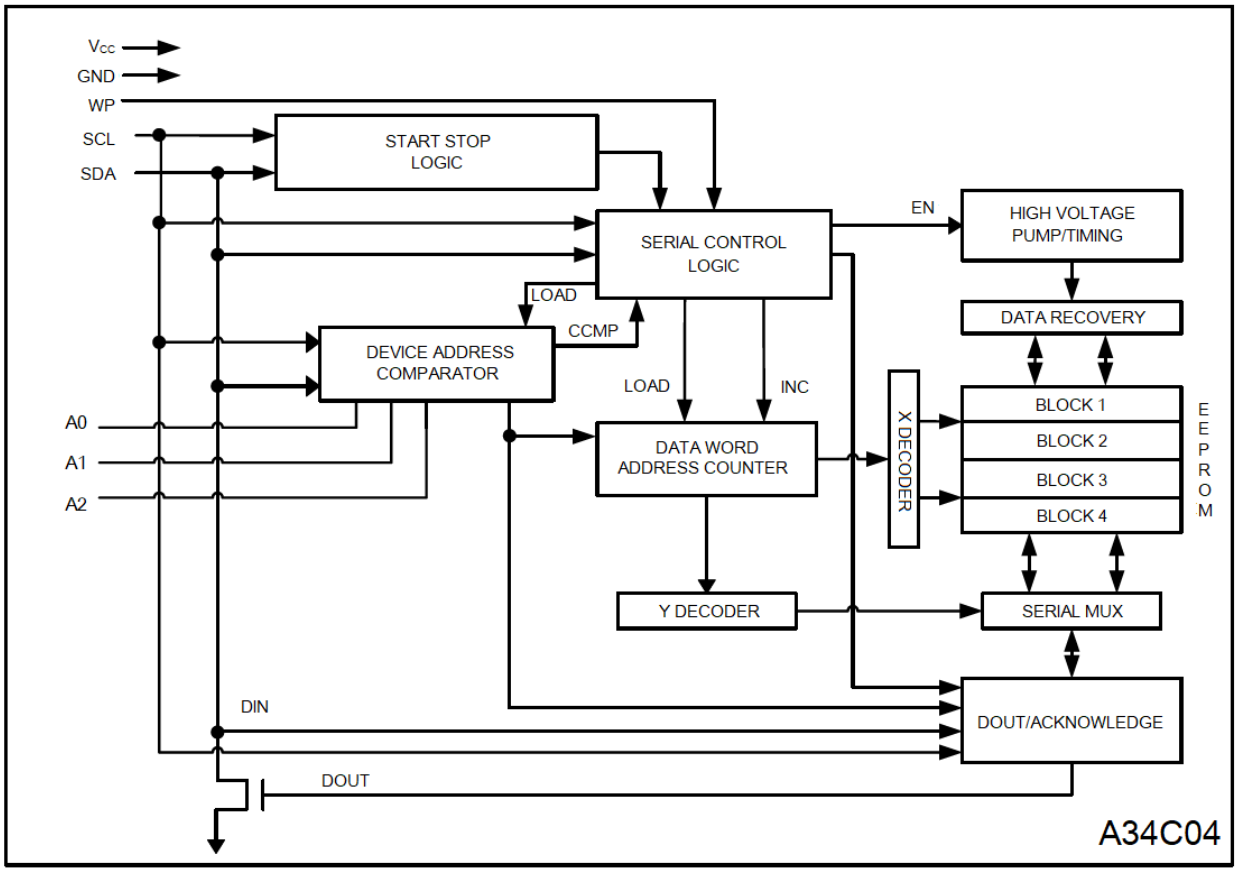
NOTE1: Initiate clock stretching, which is an optional SMBus bus feature.

NOTE2: A timeout condition can only be ensured if SCL is driven low for $t_{TIMEOUT(Max)}$ or longer; then the A34C04 is set in Standby mode and is ready to receive a new START condition. If SCL is driven low for less than $t_{TIMEOUT(Min)}$, the A34C04 internal state remains unchanged.

NOTE3: Measured during characterization, not tested in production.

NOTE4: To avoid spurious START and STOP conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.

BLOCK DIAGRAM



DETAILED INFORMATION

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the A34C04. Eight 4K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).
The A0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.
If SCL is driven low for $t_{TIMEOUT}$ (see AC Electrical Characteristics) or longer, the A34C04 is set back in Standby mode, ready to receive a new START condition.

WRITE PROTECT (WP): The A34C04 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to V_{CC}, the write protection feature is enabled.

FUNCTIONAL DESCRIPTION

1. Memory addressing

To start a communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 1 (on Serial Data (SDA), most significant bit first).

The Device Type Identifier Code (DTIC) consists of a 4-bit device type identifier, and a 3-bit slave address (A2, A1, A0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

Table 1

	Abbr	Device type identifier				Select address			R_W_n	SA0 pin
		b7	b6	b5	b4	b3	b2	b1	b0	
Read	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0,1 or V_{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0,1 or V_{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0,1 or V_{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0,1 or V_{HV}
Set Page Address to 0	SPA0					1	1	0	0	0,1 or V_{HV}
Set Page Address to 1	SPA1					1	1	1	0	0,1 or V_{HV}
Read Page Address	RPA					1	1	0	1	0,1 or V_{HV}
Reserved	-					All other encodings				

Up to eight memory devices can be connected on a single serial bus. Each one is given a unique 3-bit code on the slave address (A2, A1, A0) inputs. When the device select code is received, the device only responds if the slave address is the same as the value on the slave address (A2, A1, A0) inputs.

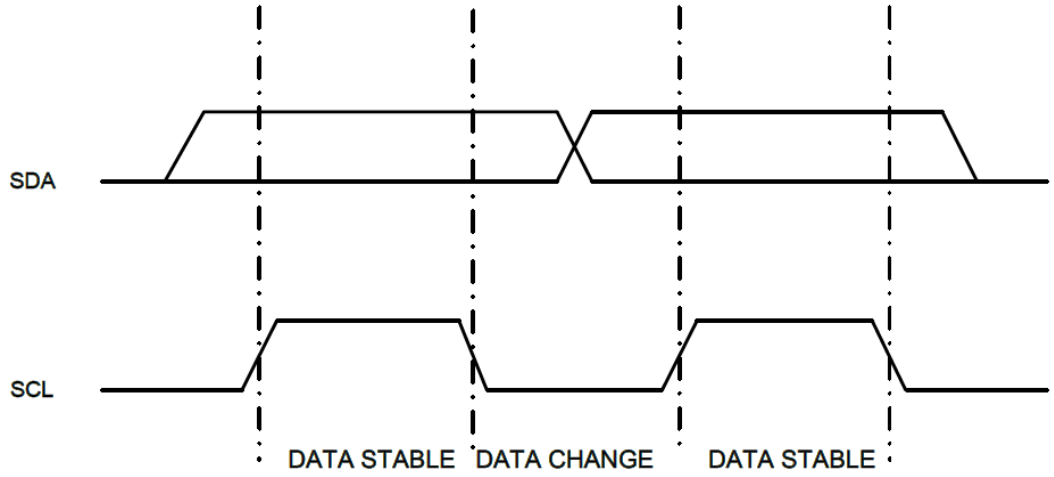
The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

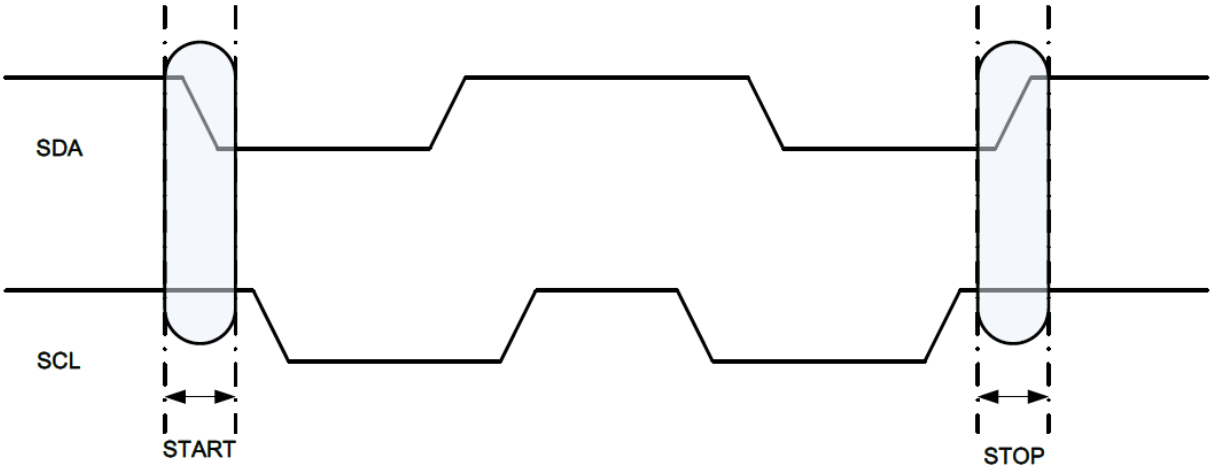
Figure 1. Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

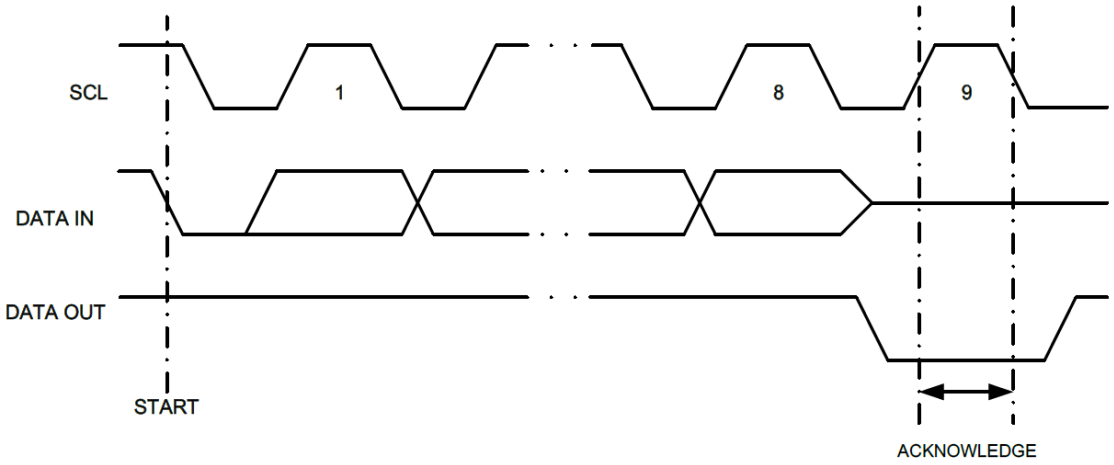
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2).

Figure 2. Start and Stop Definition



ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3. Output Acknowledge



STANDBY MODE: The A34C04 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

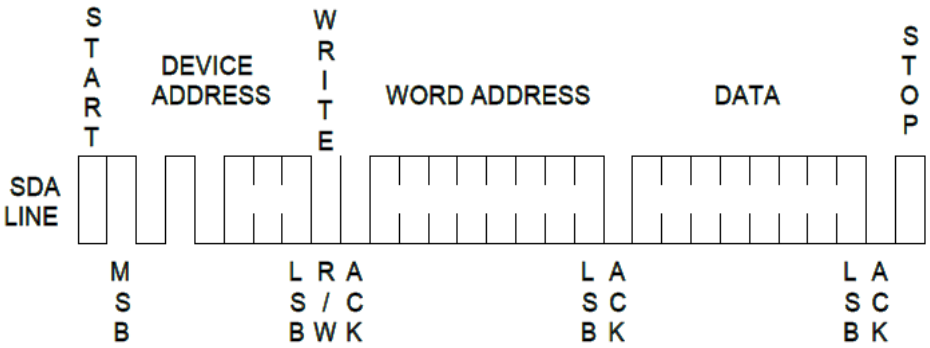
1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

DATA SECURITY: The A34C04 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

3. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (Figure 4).

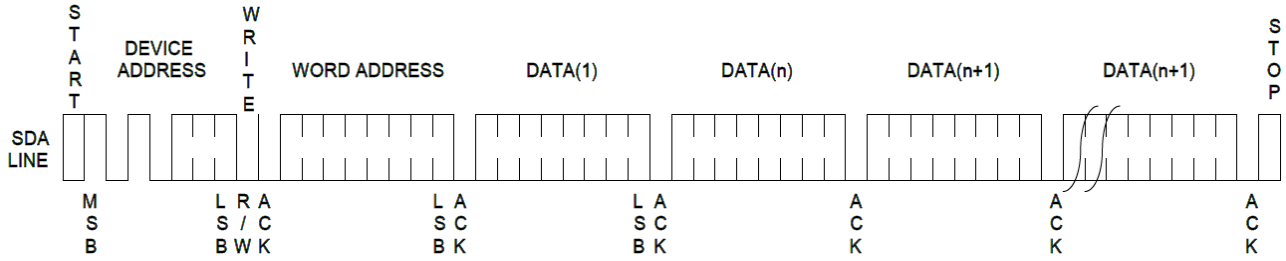
Figure 4. Byte Write



If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified.

PAGE WRITE: The Page write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory. A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

Figure 5. Page Write



The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified.

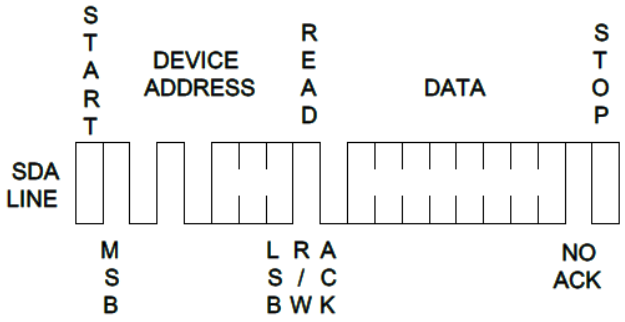
ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

4. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

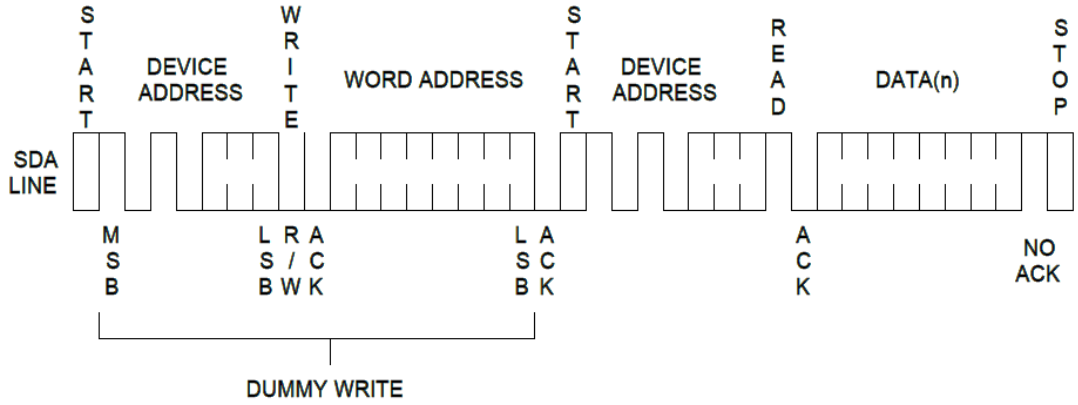
CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 6).

Figure 6. Current Address Read



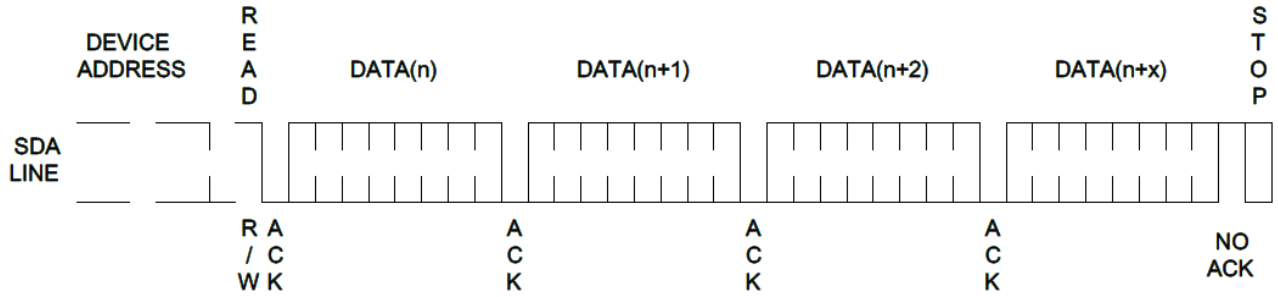
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 7)

Figure 7. Random Read



SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8).

Figure 8. Sequential Read



5. Setting the write protection

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

The device has three software commands for setting, clearing, or interrogating the write-protection status.

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), page address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), page address = 1

The level of write protection (set or cleared), that has been defined using these instructions, remains defined even after a power cycle.

- SWPn: Set Write Protection for block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection status for block n

The DTICs of the SWP, CWP and RPS instructions are defined in Table 1.

6. Set and clear the write protection (SWPn and CWP)

If the software write protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.

When decoded, SWPn and CWPn trigger a write cycle lasting t_W (see AC Electrical Characteristics).

The DTICs of the SWP and CWP instructions are defined in Table 1.

7. Read the protection status (RPSn)

The serial bus master issues an RPSn command specifying which block to report upon. If the software write protection has not been set, the device replies to the data byte with an Ack. If it has been set, the device replies to the data byte with a NoAck.

The DTIC of the RPSn instruction is defined in Table 1.

8. Set the page address (SPAn)

The SPAn command selects the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the page address is always 0, selecting the lower 256 bytes.

The DTIC of the SPAn instruction is defined in Table 1.

9. Read the page address (RPA)

The RPA command determines if the currently selected page is 0 (device returns Ack) or 1 (device returns NoAck). The DTIC of the RPA instruction is defined in Table 1.

Use within a DDR4 DRAM module

In the application, the A34C04 is soldered directly in the printed circuit module. The three slave address inputs (A2, A1, A0) must be connected to GND or V_{CC} directly (that is without using a serial resistor) through the DRAM module connector (see Table 2). The pull-up resistor on SDA is connected on the SMBus of the motherboard.

The Write Protect (WP) of the A34C04 can be left unconnected. However, connecting it to GND is recommended, to maintain full read and write access.

Table 2

DIMM position	A2	A1	A0
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

1. Programming the A34C04

The situations in which the A34C04 is programmed can be considered under two headings:

- when the DDR4 DRAM is isolated (not inserted on the PCB motherboard)
- when the DDR4 DRAM is inserted on the PCB motherboard

Isolated DRAM module: With a specific programming equipment, it is possible to define the A34C04 content, using Byte and Page write instructions, and the write-protection SWP(n) and CWP instructions. To issue the SWP(n) and CWP instructions, the signal applied on SA0 must be driven to V_{HV} during the whole instruction.

DRAM module inserted in the application motherboard: Table 3 and Table 4 show how the Ack bits can be used to identify the write-protection status.

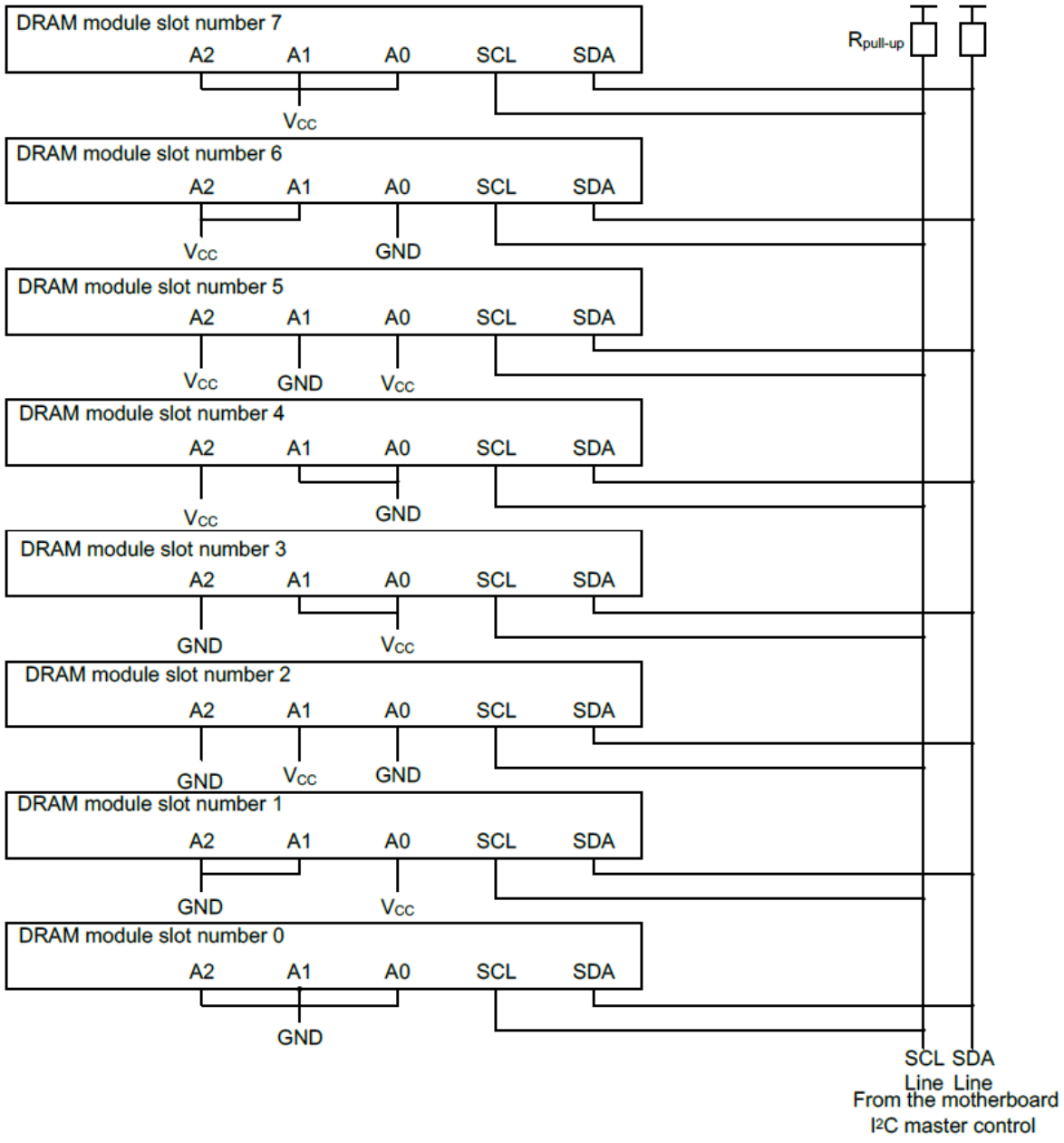
Table 3

Status	Instruction	Ack	Address	Ack	Data byte	Ack	Write cycle (t_W)
Protected	SWPn	NoAck	Not significant	NoAck	Not significant	NoAck	No
	CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write in protected block	Ack	Address	Ack	Data	NoAck	No
Not Protected	SWPn or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write	Ack	Address	Ack	Data	Ack	Yes

Table 4

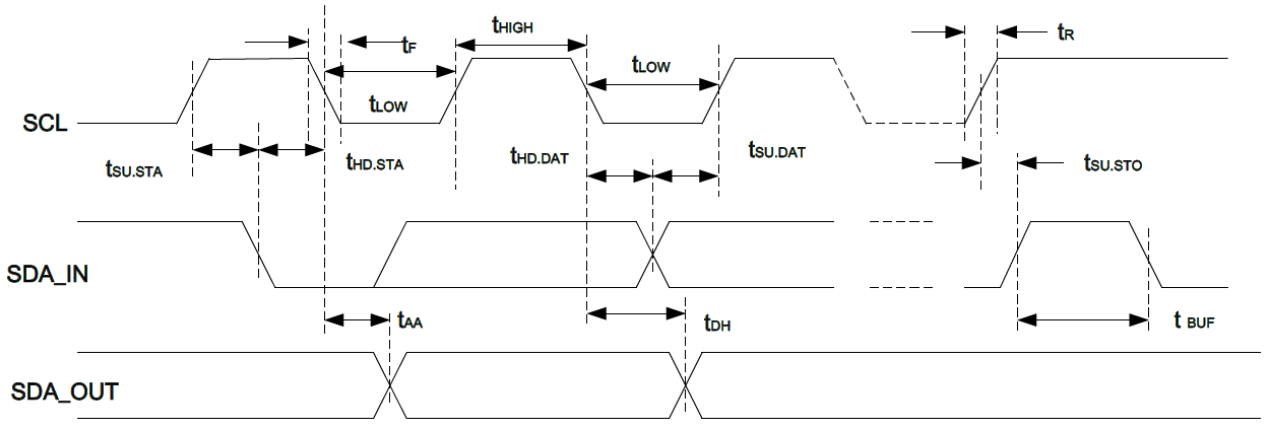
SWPn Status	Instruction	Ack	Address	Ack	Data byte	Ack
Set	RPSn	NoAck	Not significant	NoAck	Not significant	NoAck
Not set	RPSn	Ack	Not significant	NoAck	Not significant	NoAck

Figure 9


DRAM module slot number 7
A2 A1 A0 SCL SDA
Vcc
DRAM module slot number 6
A2 A1 A0 SCL SDA
Vcc GND
DRAM module slot number 5
A2 A1 A0 SCL SDA
Vcc GND Vcc
DRAM module slot number 4
A2 A1 A0 SCL SDA
Vcc GND
DRAM module slot number 3
A2 A1 A0 SCL SDA
GND Vcc
DRAM module slot number 2
A2 A1 A0 SCL SDA
GND Vcc GND
DRAM module slot number 1
A2 A1 A0 SCL SDA
GND Vcc
DRAM module slot number 0
A2 A1 A0 SCL SDA
GND
Rpull-up
SCL Line
SDA Line
From the motherboard
I2C master control

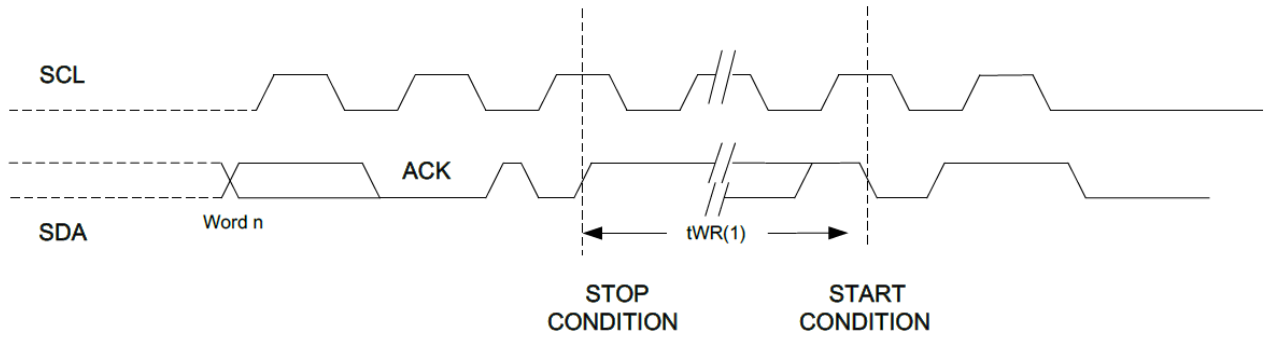
Bus Timing

Figure 10. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

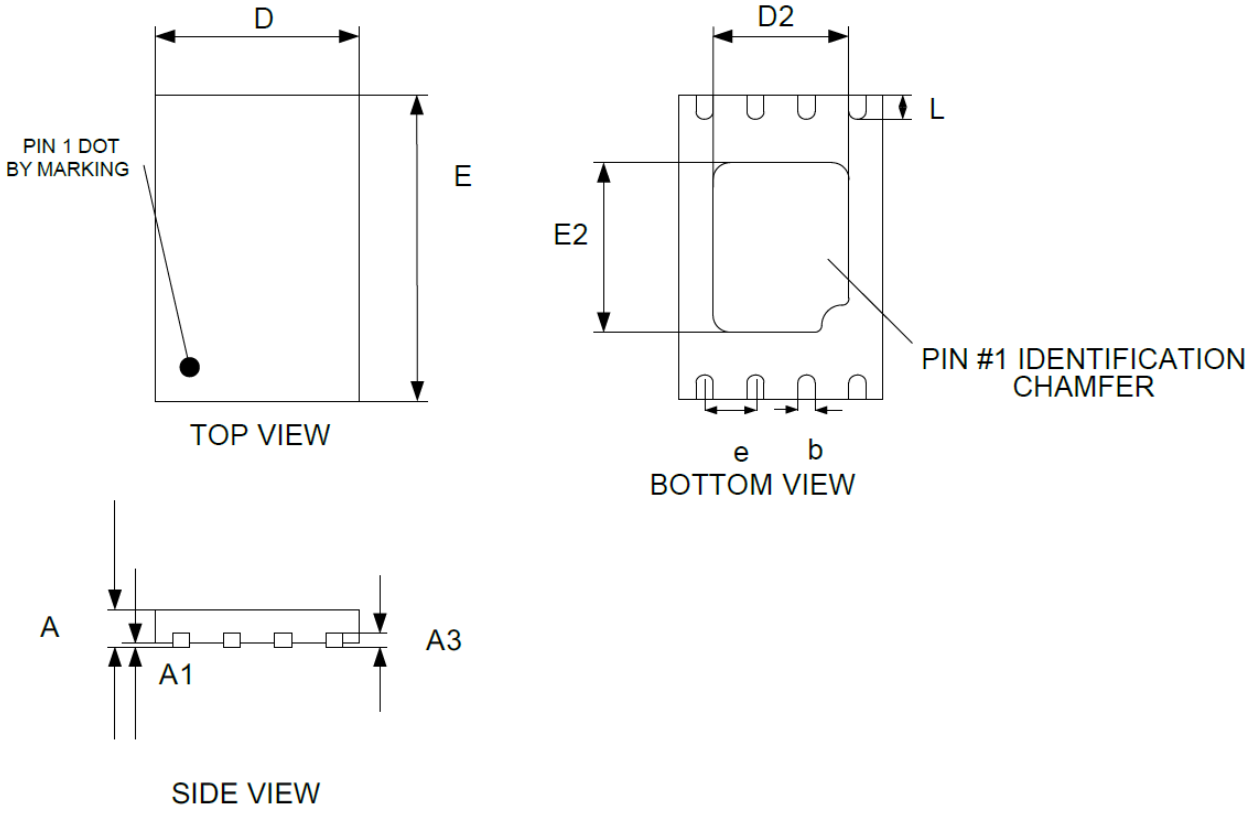
Figure 11. SCL: Serial Clock, SDA: Serial Data I/O



NOTE: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

PACKAGE INFORMATION

Dimension in DFN8 (Unit: mm)



Symbol	UT:ULTRA THIN	
	Min	Max
A	0.50	0.60
A1	0.00	0.05
A3	0.15REF	
D	1.95	2.05
E	2.95	3.05
b	0.20	0.30
L	0.20	0.40
D2	1.25	1.50
E2	1.15	1.40
e	0.50BSC	

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