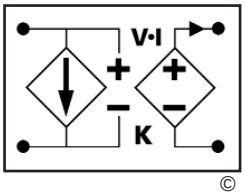


V•I Chip™ – BCM Bus Converter Module

B048K120T15[1]

- 48V to 12V V•I Chip Converter
- 150 Watt (225 Watt for 1 ms)
- High density – up to 600 W/in³
- Small footprint – 150 W/in²
- Low weight – 0.4 oz (12 g)
- Pick & Place / SMD
- >96% efficiency
- 125°C operation
- <1 µs transient response
- >3.5 million hours MTBF
- No output filtering required
- V•I Chip BGA package



©

Vin = 42 - 53 V
Vout = 10.5 - 13.25 V
Iout = 12.5 A
K = 1/4
Rout = 32 mΩ max



Actual size

Product Description

The V•I Chip Bus Converter Module (BCM) is a high efficiency (>96%), narrow input range Voltage Transformation Module (VTM) operating from a pre-regulated 48 Vdc primary bus to deliver an isolated 12 V secondary for Intermediate Bus Architecture applications. The BCM may be used to power non-isolated POL converters or as an independent 12 V source. Due to the fast response time and low noise of the BCM, the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters is reduced—or eliminated—resulting in savings of board area, materials and total system cost.

The BCM achieves a power density of 600 W/in³ and may be surface mounted with a profile as low as 0.16" (4mm) over the PCB. Its V•I Chip power BGA package is compatible with on-board or in-board surface mounting. The V•I Chip package provides flexible thermal management through its low Junction-to-Case and Junction-to-BGA thermal resistance. Owing to its high conversion efficiency and safe operating temperature range, the BCM does not require a discrete heat sink in typical applications. It is also compatible with heat sink options, assuring low junction temperatures and long life in the harshest environments.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60.0	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
TM to -In	-0.3 to 7.0	Vdc	
SG to -In	500	mA	
+Out to -Out	-0.5 to 15.0	Vdc	
Isolation voltage	1500	Vdc	Input to Output
Operating junction temperature	-40 to 125	°C	See note 2
Output current	12.5	A	Continuous
Peak output current	18.7	A	For 1 ms
Case temperature during reflow	208	°C	
Storage temperature	-40 to 150	°C	
Output power	150	W	Continuous
Peak output power	225	W	For 1 ms

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Junction-to-case	1.1	1.5	°C/W
$R_{\theta JB}$	Junction-to-BGA	2.1	2.5	°C/W
$R_{\theta JA}$	Junction-to-ambient[3]	6.5	7.2	°C/W
$R_{\theta JA}$	Junction-to-ambient[4]	5.0	5.5	°C/W

Notes

1. For complete product matrix see chart on page 10.
2. The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by the temperature monitor (TM) signal and by a shutdown comparator.
3. B048K120T15 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
4. B048L120T15 (0.25"H integral Pin Fins) surface mounted on FR4 board, 300 LFM.

PRELIMINARY

INPUT (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	42	48	53	V	
Input dV/dt			10	V/µs	
Input undervoltage turn-on			42	V	
Input undervoltage turn-off	37			V	
Input overvoltage turn-on	53			V	
Input overvoltage turn-off			59	V	
Input quiescent current		1.5	1.8	mA	PC low
Inrush current overshoot		0.8		A	Using test circuit in Fig.24; See Fig.1
Input current			3.5	A	
Input reflected ripple current		40	60	mA p-p	Using test circuit in Fig.24; See Fig.4
No load power dissipation		1.9	3.0	W	See Fig.6
Internal input capacitance		4		µF	
Internal input inductance		20		nH	
Recommended external input capacitance	8			µF	200 nH maximum source inductance; See Fig.24

PRELIMINARY

INPUT WAVEFORMS

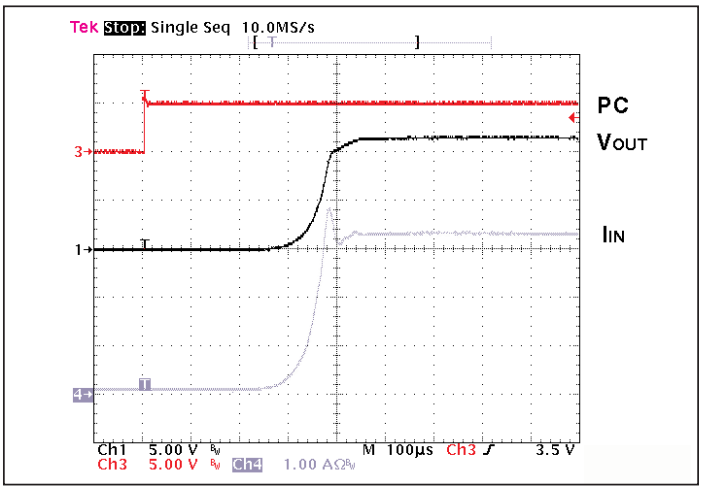


Figure 1— *Inrush transient current at full load and nominal V_{IN} with PC enabled*

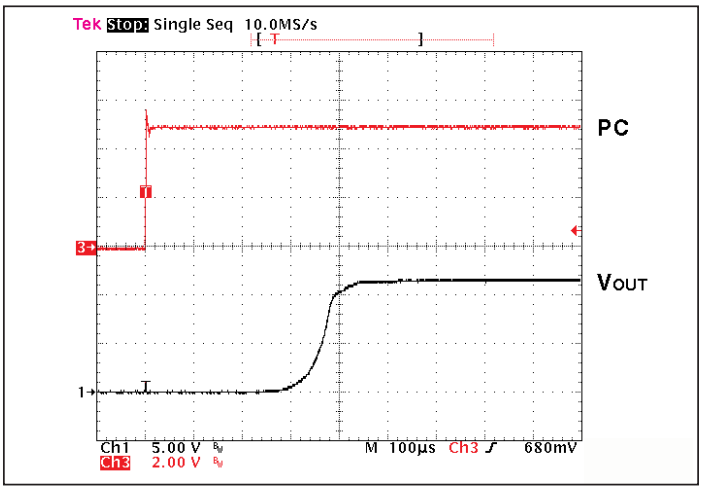


Figure 2— *Output voltage turn-on waveform with PC enabled at full load and nominal V_{IN}*

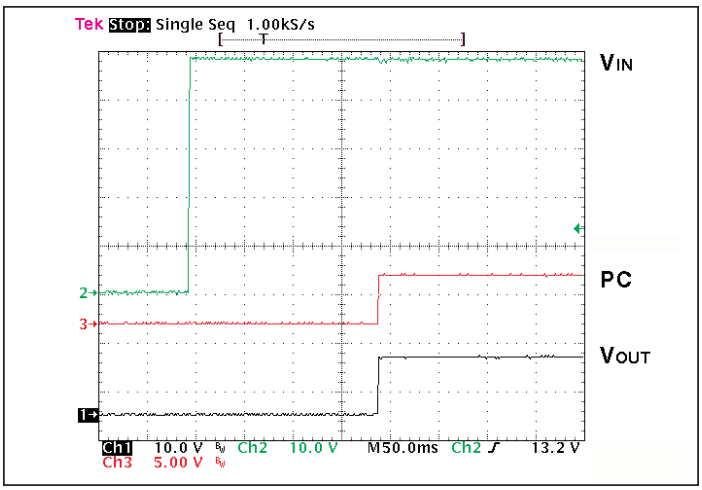


Figure 3—*Output voltage turn-on waveform with input turn-on at full load and nominal V_{IN}*

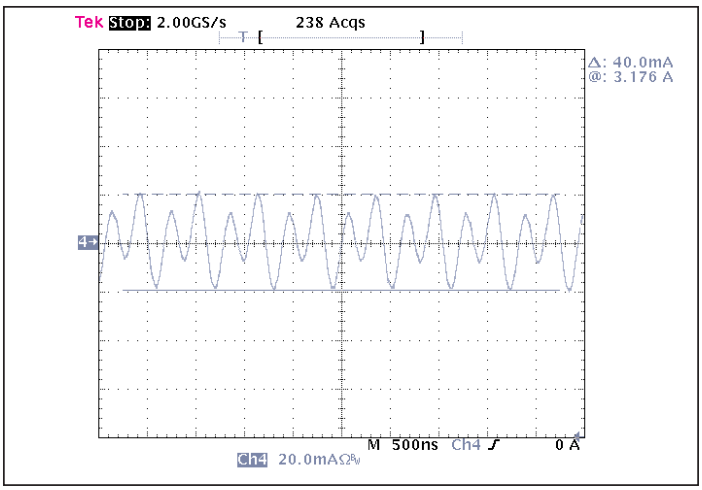


Figure 4— *Input reflected ripple current at full load and nominal V_{IN}*

OUTPUT (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Rated DC current	0		12.5	A	
Peak repetitive current			18.7	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
DC current limit	12.5	16.0	20.0	A	
Current share accuracy		5	10	%	See Parallel Operation on page 11
Efficiency					
Half load	95.0	95.8		%	See Fig.5
Full load	95.0	96.0		%	See Fig.5
Internal output inductance		1.6		nH	
Internal output capacitance		12		µF	Effective value
Load capacitance			1000	µF	
Output overvoltage setpoint		14.75		V	
Output ripple voltage					
No external bypass		90	150	mV	See Figs.7 and 10
1µF bypass capacitor		8		mV	See Fig.8
Average short circuit current		200		mA	
Effective switching frequency	2.8	3.5	4.2	MHz	Fixed, 1.75 MHz per phase
Line regulation					
K	0.245	0.250	0.255		$V_{OUT}=K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}			32	mΩ	See Figs.9 and 28
Transient response					
Voltage undershoot		148		mV	0-12.5A load step, w/Cin = 100µF, see Fig.11
Voltage overshoot		144		mV	12.5-0A load step, w/Cin = 100µF, see Fig.12
Response time		200		ns	See Figs.11 and 12
Recovery time		1		µs	See Figs.11 and 12
Output overshoot					
Input turn-on		0		mV	No output filter; See Fig.2
PC enable		0		mV	No output filter; See Fig.3
Output turn-on delay					
From application of power		160	300	ms	See Fig.3
From release of PC pin		320	410	µs	See Fig.2

PRELIMINARY

OUTPUT WAVEFORMS

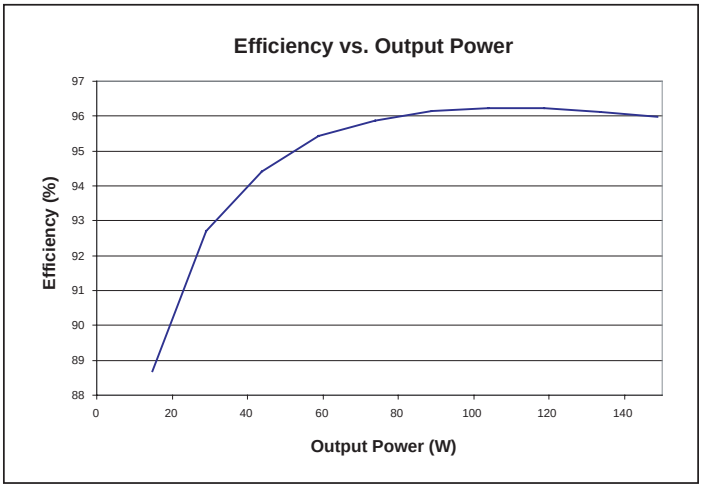


Figure 5— *Efficiency vs. output power at nominal V_{IN}*

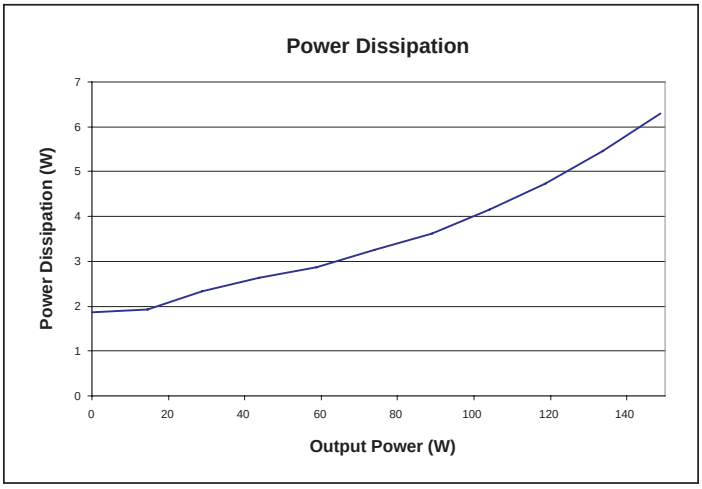


Figure 6—*Power dissipation as a function of output power*

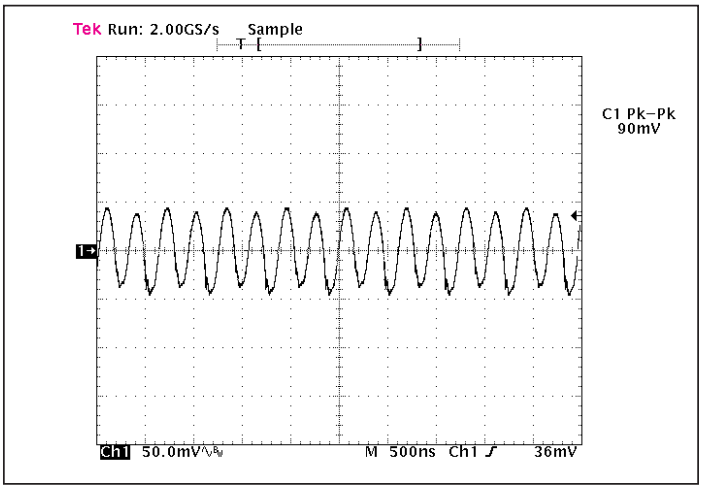


Figure 7*— Output voltage ripple at full load and nominal V_{IN}; without any external bypass capacitor.*

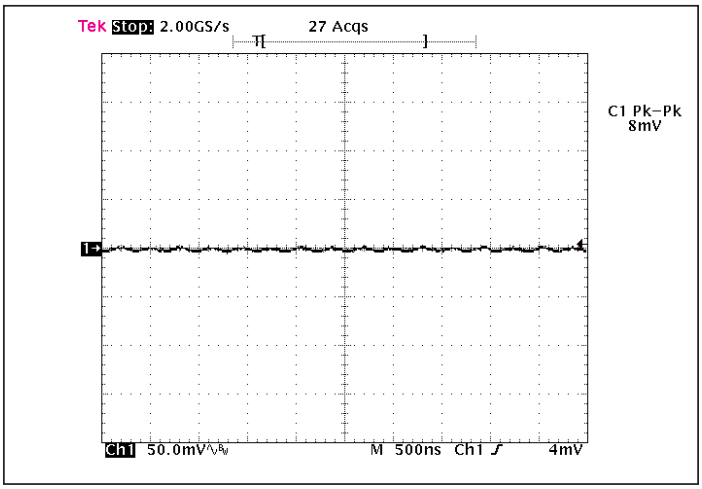


Figure 8*—Output voltage ripple at full load and nominal V_{IN} with 1 µF ceramic external bypass capacitor.*

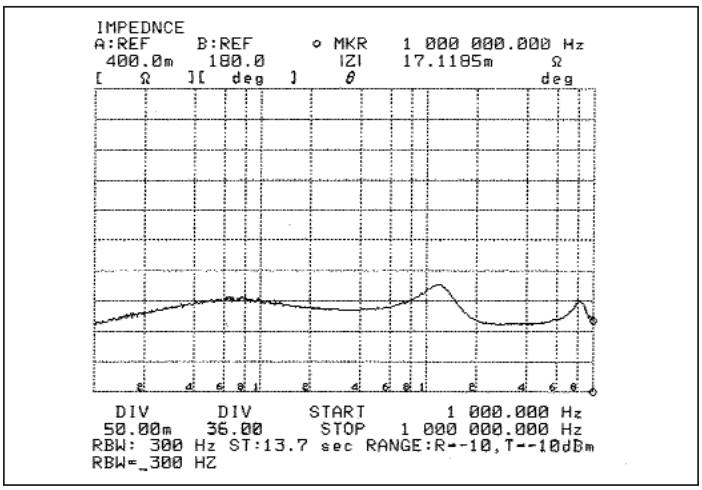


Figure 9*— Output impedance vs. frequency*

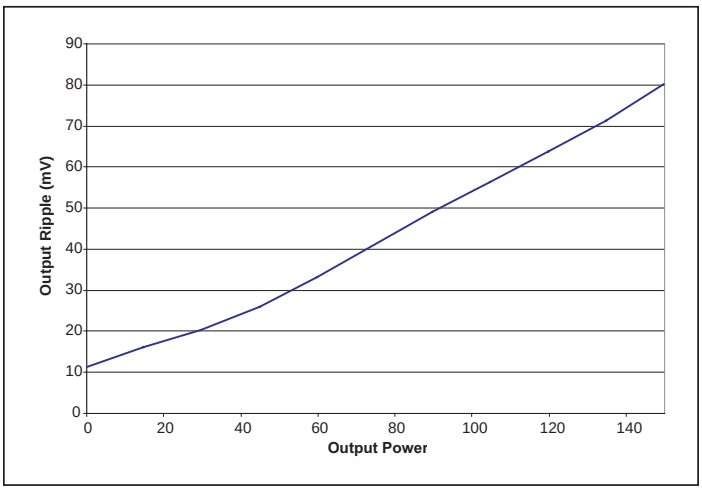


Figure 10*— Output voltage ripple vs. output power at nominal line without any external bypass capacitor.*

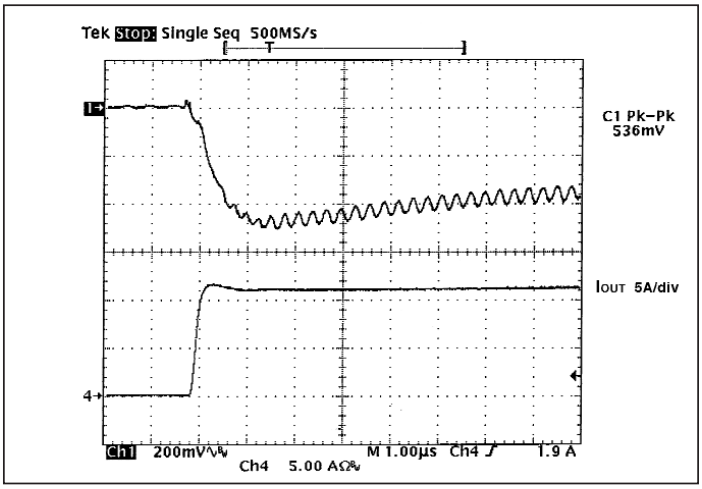


Figure 11*— 0-12.5A transient response with no external bypass capacitance.*

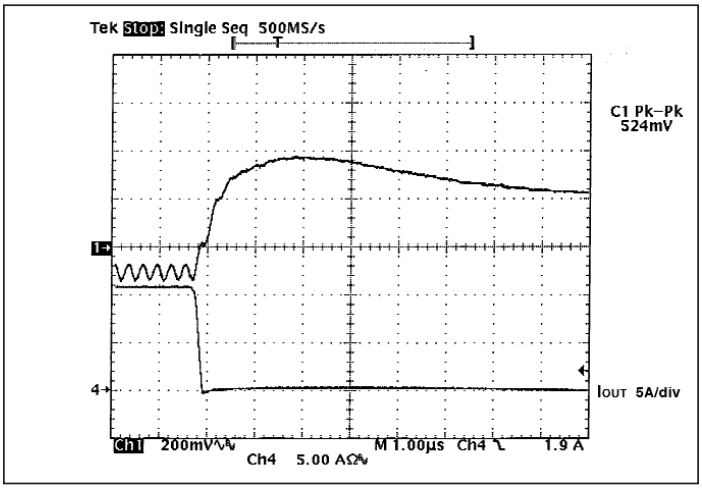


Figure 12*— 12.5-0A transient response with no external bypass capacitance.*

GENERAL

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.6		Mhrs	25°C, GB
Telcordia TR-NT-000332		4.2		Mhrs	
Telcordia SR-332		TBD		hrs	
Demonstrated		TBD		hrs	
Isolation specifications					
Voltage	1,500			Vdc	Input to Output
Capacitance		5,000	6,500	pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals(pending)		cTÜVus			UL/CSA 60950, EN 60950
		CE Mark			Low Voltage Directive
Mechanical parameters					See mechanical drawing, Figs.16 and 18
Weight		0.43 / 12.25		oz / g	
Dimensions					
Length		1.26 / 32		in / mm	
Width		0.85 / 21.5		in / mm	
Height		0.24 / 6		in / mm	

PRELIMINARY

Auxiliary Pins (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary control (PC)					
DC voltage	4.8	5.0	5.2	V	
Module disable voltage	2.4	2.5		V	
Module enable voltage		2.5	2.6	V	
Current limit	2.4	2.5	2.9	mA	Source only
Enable delay time		320	410	µs	See Fig. 2
Disable delay time		16	40	µs	See Fig. 13
Temperature Monitor (TM)					
27°C setting	2.95	3.00	3.05	V	Operating junction temperature
Temperature coefficient		10		mV/°C	
Full range accuracy	-5		5	°C	Operating junction temperature
Current limit	100			µA	Source only

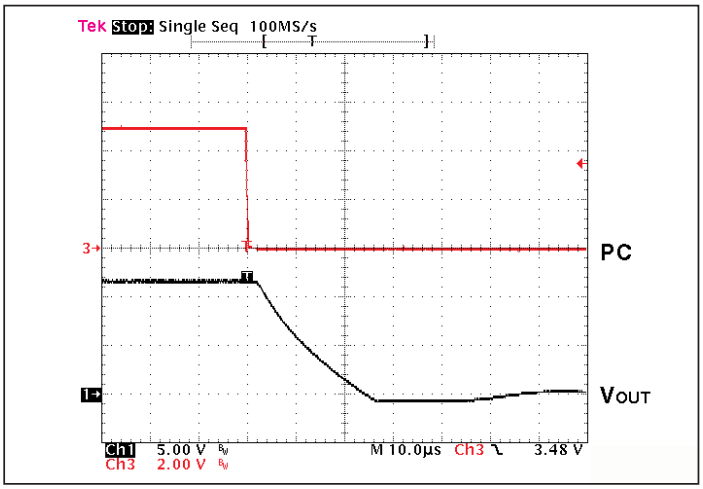


Figure 13— *VOUT at full load vs. PC disable*

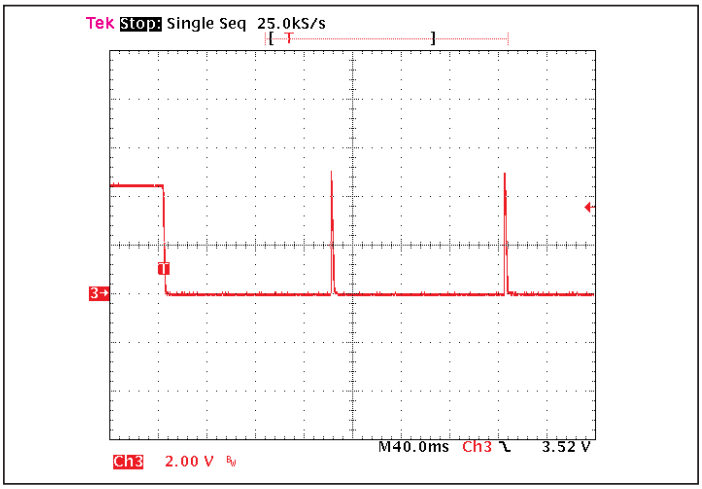


Figure 14— *PC signal during fault*

THERMAL

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Over temperature shutdown	125	130	135	°C	Junction temperature
	Thermal capacity		0.61		Ws/°C	
$R_{\theta JC}$	Junction-to-case thermal impedance		1.1	1.5	°C/W	
$R_{\theta JB}$	Junction-to-BGA thermal impedance		2.1	2.5	°C/W	
$R_{\theta JA}$	Junction-to-ambient [1]		6.5	7.2	°C/W	
$R_{\theta JA}$	Junction-to-ambient [2]		5.0	5.5	°C/W	

Notes

1. B048K120T15 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
2. B048L120T15 (0.25"H integral Pin Fins) surface mounted on FR4 board, 300 LFM.

V•I CHIP STRESS DRIVEN PRODUCT QUALIFICATION PROCESS

Test	Standard	Environment
High Temperature Operational Life (HTOL)	JESD22-A-108-B	125°C, Vmax, 1,008 hrs
Temperature Cycling	JESD22-A-104B	-55°C to 125°C, 1,000 cycles
High Temperature Storage	JESD22-A-103A	150°C, 1,000 hrs
Moisture Resistance	JESD22-A113-B	Moisture Sensitivity Level 4
Temperature Humidity Bias Testing (THB)	EIA/JESD22-A-101-B	85°C, 85% RH, Vmax, 1,008 hrs
Pressure Cooker Testing (Autoclave)	JESD22-A-102-C	121°C, 100% RH, 15 PSIG, 96 hrs
Highly Accelerated Stress Testing (HAST)	JESD22-A-110B	130°C, 85% RH, Vmax, 96 hrs
Solvent Resistance/Marking Permanency	JESD22-B-107-A	Solvents A, B & C as defined
Mechanical Vibration	JESD22-B-103-A	20g peak, 20-2,000 Hz, test in X, Y & Z directions
Mechanical Shock	JESD22-B-104-A	1,500g peak 0.5 ms pulse duration, 5 pulses in 6 directions
Electro Static Discharge Testing – Human Body Model	EIA/JESD22-A114-A	Meets or exceeds 2,000 Volts
Electro Static Discharge Testing – Machine Model	EIA/JESD22-A115-A	Meets or exceeds 200 Volts
Highly Accelerated Life Testing (HALT)	Per Vicor Internal Test Specification	Operation limits verified, destruct margin determined
Dynamic Cycling	Per Vicor Internal Test Specification	Constant line, 0-100% load, -20°C to 125°C

V•I CHIP BALL GRID ARRAY INTERCONNECT QUALIFICATION

Test	Standard	Environment
BGA Daisy-Chain Thermal Cycling	IPC-SM-785 IPC-9701	TC3, -40 to 125°C at <10 °C/min, 10 min dwell time.
Ball Shear	IPC-9701 IPC J-STD-029	No failure through intermetallic.
Bend Test	IPC J-STD-029	Deflection through 4 mm.

+IN/-IN – DC Voltage Input Ports
The V•I Chip input voltage range should not be exceeded. An internal under/over voltage lockout-function prevents operation outside of the normal operating input range. The BCM turns ON within an input voltage window bounded by the "Input under-voltage turn-on" and "Input over-voltage turn-off" levels, as specified. The V•I Chip may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 8 µF in series with 0.3Ω.

SG – Signal Ground
The Signal Ground provides a Kelvin return for the PC and TM ports. It is internally connected to the –IN port. The SG connection is not sized to carry the –IN current and cannot be a substitute for the –IN port, which must be connected with low interconnect impedance.

PC – Primary Control
The Primary Control port is a multifunction node that provides the following functions:

Enable/Disable – If the PC port is left floating or is at a logic HI, the BCM output is enabled. Once this port is pulled lower than 2.4 Vdc with respect to SG, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. Refer to Figures 1-3, 13 and 14 for the typical Enable/Disable characteristics. This port should not be toggled at a rate higher than 1 Hz.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5.0 Vdc.

Alarm – The BCM contains watchdog circuitry that monitors output overload, input over voltage or under voltage, and internal junction temperatures. In response to an abnormal condition in any of the monitored parameters, the PC port will toggle. Refer to Figure 14 for PC alarm characteristics.

TM – Temperature Monitor
The Temperature Monitor port monitors the highest junction temperature of the BCM. This output may be used to provide feedback and validation of the thermal management of V•I Chips, as applied in diverse power systems and environments.

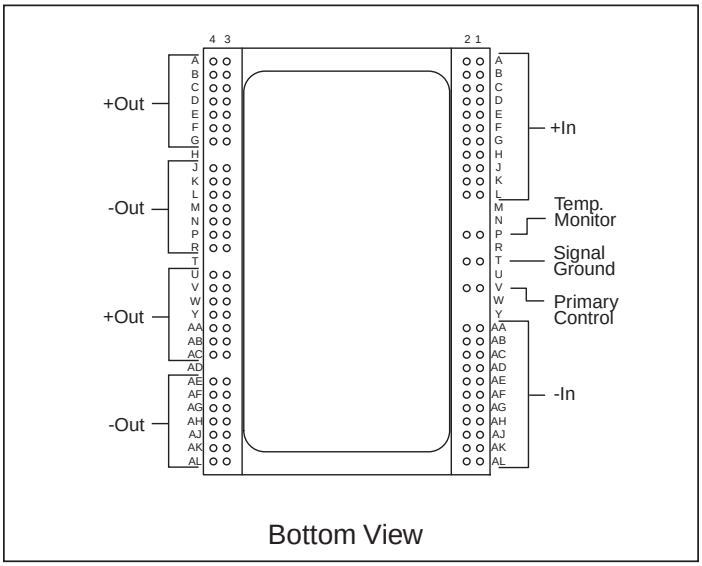


Figure 15*—BCM BGA configuration*

Signal Name	BGA Designation
+In	A1-L1, A2-L2
–In	AA1-AL1, AA2-AL2
TM	P1, P2
SG	T1, T2
PC	V1, V2
+Out	A3-G3, A4-G4, U3-AC3, U4-AC4
–Out	J3-R3, J4-R4, AE3-AL3, AE4-AL4

At 300 °K (+27 °C), the TM output is nominally 3.0 Vdc. The TM output is proportional to temperature and varies at 10 mV/°C. The TM accuracy is +/-5 °C. SG should be used as ground return of the TM signal to maintain the specified accuracy.

+OUT/-OUT – DC Voltage Output Ports
Two sets of contacts are provided for the +OUT port. They must be connected in parallel with low interconnect resistance. Similarly, two sets of contacts are provided for the –OUT port. They must be connected in parallel with low interconnect resistance. Within the specified operating range, the average output voltage is defined by the Level 1 DC behavioral model of Figure 28. The current source capability of the BCM is rated in the specifications section of this document.

The low output impedance of the BCM, see Figure 9, reduces or eliminates the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters.

Total load capacitance at the output of the BCM should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM (see Figure 9), low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM.

PRELIMINARY

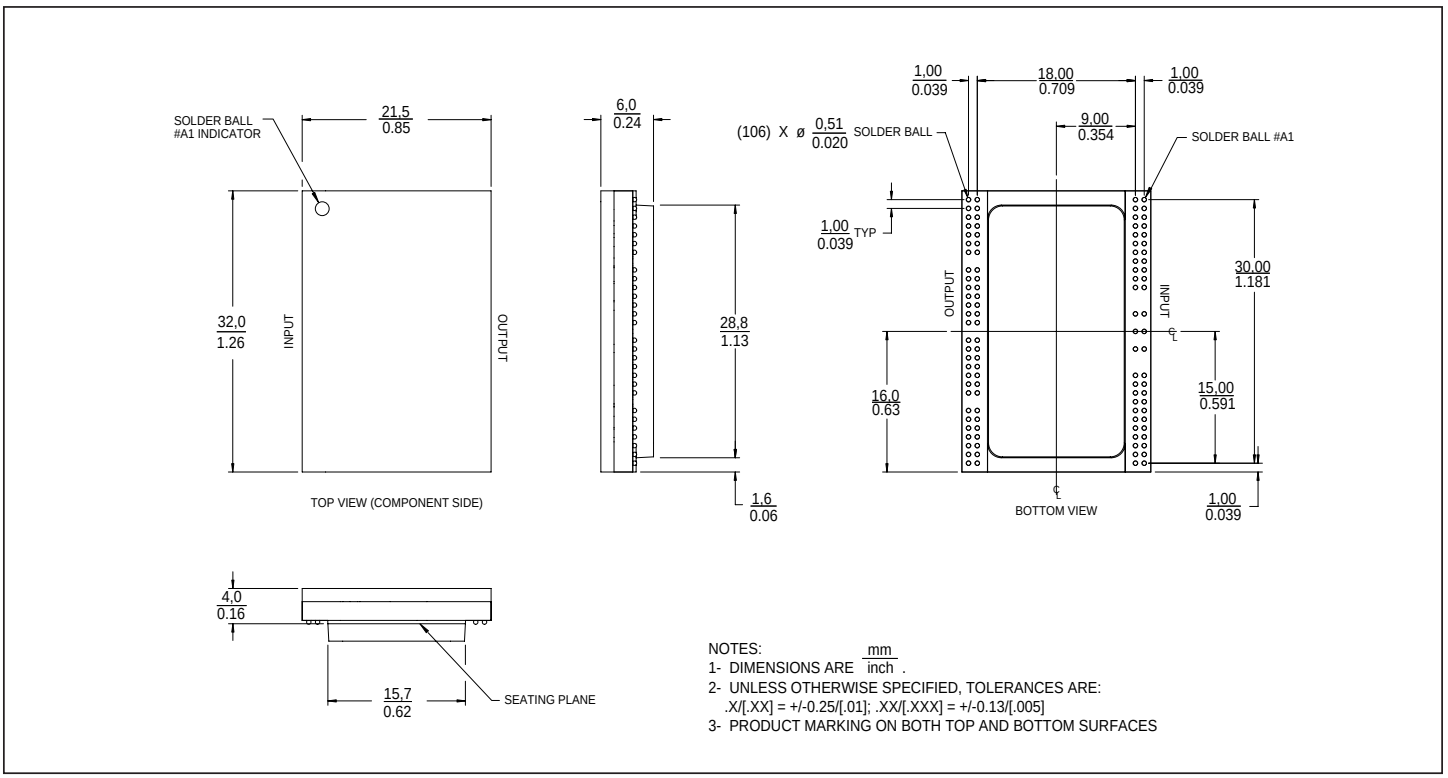


Figure 16*—BCM BGA mechanical outline; In-board mounting*

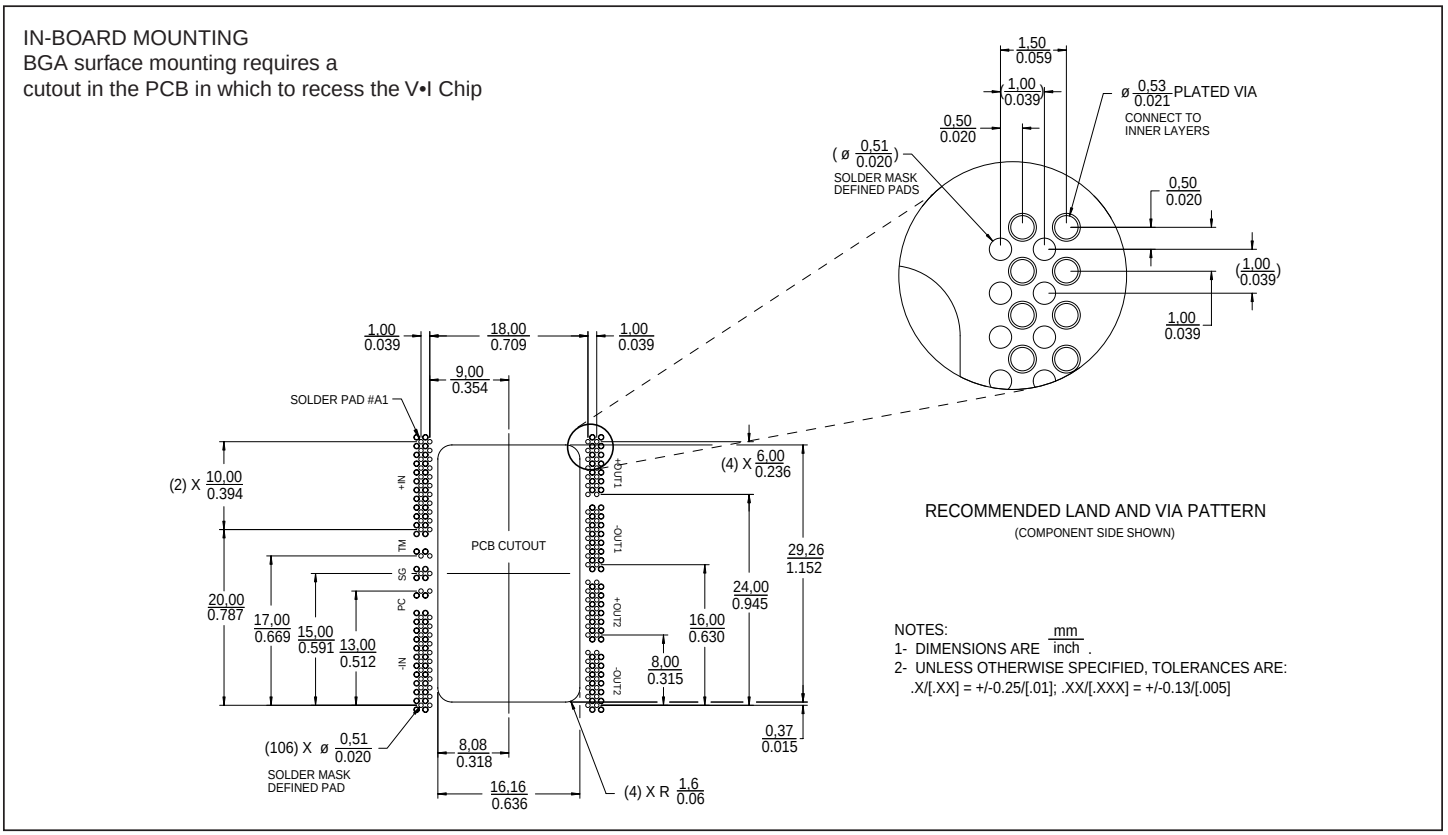


Figure 17*—BCM BGA PCB land/VIA layout information; In-board mounting*

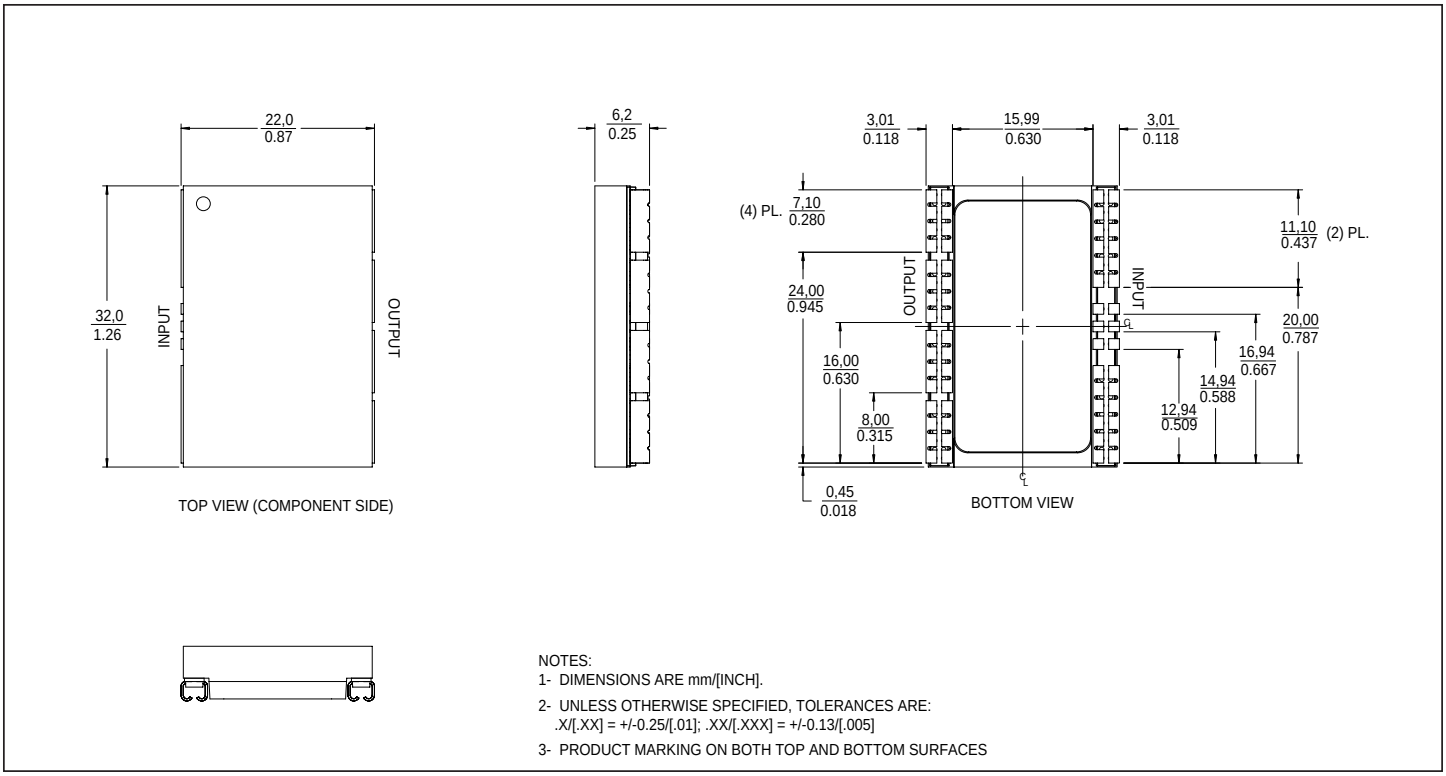


Figure 18*—BCM J-lead mechanical outline; On-board mounting*

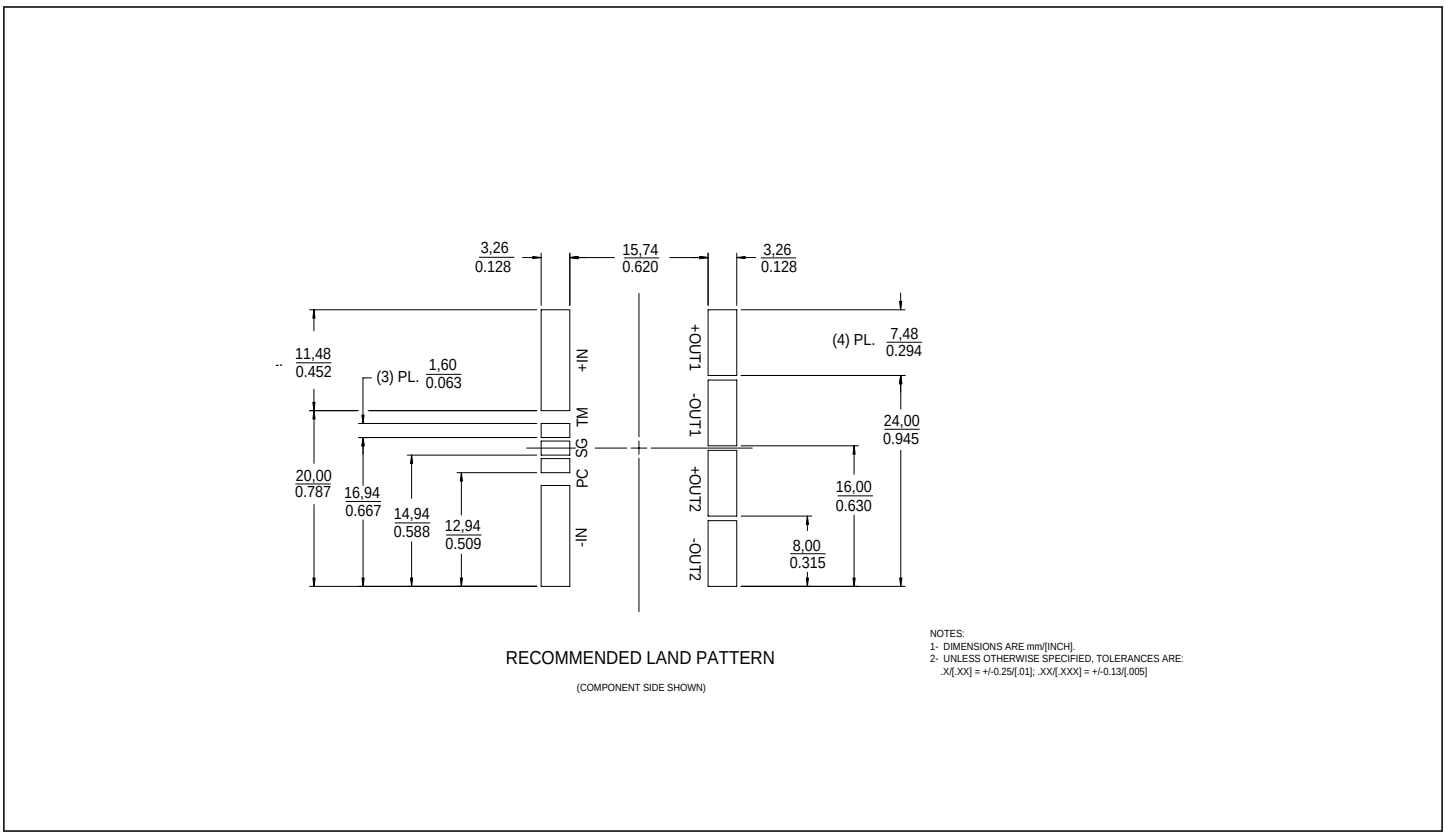


Figure 19*— BCM J-lead PCB land layout information; On-board mounting*

V•I Chip BUS CONVERTER PART NUMBERING

B	048	K	120	T	15
Bus Converter Module	Input Voltage Designator	Configuration Options F = On-board (Fig.21) G = On-board with 0.25" Integral Pin Fins (Fig.23) K = In-board (Fig.20) L = In-board with 0.25" Integral Pin Fins (Fig.22)	Output Voltage Designator (=Vout x10)	Product Grade Temperatures (°C) Grade: T Storage: -40 to150 Operating: -40 to125	Output Power Designator (=Pout/10) NOTE: 100W and 200W versions are also available.

CONFIGURATION OPTIONS

CONFIGURATION	IN-BOARD*	ON-BOARD*	IN-BOARD WITH 0.25" PIN FINS**	ON-BOARD WITH 0.25" PIN FINS**
Effective Power Density	875 W/in^3	547 W/in^3	304 W/in^3	244 W/in^3
Junction-Board Thermal Resistance	2.1 °C/W	2.4 °C/W	2.1 °C/W	2.4 °C/W
Junction-Case Thermal Resistance	1.1 °C/W	1.1 °C/W	N/A	N/A
Junction-Ambient Thermal Resistance 300LFM	6.5 °C/W	6.8 °C/W	5.0 °C/W	5.0 °C/W
BCM Model No.	B048K120T15	B048F120T15	B048L120T15	B048G120T15

*Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu

**Pin Fin heat sink also available as a separate item

PRELIMINARY

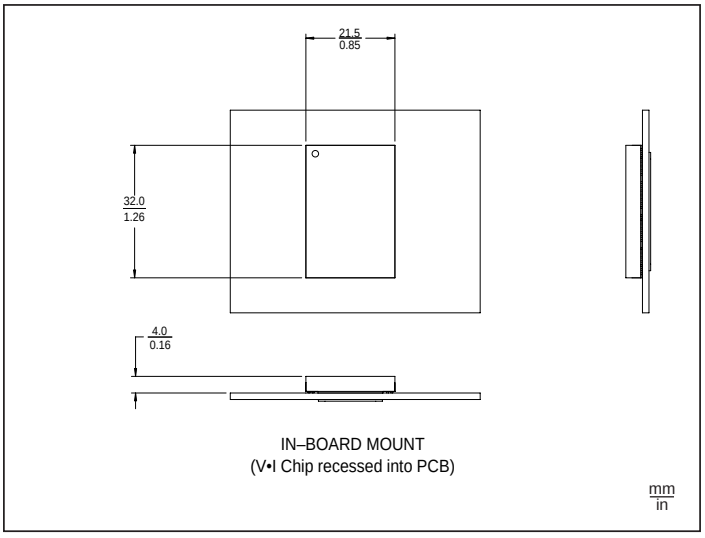


Figure 20*—In-board mounting – package K*

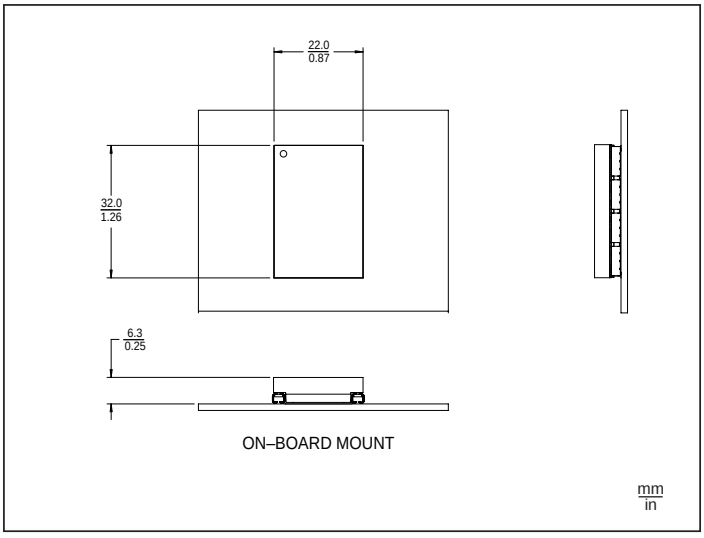


Figure 21*—On-board mounting – package F*

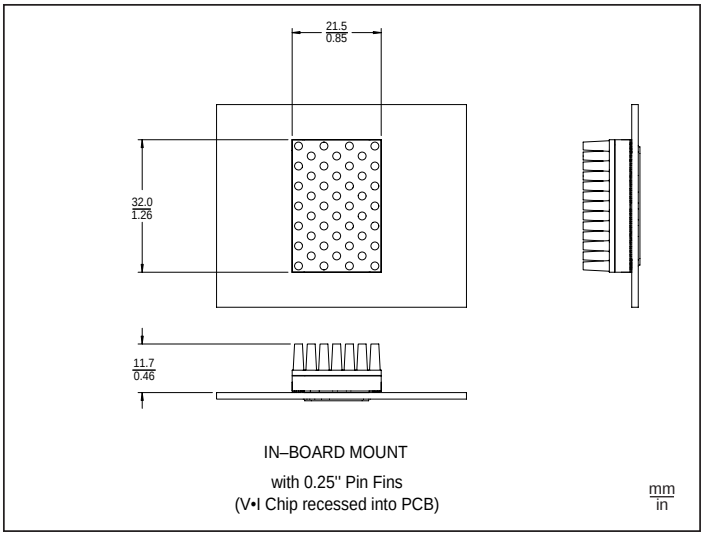


Figure 22*— In-board with pin fins – package L*

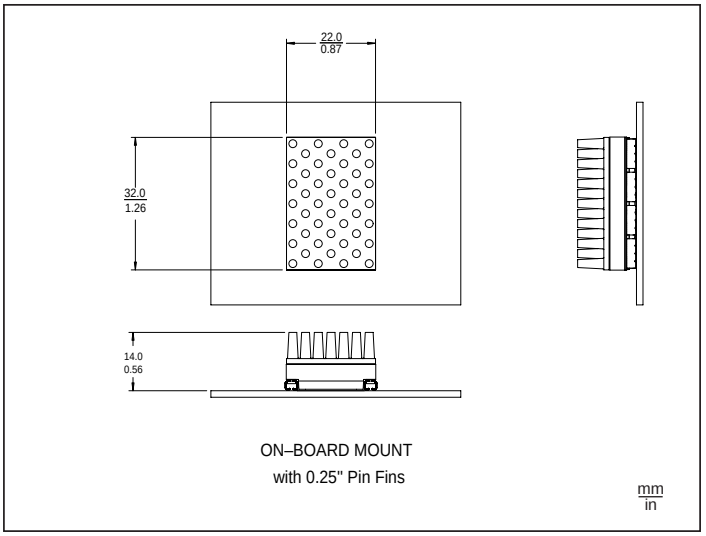


Figure 23*— On-board with pin fins – package G*

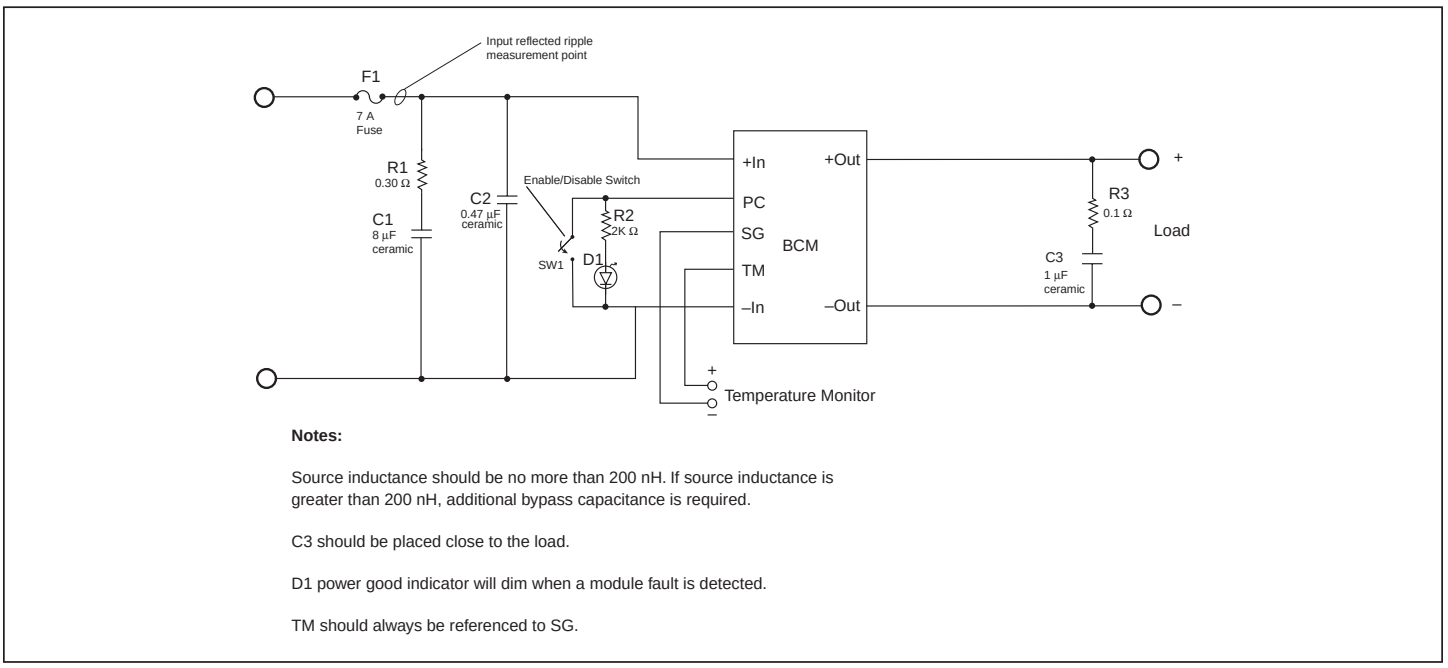


Figure 24*—BCM test circuit*

Application Note

Parallel Operation

The BCM will inherently current share when properly configured in an array of BCMs. Arrays may be used for higher power or redundancy in an application.

Current sharing accuracy is maximized when the source and load impedance presented to each BCM within an array are equal.

The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

The BCM power train and control architecture allow bi-directional power transfer, including reverse power processing from the BCM output to its input. Reverse power transfer is enabled if the BCM input is within its operating range and the BCM is otherwise enabled. The BCM's ability to process power in reverse improves the BCM transient response to an output load dump.

Thermal Management

The high efficiency of the V•I Chip results in relatively low power dissipation and correspondingly low generation of heat. The heat generated within internal semiconductor junctions is coupled with low effective thermal resistances, $R\theta_{JC}$ and $R\theta_{JB}$, to the V•I Chip case and its Ball Grid Array allowing thermal management flexibility to adapt to specific application requirements (Fig. 25).

CASE 1 Convection via optional Pin Fins to air (Pin Fins available mounted to the V•I Chip or as a separate item.)

If the application is in a typical environment with forced convection over the surface of the PCB and greater than 0.4" headroom, a simple thermal management strategy is to procure V•I Chips with the Pin Fin option. The total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, of a surface mounted V•I Chip with integral 0.25" Pin Fins is 5 °C/W in 300 LFM air flow (Fig.27). At full rated output power of 150 W, the heat generated by the BCM is approximately 6 W (Fig.6). Therefore, the junction temperature rise to ambient is approximately 30°C. Given a maximum junction temperature of 125°C, a temperature rise of 30°C allows the V•I Chip to operate at rated output power at up to 95°C ambient temperature. At 75 W of output power, operating ambient temperature extends to 105°C.

CASE 2—Conduction to the PCB

The low thermal resistance Junction-to-BGA, $R\theta_{JB}$, allows use of the PCB to exchange heat from the V•I Chip, including convection from the PCB to the ambient or conduction to a cold plate.

For example, with a V•I Chip surface mounted on a 2" x 2" area of a multi-layer PCB, with an aggregate 8 oz of effective copper weight, the total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, is 6.5 °C/W in 300 LFM air flow (see Thermal Resistance section, page 1). Given a maximum junction temperature of 125°C and 6 W dissipation at 150 W of output power, a temperature rise of 39°C allows the V•I Chip to operate at rated output power at up to 86°C ambient temperature.

The thermal resistance of the PCB to the surrounding environment in proximity to V•I Chips may be reduced by low profile heat sinks surface mounted to the PCB.

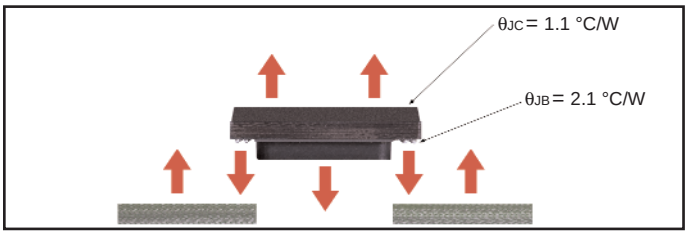


Figure 25*—Thermal resistance*

The PCB may also be coupled to a cold plate by low thermal resistance standoff elements as a means of achieving effective cooling for an array of V•I Chips, without a direct interface to their case.

CASE 3—Combined direct convection to the air and conduction to the PCB.

Parallel use of the V•I Chip internal thermal resistances (including Junction-to-Case and Junction-to-BGA) in series with external thermal resistances provides an efficient thermal management strategy as it reduces total thermal resistance. This may be readily estimated as the parallel network of two pairs of series configured resistors.

The TM (Temperature Monitor) port monitors the V•I Chip junction temperature and provides feedback and validation of the thermal management of V•I Chips, as applied in diverse power systems and environments.

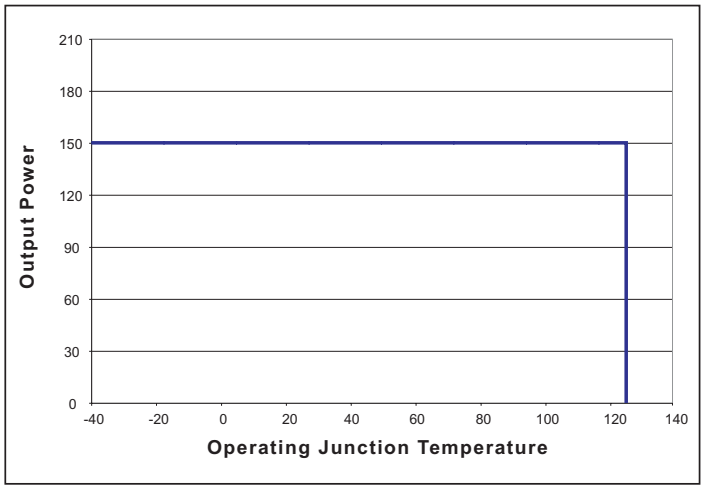


Figure 26*— Thermal derating curve*

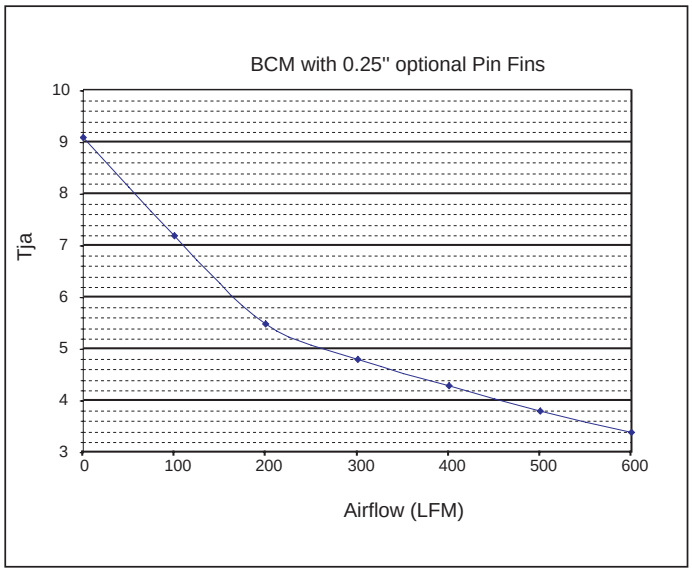


Figure 27*—Junction-to-ambient thermal resistance of BCM with 0.25" Pin Fins (Pin Fins available mounted to the V•I Chip or as a separate item.)*

■ V•I Chip BUS CONVERTER LEVEL 1 DC BEHAVIORAL MODEL for 48V to 12V, 150W

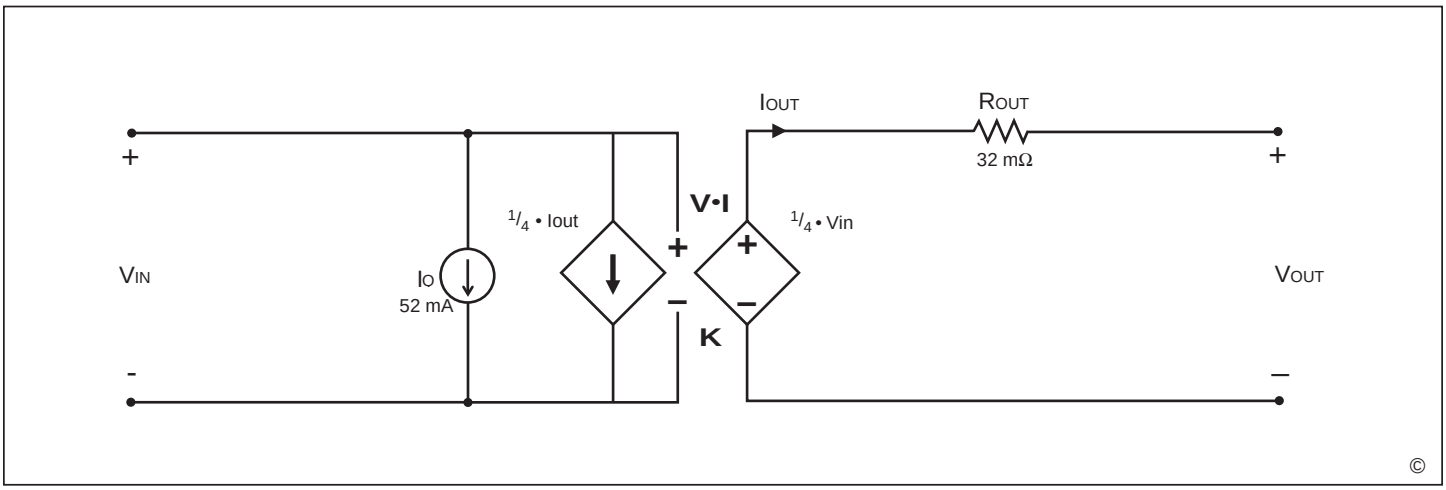


***Figure 28**—This model characterizes the DC operation of the V•I Chip bus converter, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

■ V•I Chip BUS CONVERTER LEVEL 2 TRANSIENT BEHAVIORAL MODEL for 48V to 12V, 150W

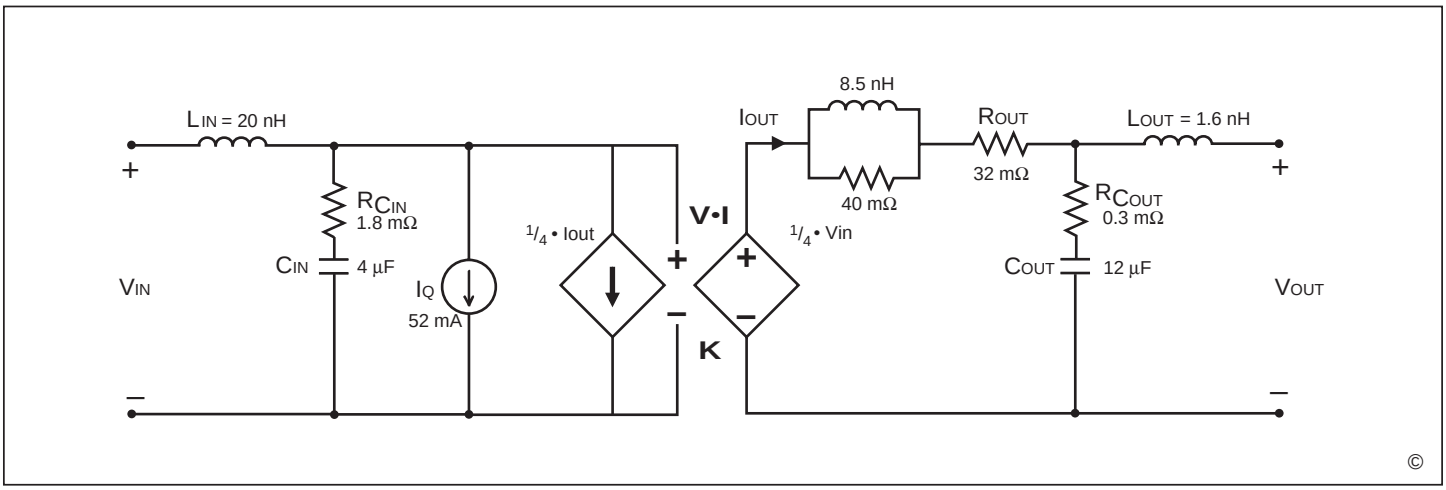


***Figure 29**—This model characterizes the AC operation of the V•I Chip bus converter including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

V•I Chip Handling and Solderability

The product should remain in its package in a dry environment until ready for use.

The following table shows the soldering requirements for both the BGA in-board surface mount package and the J-lead on-board surface mount package.

The reflow process should use industry standard Surface Mount Technology (SMT) conditions. The exact conditions will depend upon the solder paste manufacturer's recommendations. Under no circumstance should the case temperature exceed 208°C. Refer to Fig. 30 for a suggested thermal profile.

	BGA Package	J-Lead Package
Solder Paste	63/37 "No Clean"*	63/37 "No Clean"
Stencil Thickness	4-6 mil	4-6 mil
Stencil Aperture	20 mil; 1:1 ratio	0.8-0.9:1 ratio
Placement	Within 50% of pad center	± 5 mil
Acceleration Rate	<500 in/sec^2	<500 in/sec^2

*Halide free water washable 63/37 Flux paste can be used for the BGA version package only. Please consult our Application Engineers for further information.

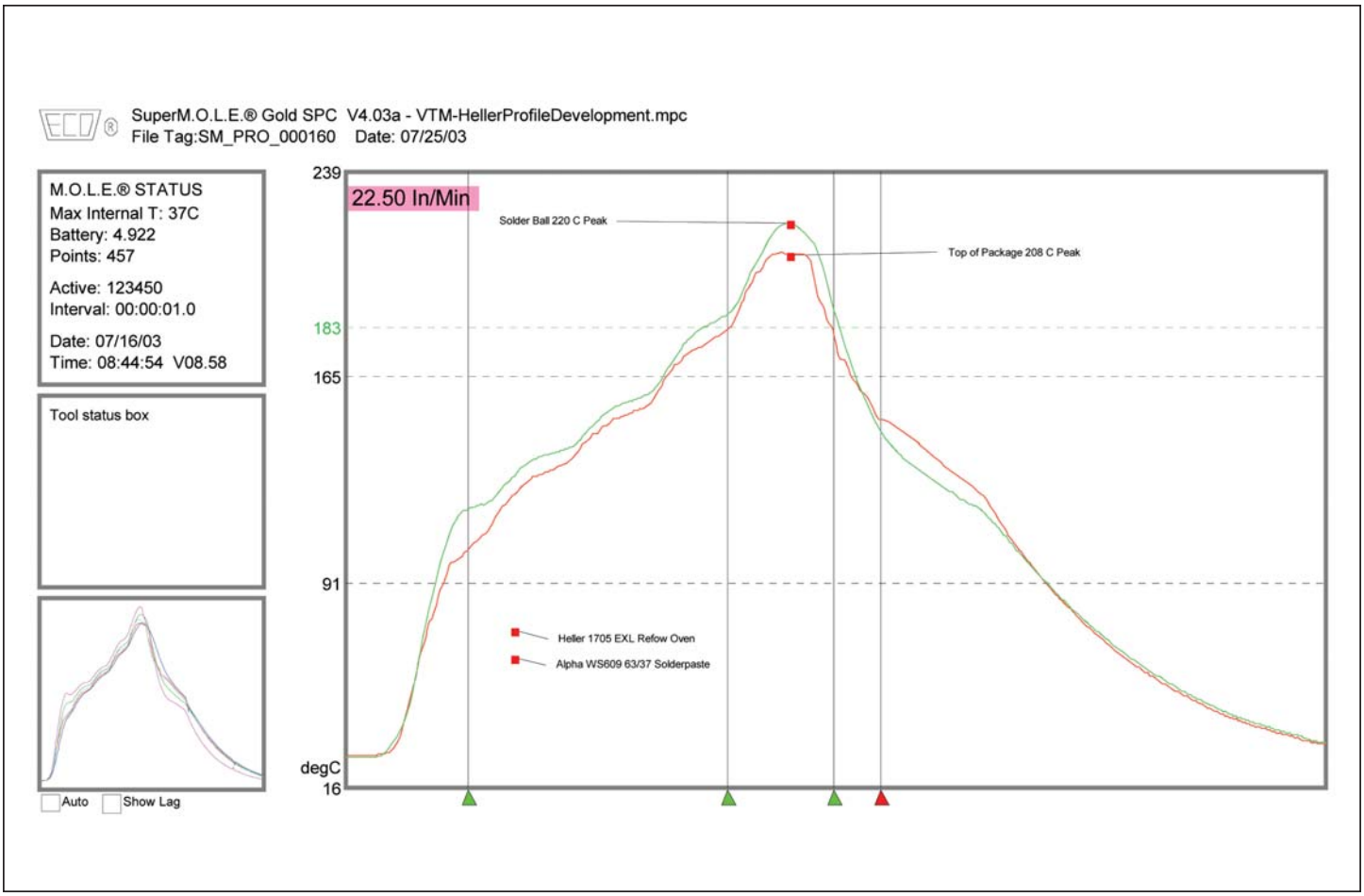


***Figure 30**—Thermal profile diagram*

Input Impedance Recommendations

To take full advantage of the BCM capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance (less than 100 nH) and should have a critically damped response. If the interconnect inductance exceeds 100 nH, the BCM input pins should be bypassed with an RC damper (e.g., 8 µF in series with 0.3 ohm) to retain low source impedance and stable operations. Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the BCM is operated near low or high line as the over/under voltage detection circuitry could be activated.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in power system configuration. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse, such as NANO2 FUSE 451 Series 7 A 125 V, is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +IN port.

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• The electrical and thermal utility of the V•I Chip package

• The design of the V•I Chip package

• The Power Conversion Topology utilized in the V•I Chip package

• The Control Architecture utilized in the V•I Chip package

• The Factorized Power Architecture.

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