Dual, 550kHz, 2-Phase Synchronous Regulators

FEATURES

- **Dual, 180° Phased Controllers Reduce Required Input Capacitance and Power Supply Induced Noise**
- **OPTI-LOOP® Compensation Minimizes C_{OUT}**
- **±1% Output Voltage Accuracy (LTC3728LC)**
- **Power Good Output Voltage Indicator**
- **Phase-Lockable Fixed Frequency 250kHz to 550kHz**
- Dual N-Channel MOSFET Synchronous Drive
- Wide V_{IN} Range: 4.5V to 28V Operation
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Soft-Start Current Ramping
- Foldback Output Current Limiting
- Latched Short-Circuit Shutdown with Defeat Option
- Output Overvoltage Protection
- Low Shutdown I_Q: 20µA
- 5V and 3.3V Standby Regulators
- 3 Selectable Operating Modes: Constant Frequency, Burst Mode® Operation and PWM
- 5mm × 5mm QFN and 28-Lead Narrow SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers
- Telecom Systems
- Portable Instruments
- Battery-Operated Digital Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®3728L/LTC3728LX are dual high performance step-down switching regulator controllers that drive all N-channel synchronous power MOSFET stages. A constant frequency current mode architecture allows phase-lockable frequency of up to 550kHz. Power loss and noise due to the ESR of the input capacitors are minimized by operating the two controller output stages out of phase.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The precision 0.8V reference and power good output indicator are compatible with future microprocessor generations, and a wide 4.5V to 28V (30V maximum) input supply range encompasses all battery chemistries.

A RUN/SS pin for each controller provides both soft-start and optional timed, short-circuit shutdown. Current foldback limits MOSFET dissipation during short-circuit conditions when overcurrent latchoff is disabled. Output overvoltage protection circuitry latches on the bottom MOSFET until V_{OUT} returns to normal. The FCB mode pin can select among Burst Mode, constant frequency mode and continuous inductor current mode or regulate a secondary winding. The LTC3728L/LTC3728LX include a power good output pin that indicates when both outputs are within 7.5% of their designed set point.

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Burst Mode and OPTI-LOOP are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

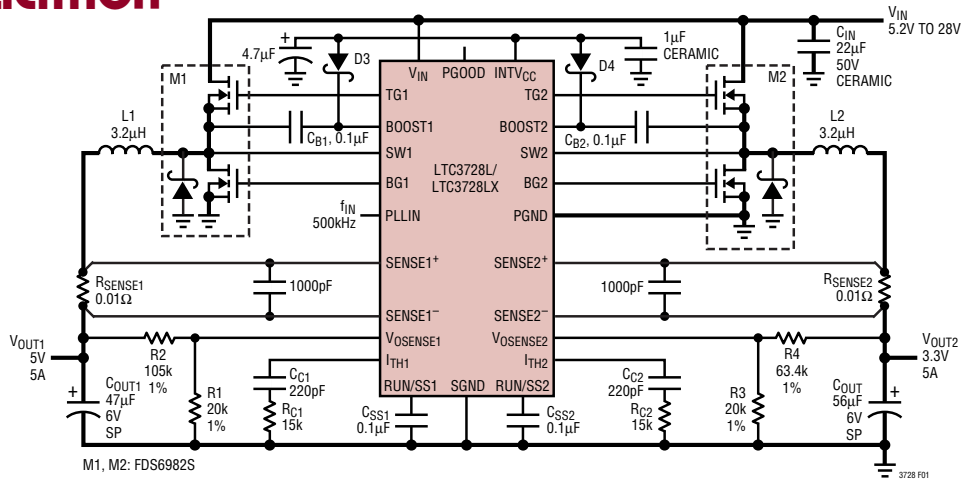


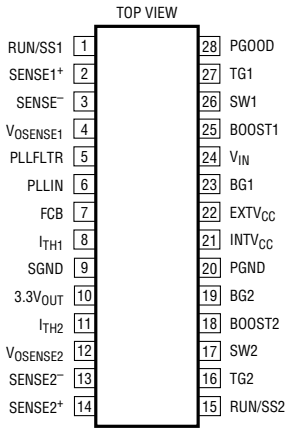
Figure 1. High Efficiency Dual 5V/3.3V Step-Down Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 30V to –0.3V
Top Side Driver Voltages
(BOOST1, BOOST2) ..... 36V to –0.3V
Switch Voltage (SW1, SW2) ..... 30V to –5V
$INTV_{CC}$, $EXTV_{CC}$, RUN/SS1, RUN/SS2, (BOOST1-SW1),
(BOOST2-SW2), PGOOD ..... 7V to –0.3V
$SENSE1^+$, $SENSE2^+$, $SENSE1^–$,
$SENSE2^–$ Voltages ..... (1.1)$INTV_{CC}$ to –0.3V
PLLIN, PLLFLTR, FCB, Voltage ..... $INTV_{CC}$ to –0.3V

I_{TH1}, I_{TH2}, $V_{OSENSE1}$, $V_{OSENSE2}$ Voltages ... 2.7V to –0.3V
Peak Output Current <10µs (TG1, TG2, BG1, BG2) .. 3A
$INTV_{CC}$ Peak Output Current 40mA
Operating Temperature Range (Note 7)
LTC3728LC/LTC3728LXC ..... 0°C to 85°C
LTC3728LE ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Reflow Peak Body Temperature (UH Package) .... 260°C
Lead Temperature (Soldering, 10 sec)
(GN Package) ..... 300°C

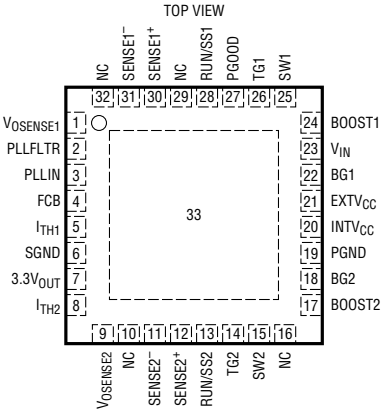
PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC3728LCGN
LTC3728LEGN



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD IS SGND (PIN 33),
MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC3728LCUH
LTC3728LEUH
LTC3728LXCUH

UH PART MARKING

3728L
3728LE
3728LX

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS1, 2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
$V_{OSENSE1, 2}$	Regulated Feedback Voltage	(Note 3); $I_{TH1, 2}$ Voltage = 1.2V (LTC3728LC) (Note 3); $I_{TH1, 2}$ Voltage = 1.2V (LTC3728LE/LTC3728LX)	● ●	0.792 0.788	0.800 0.800	0.808 0.812	V V
$I_{VOSENSE1, 2}$	Feedback Current	(Note 3)			–5	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 30V (Note 3)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2.0V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$g_{m1, 2}$	Transconductance Amplifier g_m	$I_{TH1, 2}$ = 1.2V; Sink/Source 5uA; (Note 3)			1.3		mmho

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$g_{mGBW1,2}$	Transconductance Amplifier GBW	$I_{TH1,2}$ = 1.2V; (Note 3)			3		MHz
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) V_{IN} = 15V; $EXTV_{CC}$ Tied to V_{OUT1}; V_{OUT1} = 5V $V_{RUN/SS1,2}$ = 0V			 450 20	 35	 µA µA
V_{FCB}	Forced Continuous Threshold		●	0.76	0.800	0.84	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.85V		–0.50	–0.18	–0.1	µA
$V_{BINHIBIT}$	Burst Inhibit (Constant Frequency) Threshold	Measured at FCB pin			4.3	4.8	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down	●		3.5	4	V
V_{OVL}	Feedback Overvoltage Lockout	Measured at $V_{OSENSE1,2}$	●	0.84	0.86	0.88	V
I_{SENSE}	Sense Pins Total Source Current	(Each Channel); $V_{SENSE1-,2-}$ = $V_{SENSE1+,2+}$ = 0V		–90	–60		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.4		%
$I_{RUN/SS1,2}$	Soft-Start Charge Current	$V_{RUN/SS1,2}$ = 1.9V		0.5	1.2		µA
$V_{RUN/SS1,2}$ ON	RUN/SS Pin ON Threshold	$V_{RUN/SS1}$, $V_{RUN/SS2}$ Rising		1.0	1.5	2.0	V
$V_{RUN/SS1,2}$ LT	RUN/SS Pin Latchoff Arming Threshold	$V_{RUN/SS1}$, $V_{RUN/SS2}$ Rising from 3V			4.1	4.75	V
$I_{SCL1,2}$	RUN/SS Discharge Current	Soft Short Condition $V_{OSENSE1,2}$ = 0.5V; $V_{RUN/SS1,2}$ = 4.5V		0.5	2	4	µA
I_{SDLHO}	Shutdown Latch Disable Current	$V_{OSENSE1,2}$ = 0.5V			1.6	5	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{OSENSE1,2}$ = 0.7V,$V_{SENSE1-,2-}$ = 5V $V_{OSENSE1,2}$ = 0.7V,$V_{SENSE1-,2-}$ = 5V	 ●	65 62	75 75	85 88	mV mV
 TG1, 2 t_r TG1, 2 t_f	TG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 55 55	 100 100	 ns ns
 BG1, 2 t_r BG1, 2 t_f	BG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 45 45	 100 90	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			80		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			80		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 6)			100		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA, V_{EXTVCC} = 4V			0.2	2.0	%
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			100	200	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				0.2		V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		360	400	440	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		230	260	290	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ ≥ 2.4V		480	550	590	kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 f_{PLLIN} < f_{OSC} f_{PLLIN} > f_{OSC}			 –15 15		 µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS1, 2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V Linear Regulator							
$V_{3.3OUT}$	3.3V Regulator Output Voltage	No Load	●	3.2	3.35	3.45	V
$V_{3.3IL}$	3.3V Regulator Load Regulation	$I_{3.3}$ = 0 to 10mA			0.5	2	%
$V_{3.3VL}$	3.3V Regulator Line Regulation	6V < V_{IN} < 30V			0.05	0.2	%
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level, Either Controller	V_{OSENSE} with Respect to Set Output Voltage V_{OSENSE} Ramping Negative V_{OSENSE} Ramping Positive		 –6 6	 –7.5 7.5	 –9.5 9.5	 % %

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3728LUH/LTC3728LXUH: $T_J = T_A + (P_D \bullet 34°C/W)$

LTC3728LGN: $T_J = T_A + (P_D \bullet 95°C/W)$

Note 3: The IC is tested in a feedback loop that servos $V_{ITH1, 2}$ to a specified voltage and measures the resultant $V_{OSENSE1, 2}$.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

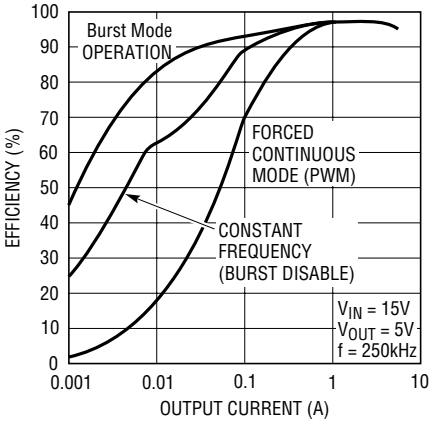
Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 6: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

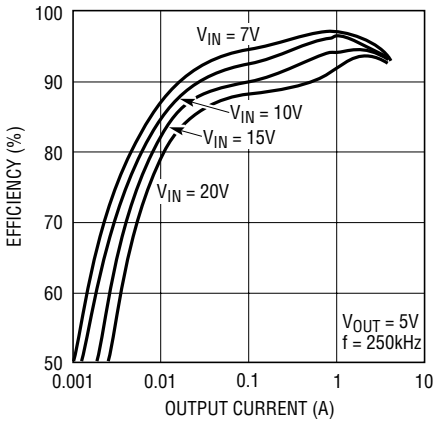
Note 7: The LTC3728LC/LTC3728LXC are guaranteed to meet performance specifications from 0°C to 85°C. The LTC3728LE is guaranteed to meet performance specifications over the –40°C to 85°C operating temperature range as assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

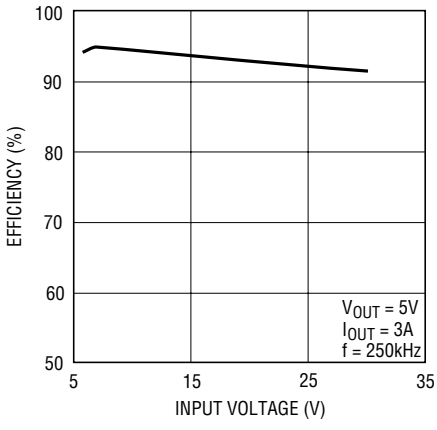
Efficiency vs Output Current and Mode (Figure 13)



Efficiency vs Output Current (Figure 13)

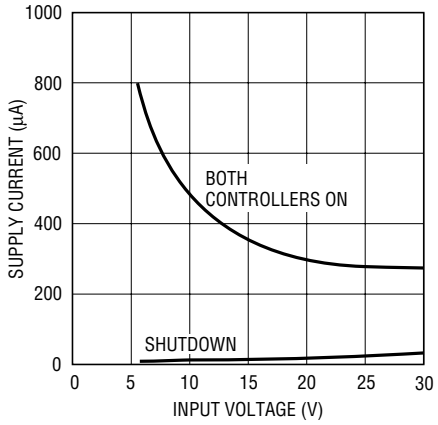


Efficiency vs Input Voltage (Figure 13)

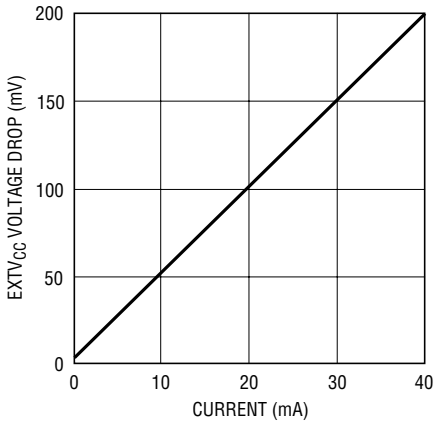


TYPICAL PERFORMANCE CHARACTERISTICS

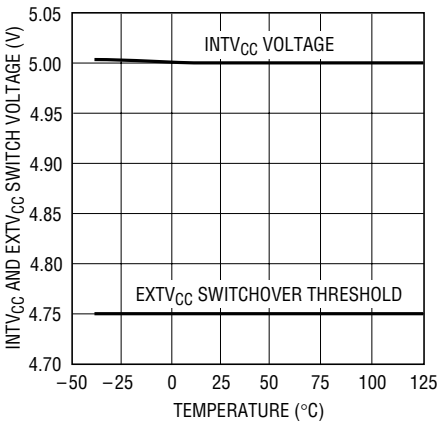
Supply Current vs Input Voltage and Mode (Figure 13)



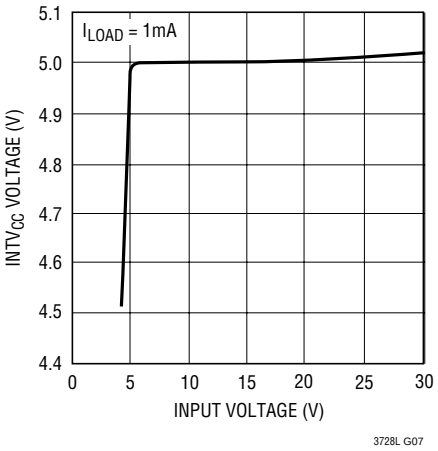
$EXTV_{CC}$ Voltage Drop



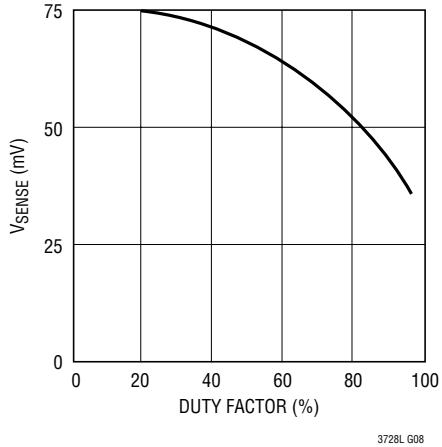
$INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature



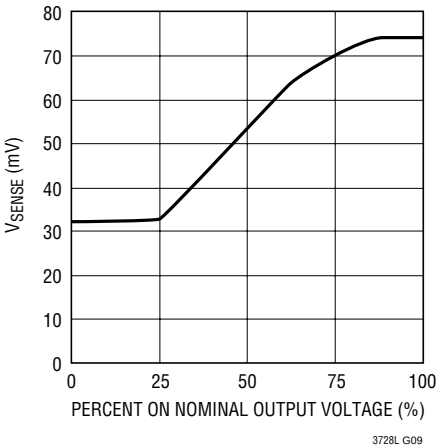
Internal 5V LDO Line Regulation



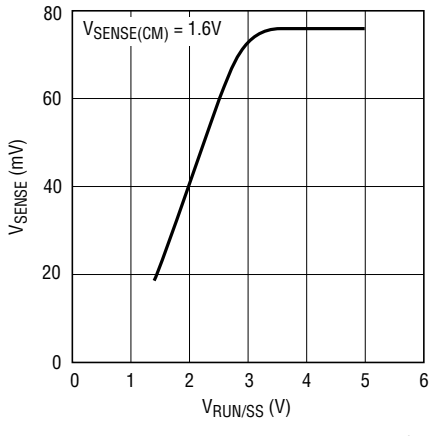
Maximum Current Sense Threshold vs Duty Factor



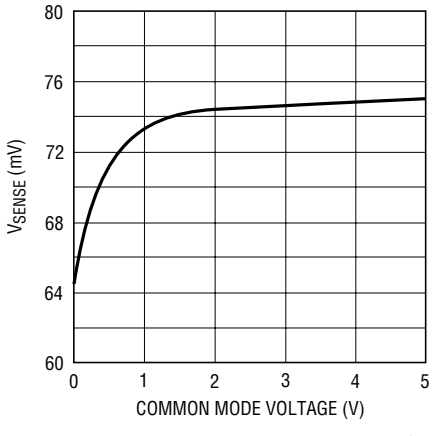
Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)



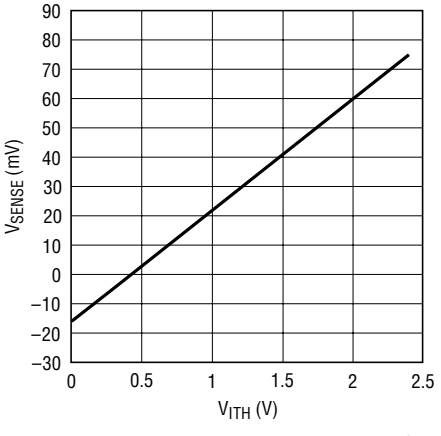
Maximum Current Sense Threshold vs $V_{RUN/SS}$ (Soft-Start)



Maximum Current Sense Threshold vs Sense Common Mode Voltage

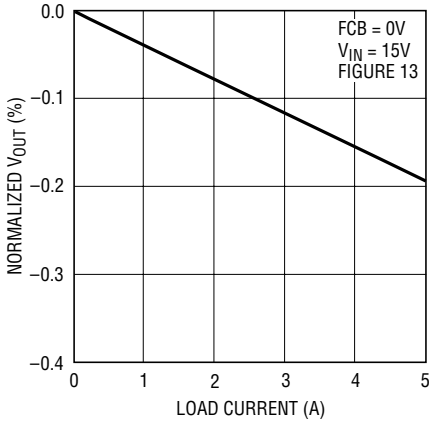


Current Sense Threshold vs I_{TH} Voltage

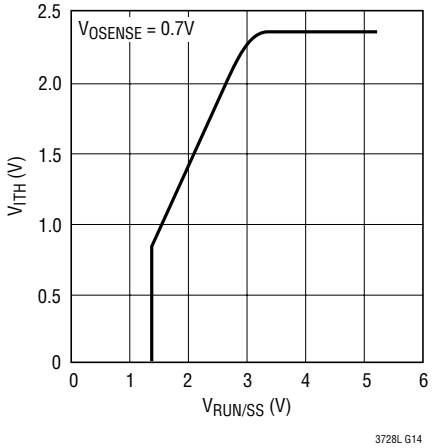


TYPICAL PERFORMANCE CHARACTERISTICS

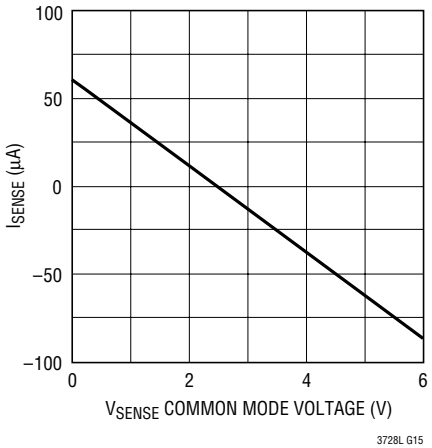
Load Regulation



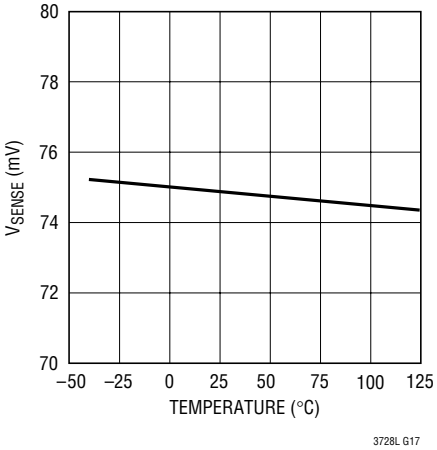
VITH vs VRUN/SS



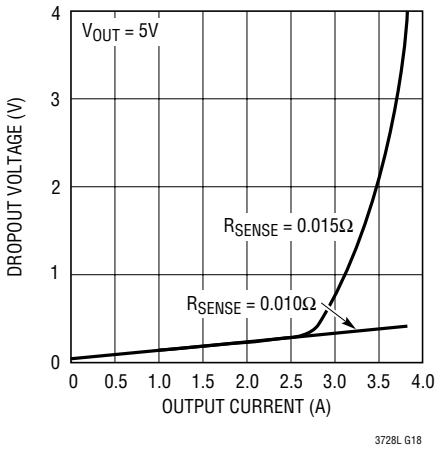
SENSE Pins Total Source Current



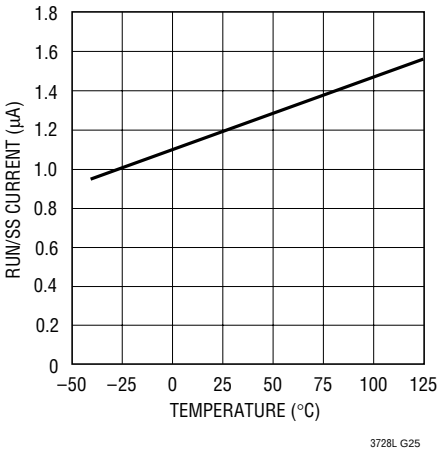
Maximum Current Sense Threshold vs Temperature



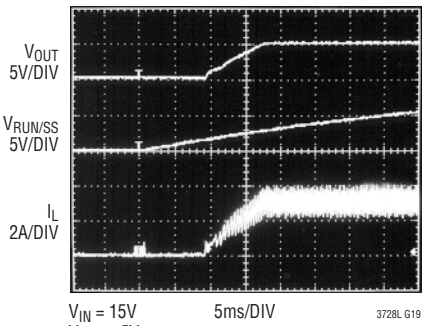
Dropout Voltage vs Output Current (Figure 14)



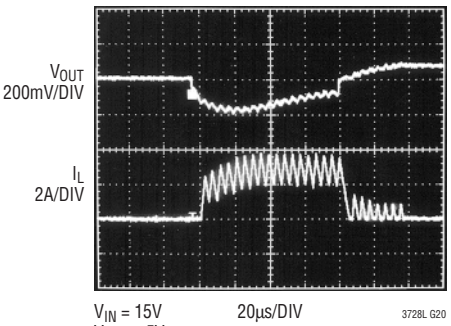
RUN/SS Current vs Temperature



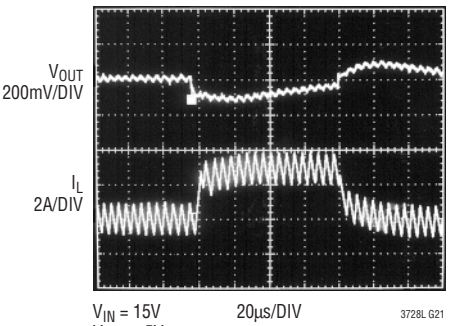
Soft-Start Up (Figure 13)



Load Step (Figure 13)

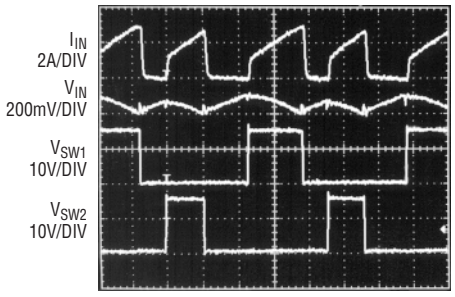


Load Step (Figure 13)



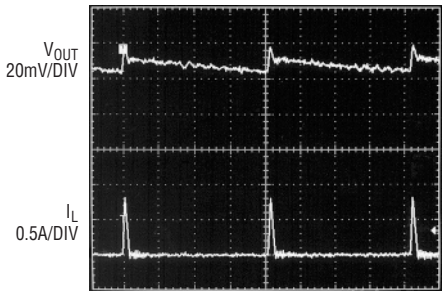
TYPICAL PERFORMANCE CHARACTERISTICS

Input Source/Capacitor Instantaneous Current (Figure 13)



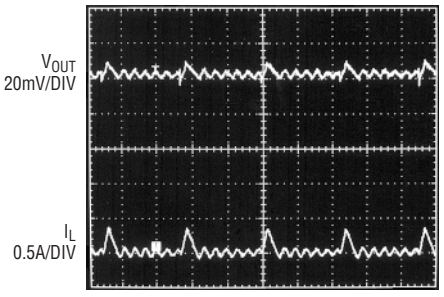
V_{IN} = 15V 1µs/DIV 3728L G22
V_{OUT1} = 5V, V_{OUT2} = 3.3V
$V_{PLLFLTR}$ = 0V
I_{OUT5} = $I_{OUT3.3}$ = 2A

Burst Mode Operation (Figure 13)



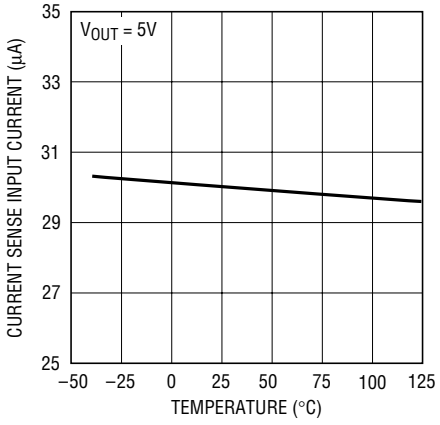
V_{IN} = 15V 10µs/DIV 3728L G23
V_{OUT} = 5V
$V_{PLLFLTR}$ = 0V
V_{FCB} = OPEN
I_{OUT} = 20mA

Constant Frequency (Burst Inhibit) Operation (Figure 13)



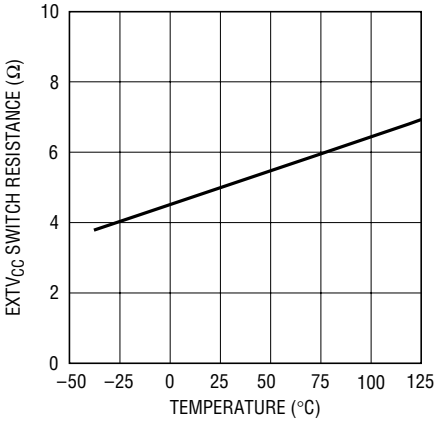
V_{IN} = 15V 2µs/DIV 3728L G24
V_{OUT} = 5V
$V_{PLLFLTR}$ = 0V
V_{FCB} = 5V
I_{OUT} = 20mA

Current Sense Pin Input Current vs Temperature



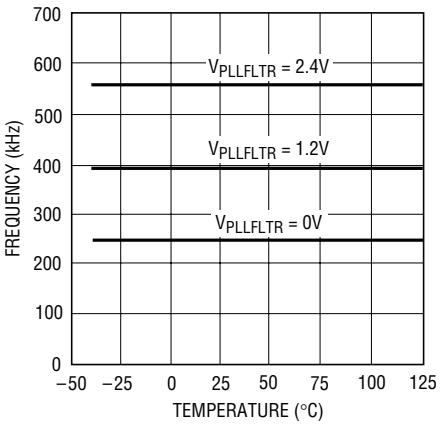
3728L G26

$EXTV_{CC}$ Switch Resistance vs Temperature



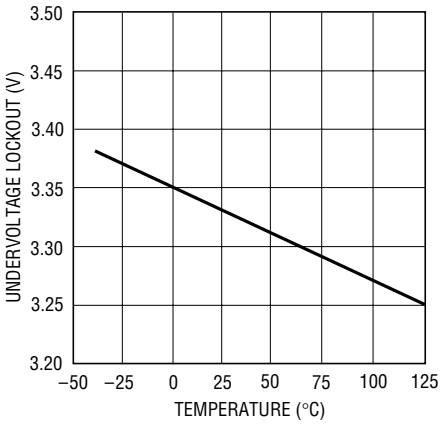
3728L G27

Oscillator Frequency vs Temperature



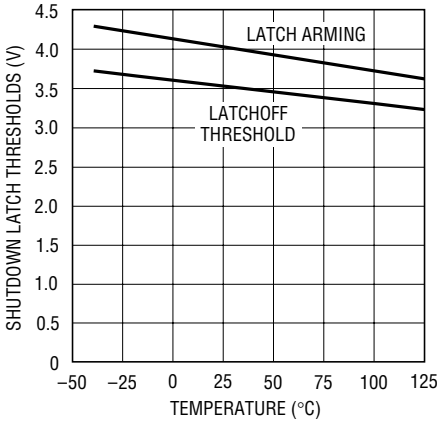
3728L G28

Undervoltage Lockout vs Temperature



3728L G29

Shutdown Latch Thresholds vs Temperature



3728L G30

PIN FUNCTIONS

$V_{OSENSE1}$, $V_{OSENSE2}$: Error Amplifier Feedback Input. Receives the remotely-sensed feedback voltage for each controller from an external resistive divider across the output.

PLLFLTR: Filter Connection for Phase-Locked Loop. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

PLLIN: External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

FCB: Forced Continuous Control Input. This input acts on both controllers and is normally used to regulate a secondary winding. Pulling this pin below 0.8V will force continuous synchronous operation.

I_{TH1}, I_{TH2}: Error Amplifier Output and Switching Regulator Compensation Point. Each associated channels' current comparator trip point increases with this control voltage.

SGND: Small Signal Ground. Common to both controllers, this pin must be routed separately from high current grounds to the common (–) terminals of the C_{OUT} capacitors.

$3.3V_{OUT}$: Lnear Regulator Output. Capable of supplying 10mA DC with peak currents as high as 50mA.

NC: No Connect.

$SENSE2^-$, $SENSE1^-$: The (–) Input to the Differential Current Comparators.

$SENSE2^+$, $SENSE1^+$: The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

RUN/SS2, RUN/SS1: Combination of soft-start, run control inputs and short-circuit detection timers. A capacitor to ground at each of these pins sets the ramp time to full output current. Forcing either of these pins back below 1.0V causes the IC to shut down the circuitry required for that particular controller. Latchoff overcurrent protection is also invoked via this pin as described in the Applications Information section.

TG2, TG1: High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

SW2, SW1: Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST2, BOOST1: Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the boost and switch pins and Schottky diodes are tied between the boost and $INTV_{CC}$ pins. Voltage swing at the boost pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

BG2, BG1: High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

PGND: Driver Power Ground. Connects to the sources of bottom (synchronous) N-channel MOSFETs, anodes of the Schottky rectifiers and the (–) terminal(s) of C_{IN}.

$INTV_{CC}$: Output of the Internal 5V Linear Low Dropout Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 4.7µF tantalum or other low ESR capacitor.

$EXTV_{CC}$: External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies V_{CC} power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ connection in Applications section. Do not exceed 7V on this pin.

V_{IN}: Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

PGOOD: Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on either V_{OSENSE} pin is not within ±7.5% of its set point.

Exposed Pad (UH Package Only): Signal Ground. Must be soldered to the PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.

FUNCTIONAL DIAGRAM

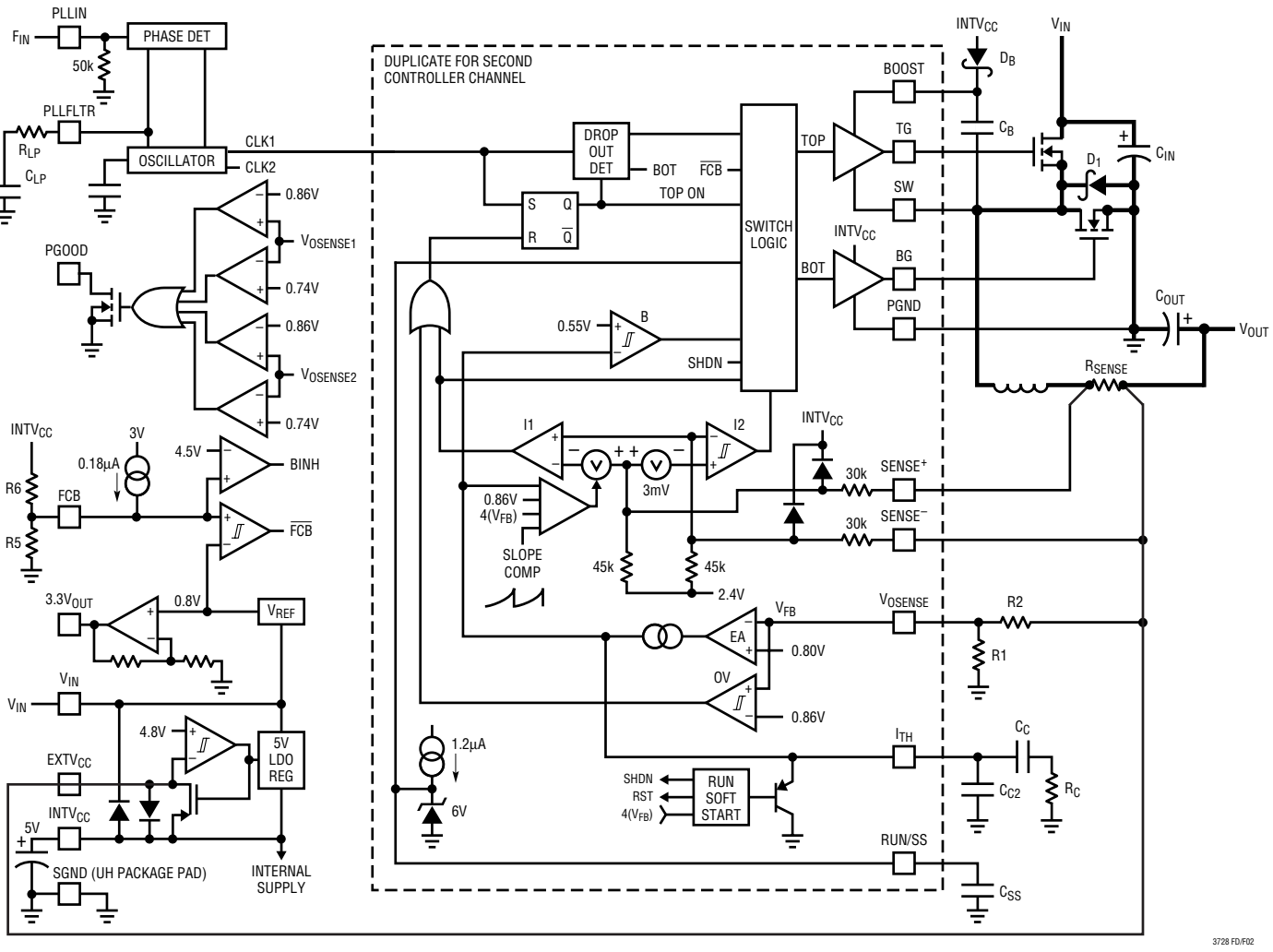


Figure 2

OPERATION (Refer to Functional Diagram)

Main Control Loop

The IC uses a constant frequency, current mode step-down architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The V_{OSENSE} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{OSENSE} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to

OPERATION (Refer to Functional Diagram)

increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 400ns every tenth cycle to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.2μA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, the I_{TH} pin voltage is gradually released allowing normal, full-current operation. When both RUN/SS1 and RUN/SS2 are low, all controller functions are shut down, including the 5V and 3.3V regulators.

Low Current Operation

The FCB pin is a multifunction pin providing two functions: 1) to provide regulation for a secondary winding by temporarily forcing continuous PWM operation on both controllers; and 2) to select between *two* modes of low current operation. When the FCB pin voltage is below 0.8V, the controller forces continuous PWM current mode operation. In this mode, the top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB pin is below V_{INTVCC} – 2V but greater than 0.8V, the controller enters Burst Mode operation. Burst Mode operation sets a minimum output current level before inhibiting the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low currents, force the I_{TH} pin below a voltage threshold that will temporarily inhibit turn-on of both output MOSFETs until the output voltage drops. There is 60mV of hysteresis in the burst comparator B tied to the I_{TH} pin. This hysteresis produces output signals to the MOSFETs that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block.

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 260kHz to 550kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

Constant Frequency Operation

When the FCB pin is tied to $INTV_{CC}$, Burst Mode operation is disabled and the forced minimum output current requirement is removed. This provides constant frequency, discontinuous current (preventing reverse inductor current) operation over the widest possible output current range. This constant frequency operation is not as efficient as Burst Mode operation, but does provide a lower noise, constant frequency operating mode down to approximately 1% of the designed maximum output current.

Continuous Current (PWM) Operation

Tying the FCB pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply to dangerous voltage levels—BEWARE!

OPERATION (Refer to Functional Diagram)

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout linear regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good (PGOOD) Pin

The PGOOD pin is connected to an open drain of an internal MOSFET. The MOSFET turns on and pulls the pin low when either output is not within ±7.5% of the nominal output level as determined by the resistive feedback divider. When both outputs meet the ±7.5% requirement, the MOSFET is turned off within 10µs and the pin is allowed to be pulled up by an external resistor to a source of up to 7V.

Foldback Current, Short-Circuit Detection and Short-Circuit Latchoff

The RUN/SS capacitors are used initially to limit the inrush current of each switching regulator. After the controller has been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used in a short-circuit time-out circuit. If the output voltage falls to less than 70% of its nominal output voltage, the RUN/SS capacitor begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin(s) voltage(s) are recycled. This built-in latchoff can be overridden by providing a >5µA pull-up at a compliance of 5V to the RUN/SS pin(s). This current shortens the soft start period but also prevents net discharge of the RUN/SS capacitor(s) during an overcurrent and/or short-circuit condition. Foldback current limiting is also activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled. Even if a short is present and the short-circuit latchoff is not enabled, a safe, low output current is provided due to internal current foldback and actual power wasted is low due to the efficient nature of the current mode switching regulator.

THEORY AND BENEFITS OF 2-PHASE OPERATION

The LTC1628 and the LTC3728L family of dual high efficiency DC/DC controllers brings the considerable benefits of 2-phase operation to portable applications for the first time. Notebook computers, PDAs, handheld terminals and automotive electronics will all benefit from the lower input filtering requirement, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

Why the need for 2-phase operation? Up until the 2-phase family, constant-frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two channels of the dual-switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. *The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.*

OPERATION (Refer to Functional Diagram)

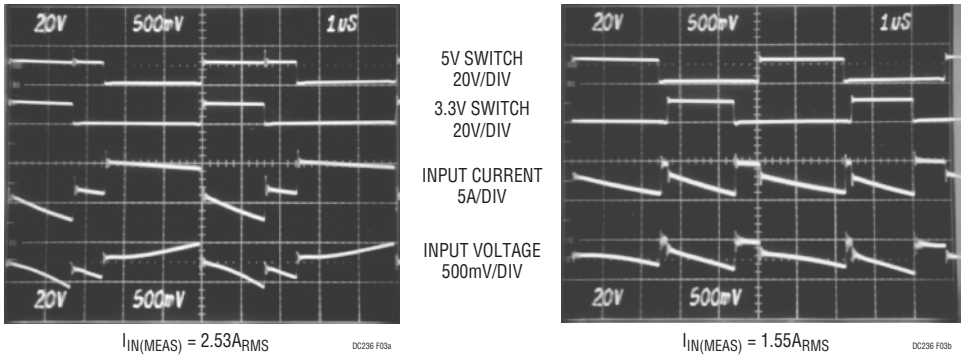


Figure 3. Input Waveforms Comparing Single-Phase (a) and 2-Phase (b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each. The Reduced Input Ripple with the LTC1628 2-Phase Regulator Allows Less Expensive Input Capacitors, Reduces Shielding Requirements for EMI and Improves Efficiency

Figure 3 compares the input waveforms for a representative single-phase dual switching regulator to the LTC1628 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase operation dropped the input current from $2.53A_{RMS}$ to $1.55A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS}^2, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple voltage also means less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}). Figure 4 shows how the RMS input current varies for single-phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

A final question: If 2-phase operation offers such an advantage over single-phase operation for dual switching regulators, why hasn't it been done before? The answer is that, while simple in concept, it is hard to implement. Constant-frequency current mode switching regulators require an oscillator derived "slope compensation" signal to allow stable operation of each regulator at over 50% duty cycle. This signal is relatively easy to derive in single-phase dual switching regulators, but required the development of a new and proprietary technique to allow 2-phase operation. In addition, isolation between the two channels becomes more critical with 2-phase operation because switch transitions in one channel could potentially disrupt the operation of the other channel.

These 2-phase parts are proof that these hurdles have been surmounted. They offer unique advantages for the ever-expanding number of high efficiency power supplies required in portable electronics.

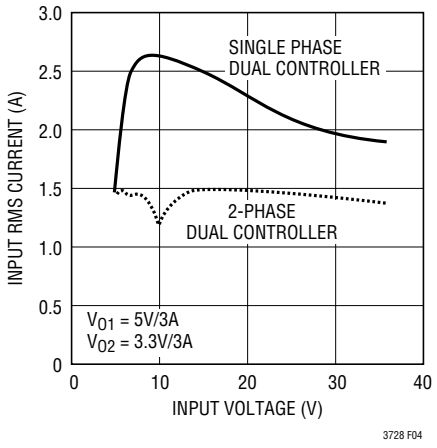


Figure 4. RMS Input Current Comparison

APPLICATIONS INFORMATION

Figure 1 on the first page is a basic LTC3728L/LTC3728LX application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND to 1.1(INTV$_{CC}$). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = \frac{50mV}{I_{MAX}}$$

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency

The IC uses a constant frequency phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization in the Applications Information section for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 5. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 550kHz.

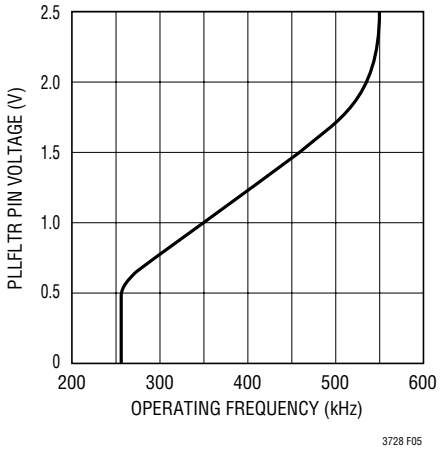


Figure 5. PLLFLTR Pin Voltage vs Frequency

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔI_L=0.3(I_{MAX}). The maximum ΔI_L occurs at the maximum input voltage.

APPLICATIONS INFORMATION

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available that do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for each controller in the LTC3728L/LTC3728LX: One N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the Gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)} + \left(V_{IN}\right)^2\left(\frac{I_{MAX}}{2}\right)\left(R_{DR}\right)\left(C_{MILLER}\right)\bullet \left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right]\left(f\right)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{MAX}\right)^2\left(1+\delta\right)R_{DS(ON)}$$

Kool Mμ is a registered trademark of Magnetics, Inc.

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where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 4Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1+δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the multiphase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst case RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS current requirement. Increasing the output current, drawn from the other out-of-phase controller, will actually decrease the input RMS ripple current from this maximum value (see Figure 4). The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

The type of input capacitor, value and ESR rating have efficiency effects that need to be considered in the selection process. The capacitance value chosen should be sufficient to store adequate charge to keep high peak battery currents down. 20µF to 40µF is usually sufficient for a 25W output supply operating at 200kHz. The ESR of the capacitor is important for capacitor power dissipation as well as overall battery efficiency. All of the power (RMS ripple current • ESR) not only heats up the capacitor but wastes power from the battery.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramic voltage coefficients are very high and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface-mount applicability; electrolytics' higher ESR and dryout possibility require several to be used. Multiphase systems allow the lowest amount of capacitance overall. As little as one 22µF or two to three 10µF ceramic capacitors are an ideal choice in a 20W to 35W power supply due to their extremely low ESR. Even though the capacitance at 20V is substantially below their rating at zero-bias, very low ESR loss makes ceramics an ideal candidate for highest efficiency battery operated systems. Also consider parallel ceramic and high quality electrolytic capacitors as an effective means of achieving ESR and bulk capacitance goals.

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx I_{MAX}\ \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's

APPLICATIONS INFORMATION

ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The benefit of the LTC3728L/LTC3728LX multiphase clocking can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the interleaving of current pulses through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Remember that input protection fuse resistance, battery resistance and PC board trace resistance losses are also reduced due to the reduced peak currents in a multiphase system. *The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.* The drains of the two top MOSFETS should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance, and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.3I_{OUT(MAX)}$ the output ripple will typically be less than 50mV at the maximum V_{IN} assuming:

C_{OUT} Recommended ESR < 2 R_{SENSE}

and $C_{OUT} > 1/(8fR_{SENSE})$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

Manufacturers such as Nichicon, United Chemi-Con and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications multiple capacitors may need to be used in parallel to meet ESR, RMS current handling and load step requirements. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have lower storage capacity per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors can be used in cost-driven applications providing that consideration is given to ripple current ratings, temperature and long term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, Panasonic SP,

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NEC Neocap, Cornell Dubilier ESRE and Sprague 595D series. Consult manufacturers for other specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the drivers and internal circuitry within the IC. The $INTV_{CC}$ pin regulator can supply a peak current of 50mA and must be bypassed to ground with a minimum of 4.7µF tantalum, 10µF special polymer, or low ESR type electrolytic capacitor. A 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND IC pins is highly recommended. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between channels.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the IC to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ and 3.3V linear regulators also needs to be taken into account for the power dissipation calculations. The total $INTV_{CC}$ current can be supplied by either the 5V internal linear regulator or by the $EXTV_{CC}$ input pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 4.7V, all of the $INTV_{CC}$ current is supplied by the internal 5V linear regulator. Power dissipation for the IC in this case is highest: $(V_{IN})(I_{INTVCC})$, and overall efficiency is lowered. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the IC V_{IN} current is thermally limited to less than 67mA from a 24V supply when not using the $EXTV_{CC}$ pin as follows:

$$T_J = 70°C + (67mA)(24V)(34°C/W) = 125°C$$

Use of the $EXTV_{CC}$ input pin reduces the junction temperature to:

$$T_J = 70°C + (67mA)(5V)(34°C/W) = 81°C$$

The absolute maximum rating for the $INTV_{CC}$ Pin is 40mA. Dissipation should be calculated to also include any added current drawn from the internal 3.3V linear regulator. To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The IC contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off and the switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal power. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation ($4.7V < V_{OUT} < 7V$) and from the internal regulator when the output is out of regulation (start-up, short-circuit). If more current is required through the $EXTV_{CC}$ switch than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this supply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open (or Grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.

2. $EXTV_{CC}$ Connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ Connected to an External supply. If an external supply is available in the 5V to 7V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.

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4. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V. This can be done with either the inductive boost winding as shown in Figure 6a or the capacitive charge pump shown in Figure 6b. The charge pump has the advantage of simple magnetics.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the functional diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Output Voltage

The output voltages are each set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.800V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right)$$

where R1 and R2 are defined in Figure 2.

SENSE+/SENSE– Pins

The common mode input range of the current comparator sense pins is from 0V to (1.1)$INTV_{CC}$. Continuous linear operation is guaranteed throughout this range allowing output voltage setting from 0.8V to 7.7V, depending upon the voltage applied to $EXTV_{CC}$. A differential NPN input stage is biased with internal resistors from an internal 2.4V source as shown in the Functional Diagram. This requires that current either be sourced or sunk from the SENSE pins depending on the output voltage. If the output voltage is below 2.4V current will flow out of both SENSE pins to the main output. The output can be easily preloaded by the V_{OUT} resistive divider to compensate for the current comparator's negative input bias current. The maximum current flowing out of each pair of SENSE pins is:

$$I_{SENSE}^{+} + I_{SENSE}^{-} = (2.4V - V_{OUT})/24k$$

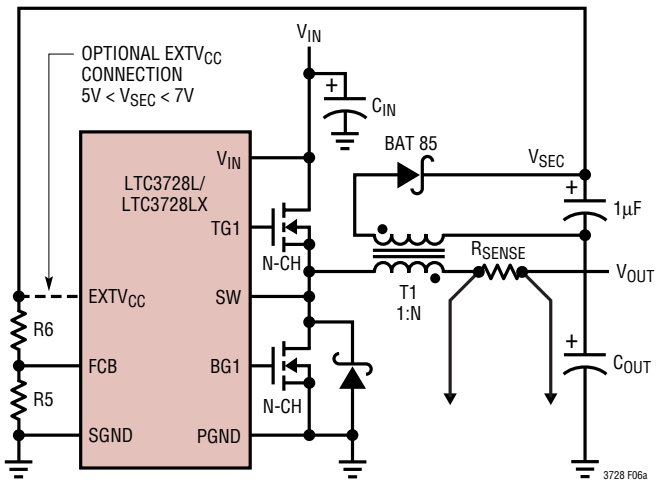


Figure 6a. Secondary Output Loop & $EXTV_{CC}$ Connection

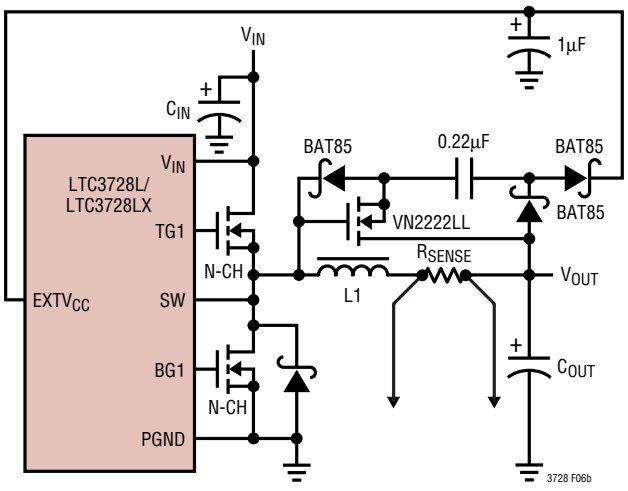


Figure 6b. Capacitive Charge Pump for $EXTV_{CC}$

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Since V_{OSENSE} is servoed to the 0.8V reference voltage, we can choose R1 in Figure 2 to have a maximum value to absorb this current.

$$R1_{(MAX)} = 24k\left(\frac{0.8V}{2.4V - V_{OUT}}\right)$$

for $V_{OUT} < 2.4V$

Regulating an output voltage of 1.8V, the maximum value of R1 should be 32k. Note that for an output voltage above 2.4V, R1 has no maximum value necessary to absorb the sense currents; however, R1 is still bounded by the V_{OSENSE} feedback current.

Soft-Start/Run Function

The RUN/SS1 and RUN/SS2 pins are multipurpose pins that provide a soft-start function and a means to shut down the LTC3728L/LTC3728LX. Soft-start reduces the input power source's surge currents by gradually increasing the controller's current limit (proportional to V_{ITH}). This pin can also be used for power supply sequencing.

An internal 1.2µA current source charges up the C_{SS} capacitor. When the voltage on RUN/SS1 (RUN/SS2) reaches 1.5V, the particular controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/R_{SENSE} to 75mV/R_{SENSE}. The output current limit ramps up slowly, taking an additional 1.25s/µF to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.25s/\mu F\right) C_{SS}$$

$$t_{IRAMP} = \frac{3V - 1.5V}{1.2\mu A} C_{SS} = \left(1.25s/\mu F\right) C_{SS}$$

By pulling both RUN/SS pins below 1V, the IC is put into low current shutdown (I_Q = 20µA). The RUN/SS pins can be driven directly from logic as shown in Figure 7. Diode D1 in Figure 7 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. Each RUN/SS pin has an internal 6V zener clamp (See Functional Diagram).

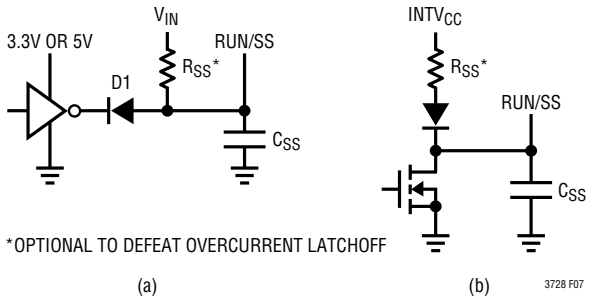


Figure 7. RUN/SS Pin Interfacing

Fault Conditions: Overcurrent Latchoff

The RUN/SS pins also provide the ability to latch off the controller(s) when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, is used initially to turn on and limit the inrush current. After the controller has been started and been given adequate time to charge up the output capacitor and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the regulator's output voltage falls to less than 70% of its nominal value after C_{SS} reaches 4.1V, C_{SS} begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of the C_{SS} and the specified discharge current, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} \approx [C_{SS}(4.1 - 1.5 + 4.1 - 3.5)]/(1.2\mu A)$$
$$= 2.7 \bullet 10^6 (C_{SS})$$

If the overload occurs after start-up the voltage on C_{SS} will begin discharging from the zener clamp voltage:

$$t_{LO2} \approx [C_{SS}(6 - 3.5)]/(1.2\mu A) = 2.1 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor to the RUN/SS pin as shown in Figure 7. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during an over current condition. Tying this pull-up resistor to V_{IN}, as in Figure 7a, defeats overcurrent latchoff.

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Diode-connecting this pull-up resistor to $INTV_{CC}$, as in Figure 7b, eliminates any extra supply current during controller shutdown while eliminating the $INTV_{CC}$ loading from preventing controller start-up.

Why should you defeat overcurrent latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will easily allow troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. After the design is complete, a decision can be made whether to enable the latchoff feature.

The value of the soft-start capacitor C_{SS} may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})\ (10^{-4})\ (R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

Fault Conditions: Current Limit and Current Foldback

The current comparators have a maximum sense voltage of 75mV resulting in a maximum MOSFET current of $75mV/R_{SENSE}$. The maximum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the highest power dissipation in the top MOSFET.

Each controller includes current foldback to help further limit load current when the output is shorted to ground. The foldback circuit is active even when the overload shutdown latch described above is overridden. If the output falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 75mV to 25mV. Under short-circuit conditions with very low duty cycles, the controller will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of each controller (typically 100ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\ (V_{IN}/L)$$

The resulting short-circuit current is:

$$I_{SC} = \frac{25mV}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 7.5% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The output of this comparator is only latched by the overvoltage condition itself and will therefore allow a switching regulator system having a poor PC layout to function while the design is being debugged. The bottom MOSFET remains on continuously for as long as the OV condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes. A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Phase-Locked Loop and Frequency Synchronization

The IC has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 400kHz. The nominal operating frequency range of the IC is 260kHz to 550kHz.

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The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$\Delta f_H = \Delta f_C = \pm 0.5\ f_O$ (260kHz-550kHz)

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 7.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The IC's PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. When using multiple ICs for a phase-locked system, the PLLFLTR pin of the master oscillator should be biased at a voltage that will guarantee the slave oscillator(s) ability to lock onto the master's frequency. A DC voltage of 0.7V to 1.7V applied to the master oscillator's PLLFLTR pin is recommended in order to meet this requirement. The resultant operating frequency can range from 300kHz to 500kHz.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10kΩ and C_{LP} is 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that each controller is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for each controller is approximately 100ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 150ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

FCB Pin Operation

The FCB pin can be used to regulate a secondary winding or as a logic level input. Continuous operation is forced on both controllers when the FCB pin drops below 0.8V. During continuous mode, current flows continuously in the transformer primary. The secondary winding(s) draw current only when the bottom, synchronous switch is on. When primary load currents are low and/or the V_{IN}/V_{OUT} ratio is low, the synchronous switch may not be on for a sufficient amount of time to transfer power from the output capacitor to the secondary load. Forced continuous operation will support secondary windings providing there is sufficient synchronous switch duty factor. Thus, the FCB input pin removes the requirement that power must be drawn from the inductor primary in order to extract

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power from the auxiliary windings. With the loop in continuous mode, the auxiliary outputs may nominally be loaded without regard to the primary output load.

The secondary output voltage V_{SEC} is normally set as shown in Figure 6a by the turns ratio N of the transformer:

$$V_{SEC} \cong (N + 1)\ V_{OUT}$$

However, if the controller goes into Burst Mode operation and halts switching due to a light primary load current, then V_{SEC} will droop. An external resistive divider from V_{SEC} to the FCB pin sets a minimum voltage $V_{SEC(MIN)}$:

$$V_{SEC(MIN)} \approx 0.8V\left(1+\frac{R6}{R5}\right)$$

where R5 and R6 are shown in Figure 2.

If V_{SEC} drops below this level, the FCB voltage forces temporary continuous switching operation until V_{SEC} is again above its minimum.

In order to prevent erratic operation if no external connections are made to the FCB pin, the FCB pin has a 0.18µA internal current source pulling the pin high. Include this current when choosing resistor values R5 and R6.

The following table summarizes the possible states available on the FCB pin:

Table 1

FCB Pin	Condition
0V to 0.75V	Forced Continuous Both Controllers (Current Reversal Allowed—Burst Inhibited)
0.85V < V_{FCB} < 4.3V	Minimum Peak Current Induces Burst Mode Operation No Current Reversal Allowed
Feedback Resistors	Regulating a Secondary Winding
>4.8V	Burst Mode Operation Disabled Constant Frequency Mode Enabled No Current Reversal Allowed No Minimum Peak Current

Voltage Positioning

Voltage positioning can be used to minimize peak-to-peak output voltage excursions under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Voltage positioning can easily be added to either or both controllers by loading the I_{TH} pin with a resistive divider having a Thevenin equivalent voltage source equal to the midpoint operating voltage range of the error amplifier, or 1.2V (see Figure 8).

The resistive load reduces the DC loop gain while maintaining the linear control range of the error amplifier. The maximum output voltage deviation can theoretically be reduced to half or alternatively the amount of output capacitance can be reduced for a particular application. A complete explanation is included in Design Solutions 10. (See www.linear-tech.com)

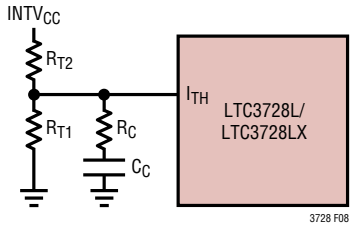


Figure 8. Active Voltage Positioning Applied to the LTC3728L/LTC3728LX

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3728L/LTC3728LX circuits: 1) IC V_{IN} current (including loading on the 3.3V internal regulator), 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table,

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which excludes MOSFET driver and control currents; the second is the current drawn from the 3.3V linear regulator output. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T+Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (V_{IN})^2 \bullet \left(\frac{I_{MAX}}{2}\right)(R_{DR}) \bullet (C_{MILLER})(f)\left(\frac{1}{5V - V_{TH}} + \frac{1}{V_{TH}}\right)$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC3728L 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point*

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truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main power line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery, and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 9 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC3728L/LTC3728LX have a maximum input voltage of 30V, most applications will also be limited to 30V by the MOSFET BVD_{SS}.

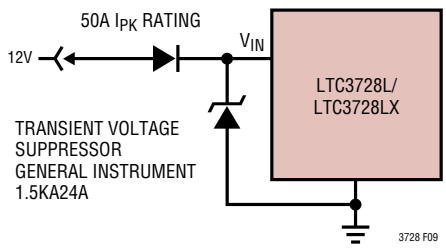


Figure 9. Automotive Application Protection

APPLICATIONS INFORMATION

Design Example

As a design example for one channel, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 1.8V, I_{MAX} = 5A, and f = 300kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the PLLFLTR pin to a resistive divider from the $INTV_{CC}$ pin, generating 0.7V for 300kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 23% ripple current and a 3.3µH will result in 33%. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.84A, for the 3.3µH value. Increasing the ripple current will also help ensure that the minimum on-time of 100ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(300kHz)} = 273ns$$

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{60mV}{5.84A} \approx 0.01\Omega$$

Since the output voltage is below 2.4V the output resistive divider will need to be sized to not only set the output voltage but also to absorb the SENSE pin's specified input current.

$$R1_{(MAX)} = 24k\left(\frac{0.8V}{2.4V - V_{OUT}}\right)$$
$$= 24k\left(\frac{0.8V}{2.4V - 1.8V}\right) = 32k$$

Choosing 1% resistors: R1 = 25.5k and R2 = 32.4k yields an output voltage of 1.816V.

The power dissipation on the top side MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{1.8V}{22V}(5)^2\left[1+(0.005)(50°C-25°C)\right]\bullet$$
$$(0.035\Omega)+(22V)^2\left(\frac{5A}{2}\right)(4\Omega)(215pF)\bullet$$
$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](300kHz) = 332mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{25mV}{0.01\Omega} - \frac{1}{2}\left(\frac{120ns(22V)}{3.3\mu H}\right) = 2.1A$$

with a typical value of $R_{DS(ON)}$ and δ= (0.005/°C)(20) = 0.1. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = \frac{22V-1.8V}{22V}(2.1A)^2(1.125)(0.022\Omega)$$
$$= 100mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.67A) = 33mV_{P-P}$$

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 10. The Figure 11 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

3. Do the LTC3728L/LTC3728LX V_{OSENSE} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of

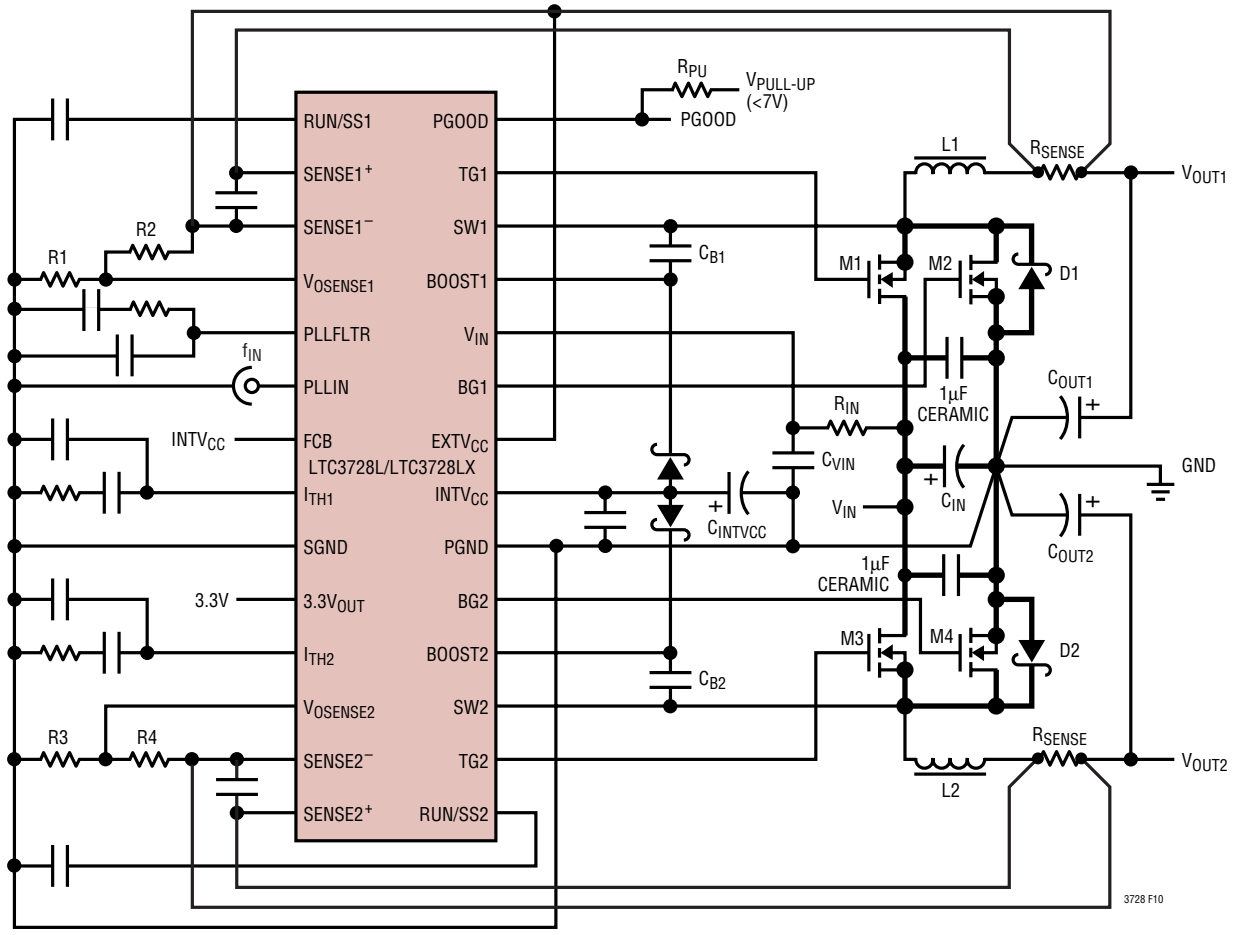


Figure 10. LTC3728L/LTC3728LX Recommended Printed Circuit Layout Diagram

APPLICATIONS INFORMATION

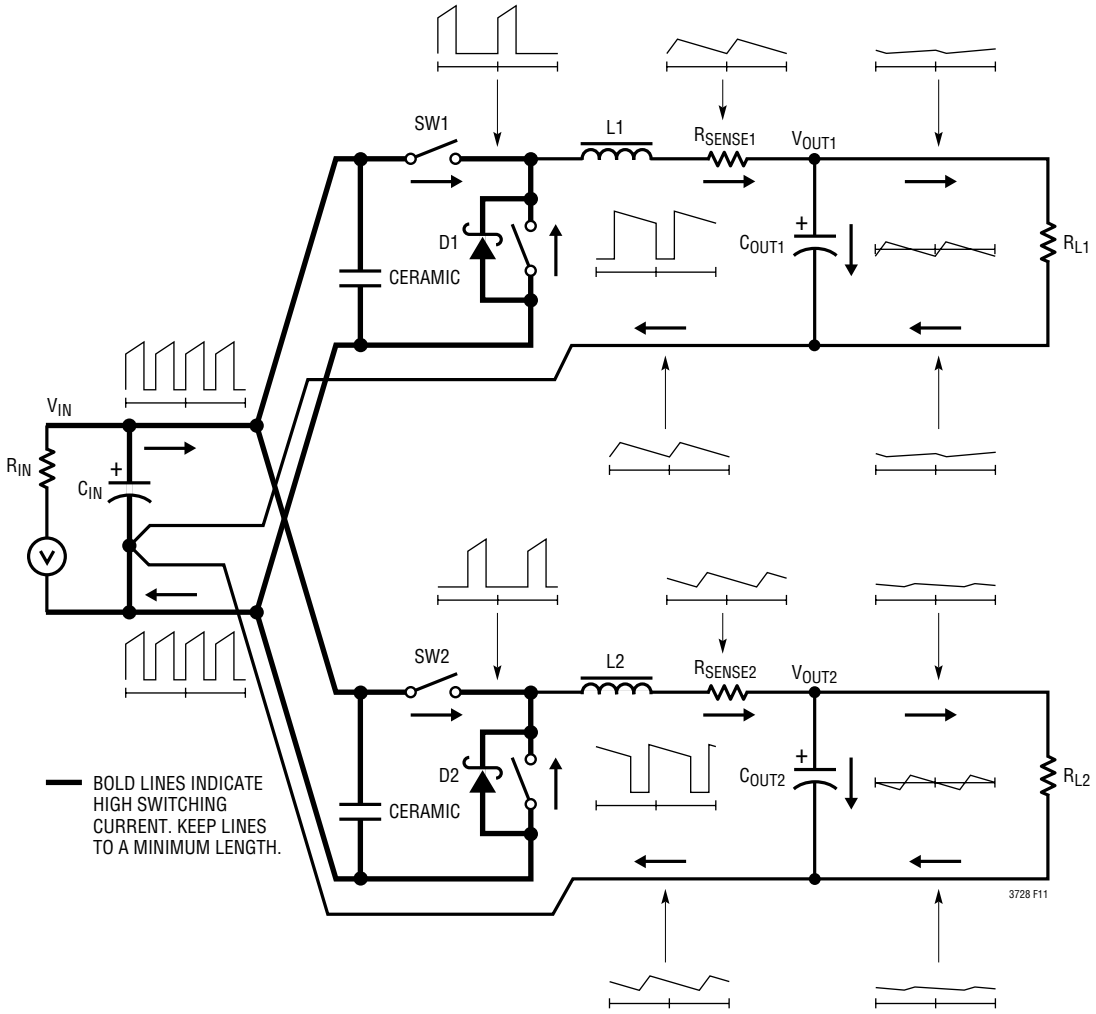


Figure 11. Branch Current Waveforms

C_{OUT} and signal ground. The R2 and R4 connections should not be along the high current input feeds from the input capacitor(s).

4. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.

6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3728L/LTC3728LX and occupy minimum PC trace area.

APPLICATIONS INFORMATION

7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% to 20% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

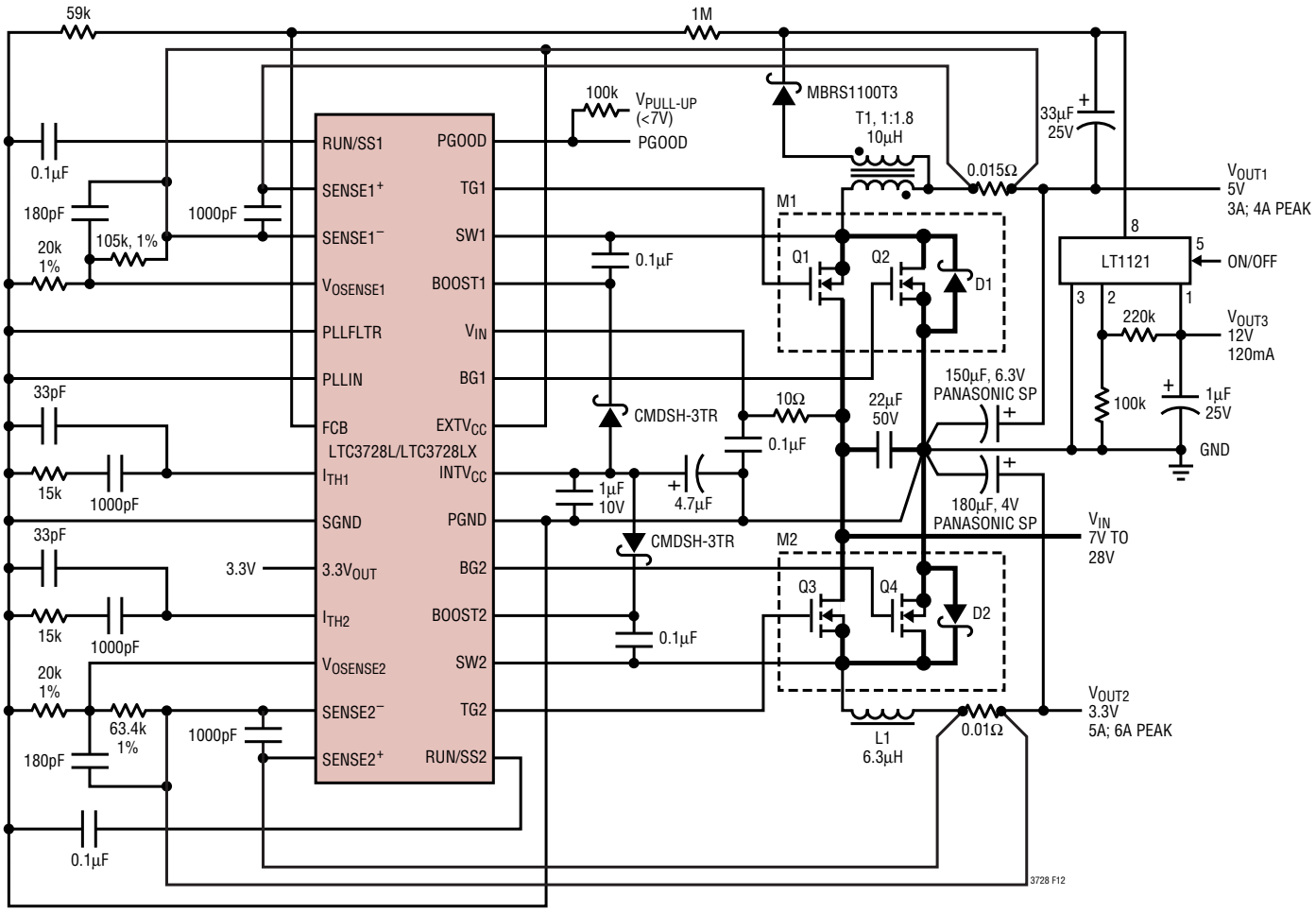
Short-circuit testing can be performed to verify proper overcurrent latchoff, or 5μA can be provided to the RUN/SS pin(s) by resistors from V_{IN} to prevent the short-circuit latchoff from occurring.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

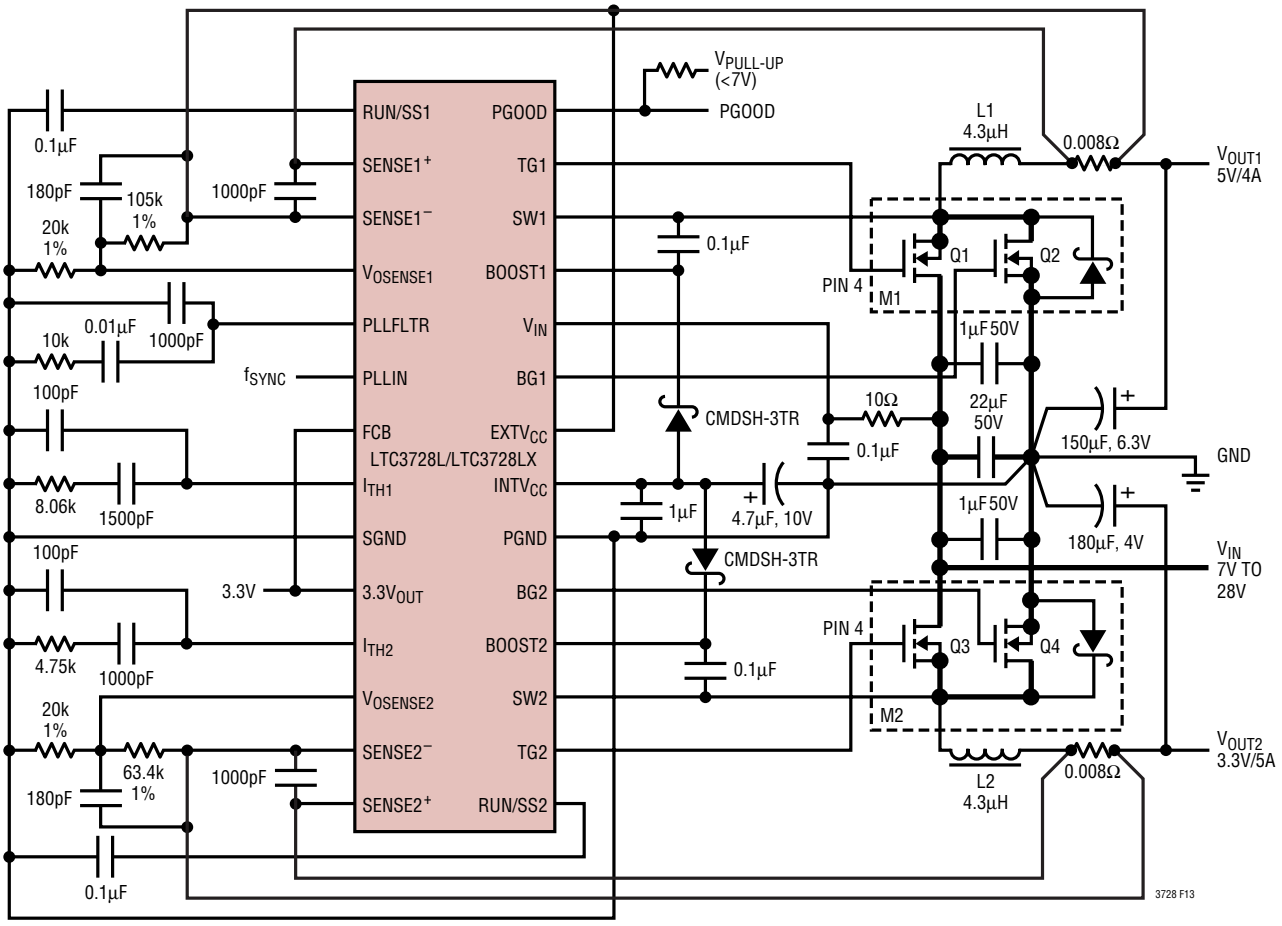
TYPICAL APPLICATIONS



V_{IN}: 7V TO 28V
V_{OUT}: 5V, 3A/3.3V, 6A/12V, 150mA
SWITCHING FREQUENCY = 250kHz
MI, M2: FDS6982S OR VISHAY Si4810DY
L1: SUMIDA CEP123-6R3MC
T1: 10µH 1:1.8 — DALE LPE6562-A262 GAPPED E-CORE OR BH ELECTRONICS #501-0657 GAPPED TOROID

Figure 12. LTC3728L/LTC3728LX High Efficiency Low Noise 5V/3A, 3.3V/5A, 12V/120mA Regulator

TYPICAL APPLICATIONS



V_{IN}: 7V TO 28V
V_{OUT}: 5V, 4A/3.3V, 5A

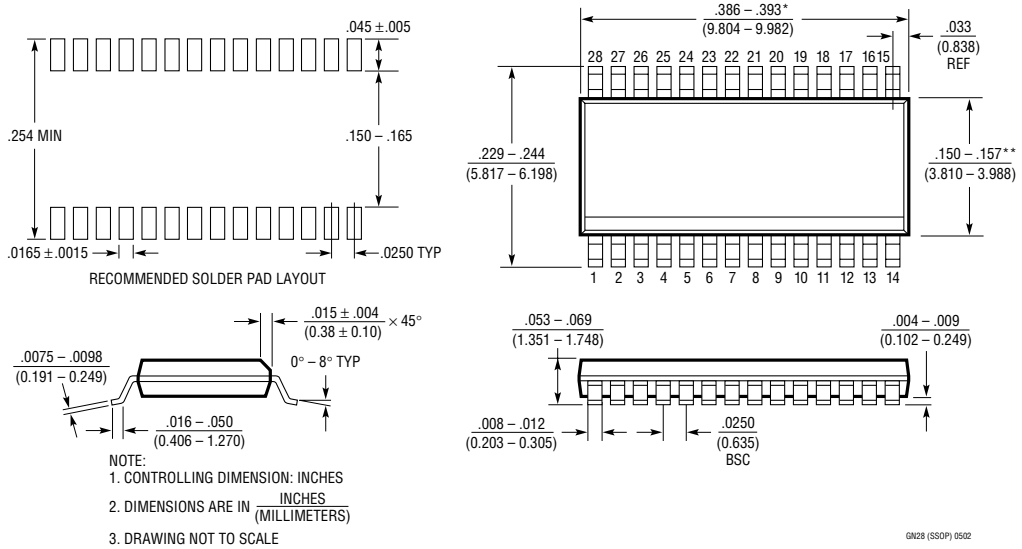
SWITCHING FREQUENCY = 250kHz TO 550kHz
M1, M2: FDS6982S OR VISHAY Si4810DY

L1, L2: SUMIDA CDEP105-4R3MC-88
OUTPUT CAPACITORS: PANASONIC SP SERIES

Figure 13. LTC3728L/LTC3728LX 5V/4A, 3.3V/5A Regulator with External Frequency Synchronization

PACKAGE DESCRIPTION (For purposes of clarity, drawings are not to scale)

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

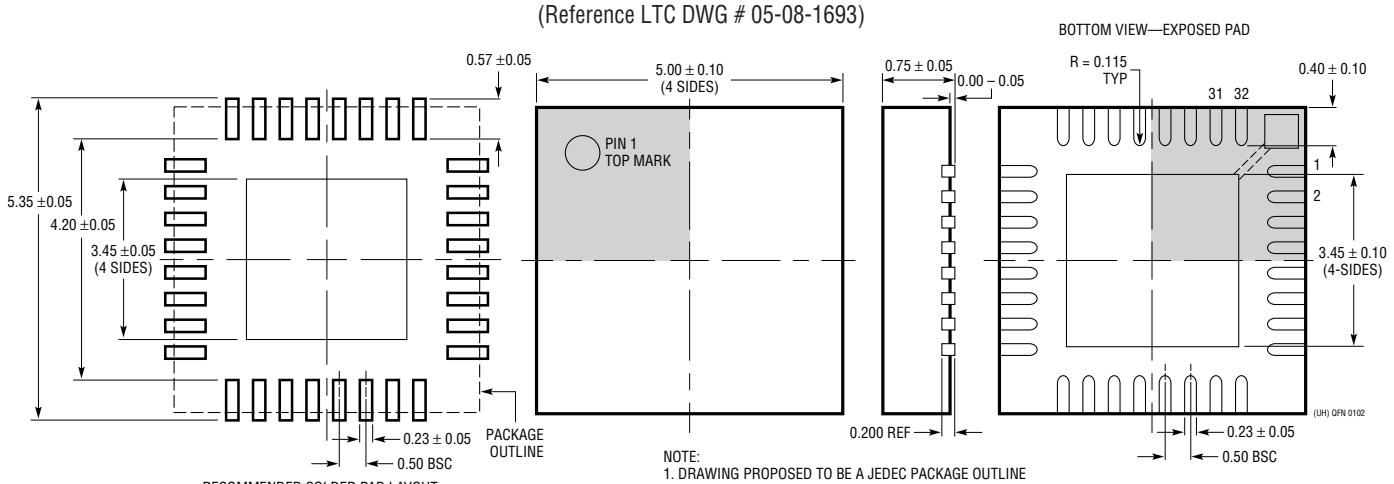


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

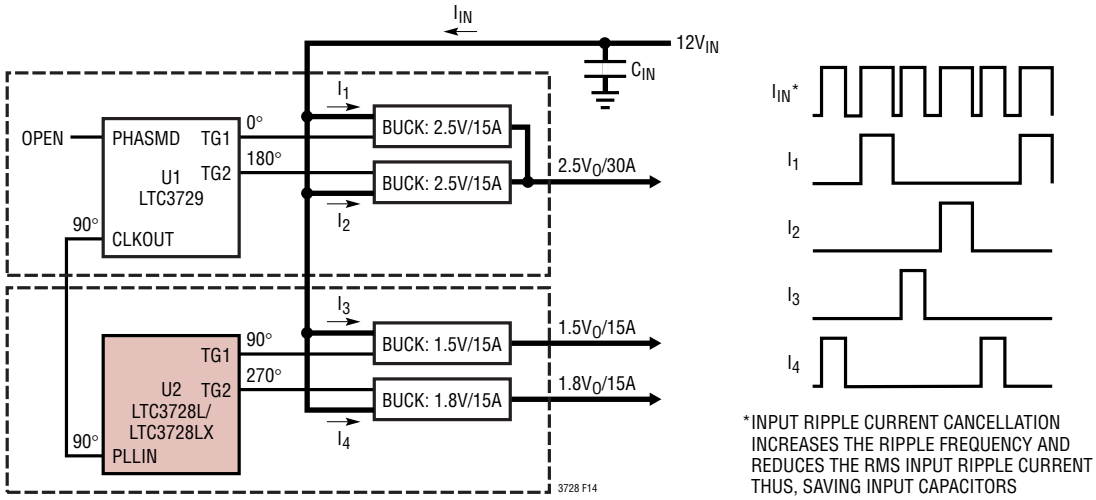


Figure 14. Multioutput PolyPhase Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC1628-PG/ LTC1628-SYNC	2-Phase, Dual Output Synchronous Step-Down DC/DC Controller	Reduces C_{IN} and C_{OUT}, Power Good Output Signal, Synchronizable, $3.5V \le V_{IN} \le 36V$, I_{OUT} up to 20A, $0.8V \le V_{OUT} \le 5V$
LTC1629/ LTC1629-PG	20A to 200A PolyPhase™ Synchronous Controllers	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, No Heat Sink, V_{IN} up to 36V
LTC1702A	No R_{SENSE} 2-Phase Dual Synchronous Step-Down Controller	550kHz, No Sense Resistor
LTC1708-PG	2-Phase, Dual Synchronous Controller with Mobile VID	$3.5V \le V_{IN} \le 36V$, VID Sets V_{OUT1}, PGOOD
LT1709/ LT1709-8	High Efficiency, 2-Phase Synchronous Step-Down Switching Regulators with 5-Bit VID	$1.3V \le V_{OUT} \le 3.5V$, Current Mode Ensures Accurate Current Sharing, $3.5V \le V_{IN} \le 36V$
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1736	High Efficiency Synchronous Controller with 5-Bit Mobile VID Control	Output Fault Protection, 24-Pin SSOP, $3.5V \le V_{IN} \le 36V$
LTC1778/LTC1778-1	No R_{SENSE} Current Mode Synchronous Step-Down Controllers	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} up to 20A
LTC1929/ LTC1929-PG	2-Phase Synchronous Controllers	Up to 42A, Uses All Surface Mount Components, No Heat Sinks, $3.5V \le V_{IN} \le 36V$
LTC3708	Dual, 2-Phase, DC/DC Controller with Output Tracking	Current Mode, No R_{SENSE}, Up/Down Tracking, Synchronizable
LTC3711	No R_{SENSE} Current Mode Synchronous Step-Down Controller with Digital 5-Bit Interface	Up to 97% Efficiency, Ideal for Pentium® III Processors, $0.925V \le V_{OUT} \le 2V$, $4V \le V_{IN} \le 36V$, I_{OUT} up to 20A
LTC3728	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 3.5V to 35V, 99% Duty Cycle, 5x5QFN, SSOP-28
LTC3729	20A to 200A, 550kHz PolyPhase Synchronous Controller	Expandable from 2-Phase to 12-Phase, Uses all Surface Mount Components, V_{IN} up to 36V
LTC3731	3- to 12-Phase Step-Down Synchronous Controller	60A to 240A Output Current, $0.6V \le V_{OUT} \le 6V$, $4.5V \le V_{IN} \le 32V$

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