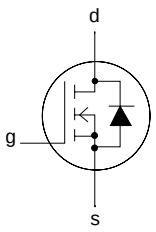
TrenchMOS™ transistor Logic level FET

PHN1011

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- High thermal cycling performance
- Low-profile surface mount package
- Logic level compatible

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 11 A

$R_{DS(ON)} \leq 11\ m\Omega$ (V_{GS} = 10 V)

$R_{DS(ON)} \leq 13.5\ m\Omega$ (V_{GS} = 5 V)

GENERAL DESCRIPTION

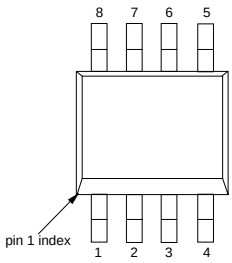
N-channel enhancement mode logic level field-effect power transistor in a surface mounting plastic package using '**trench**' technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHN1011 is supplied in the SOT96-1 (SO8) surface mounting package

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96-1 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	25	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage (DC)	-	-	± 15	V
V_{GSM}	Gate-source voltage (pulse peak value)		-	± 20	V
I_D	Drain current ($t_p \leq 10$ s)	T_a = 25 ˚C	-	11	A
		T_a = 70 ˚C	-	9	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 ˚C	-	44	A
P_{tot}	Total power dissipation	T_a = 25 ˚C	-	2.5	W
		T_a = 70 ˚C	-	1.6	W
T_j, T_{stg}	Operating junction and storage temperature	-	- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board, t ≤ 10 sec	-	50	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board	150	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	9	11	mΩ
		V_{GS} = 5 V; I_D = 5 A	-	11	13.5	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 150˚C	-	-	23	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	12	36	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 25 A; V_{DD} = 15 V; V_{GS} = 5 V	-	26	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	9.4	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	7	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	82	120	ns
t_f	Turn-off fall time		-	59	75	ns
L_d	Internal drain inductance	Drain leads to centre of die	-	1	-	nH
L_s	Internal source inductance	Source leads to source bond pad	-	3	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz	-	1700	-	pF
C_{oss}	Output capacitance		-	475	-	pF
C_{rss}	Feedback capacitance		-	300	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_a = 25 ˚C, t_p ≤ 10 s	-	-	11	A
I_{SM}	Pulsed source current (body diode)		-	-	44	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	83	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 25 V	-	0.1	-	µC

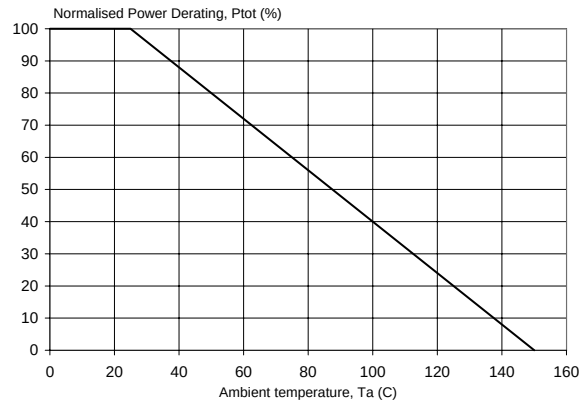


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_a)$

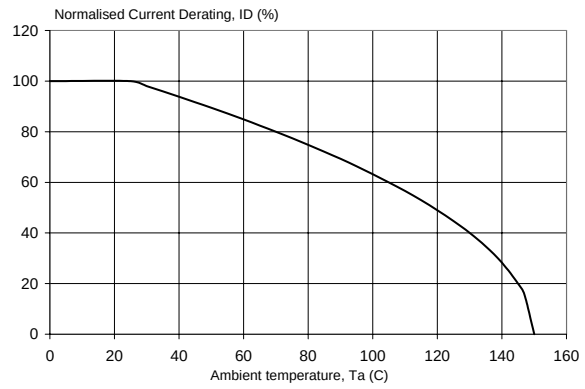


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_a)$; conditions: $V_{GS} \geq 5$ V

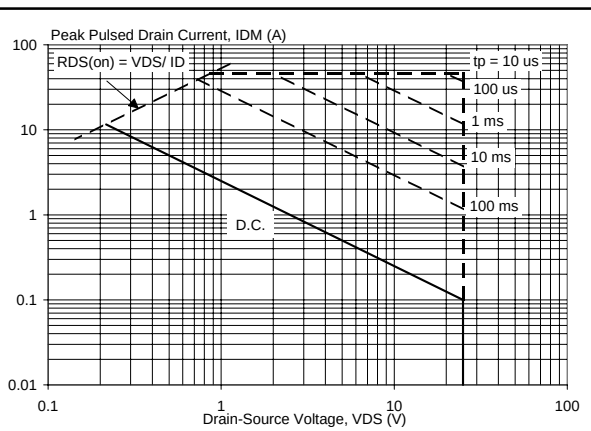


Fig.3. Safe operating area. $T_a = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

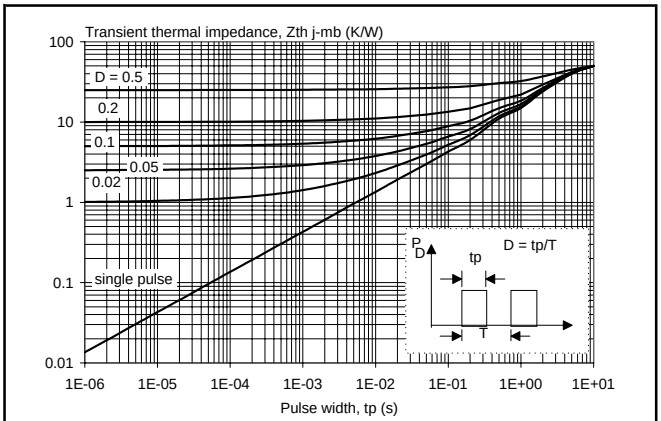


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a} = f(t)$; parameter $D = t_p/T$

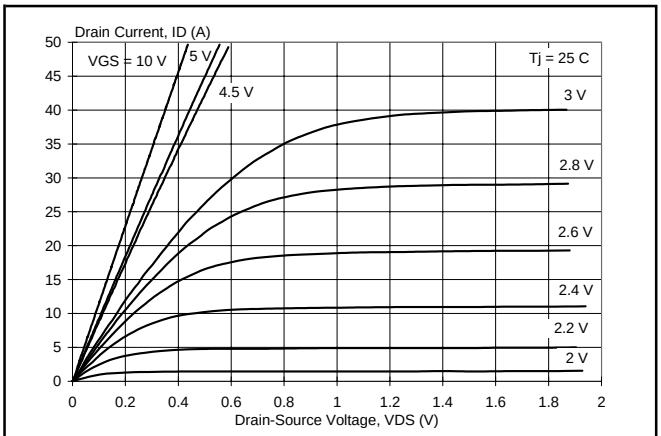


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{GS}

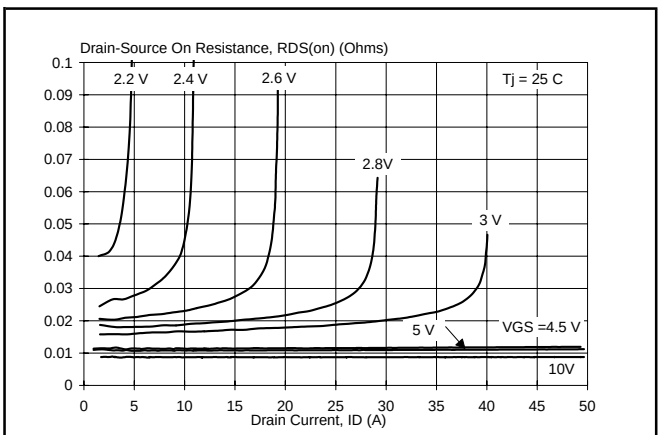


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

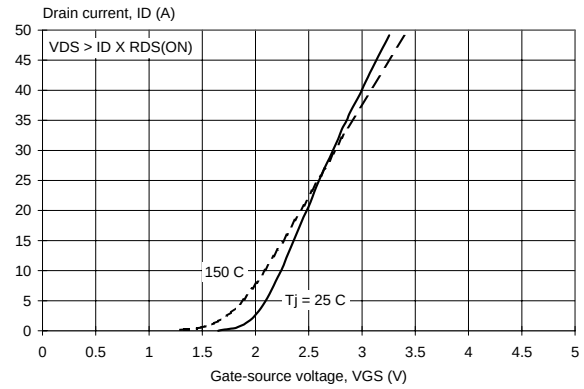


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

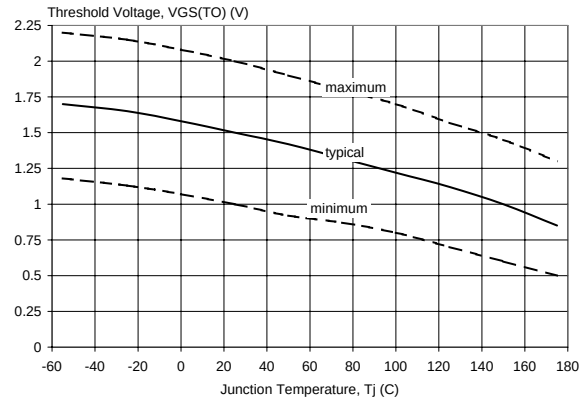


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

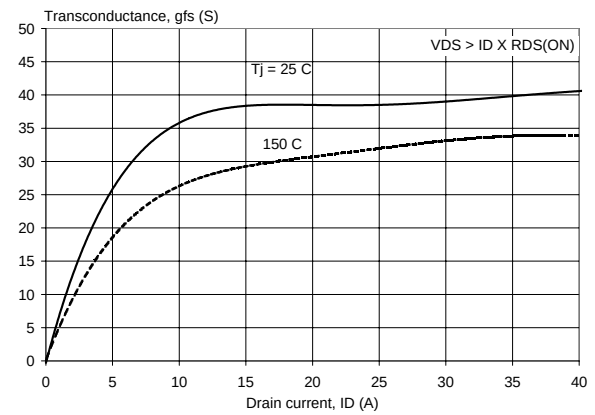


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

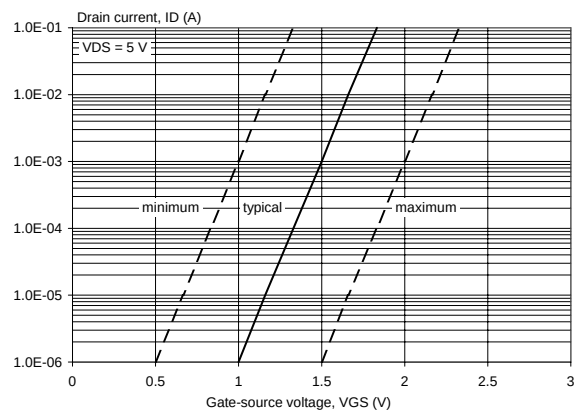


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

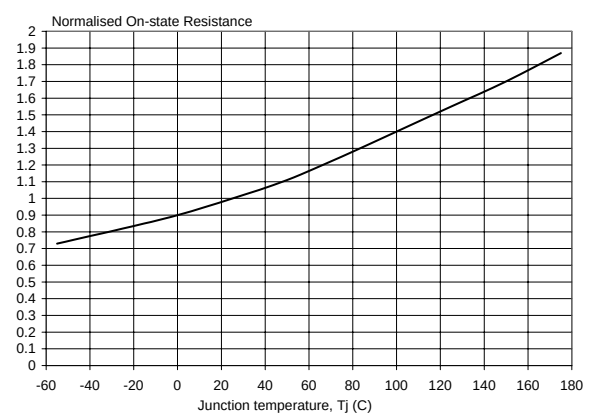


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$

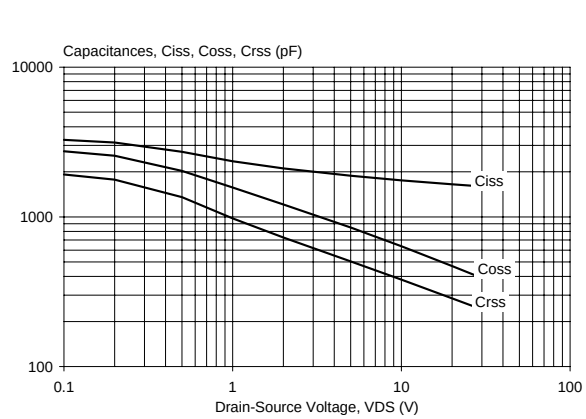


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

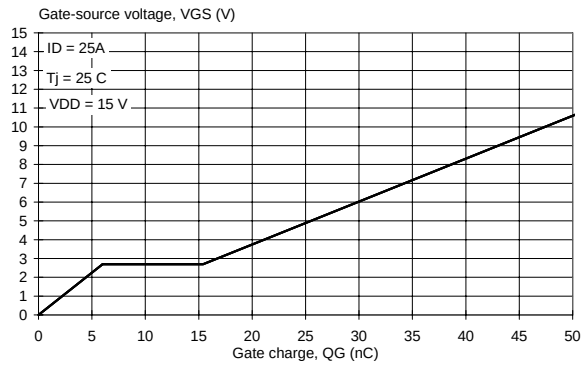


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

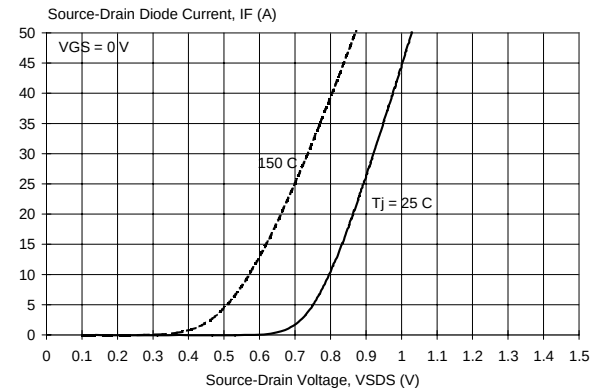
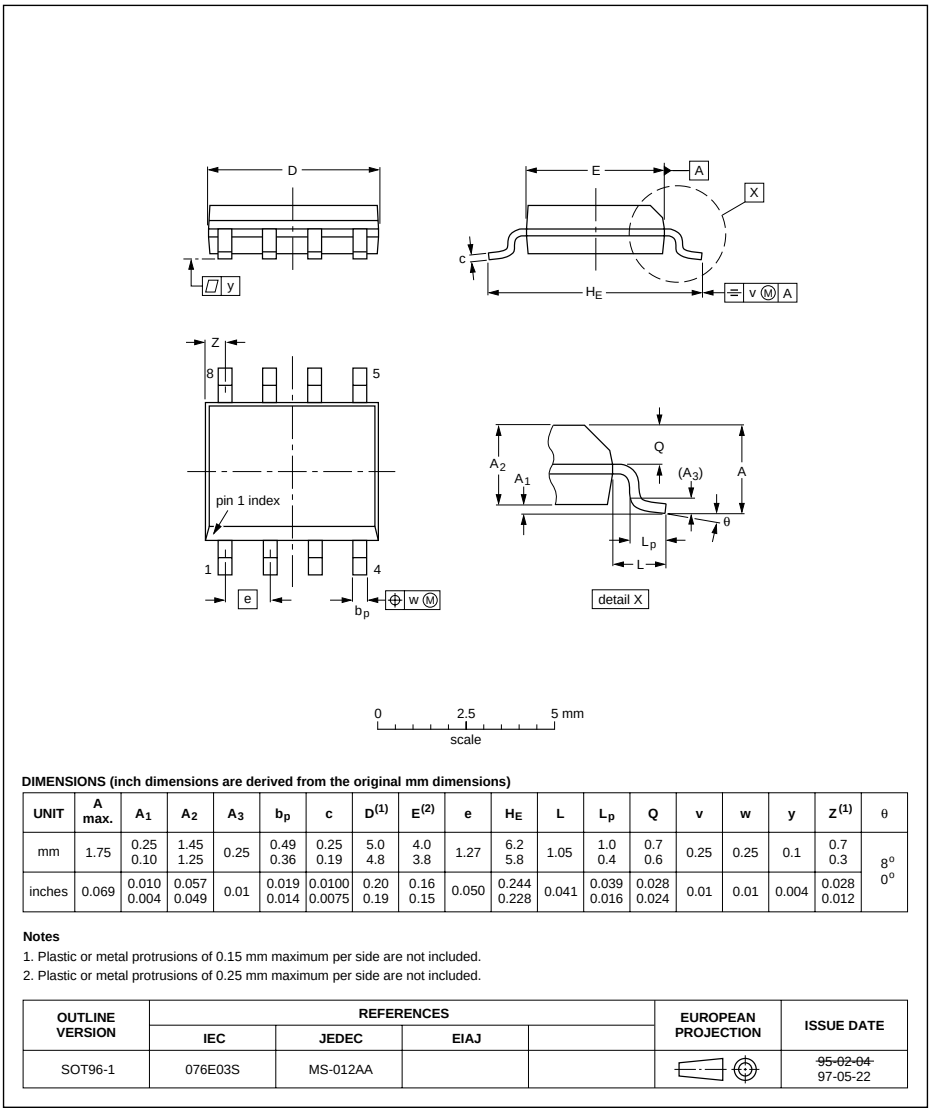


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig.15. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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