Obsolescence Notice

ZARLINK SEMICONDUCTOR

This product is obsolete.

This information is available for your convenience only.

For more information on Zarlink's obsolete products and replacement product lists, please visit

http://products.zarlink.com/obsolete_products/

GEC PLESSEY
SEMICONDUCTORS

JULY 1995

DS3798-3.1

MA838 FAMILY

SINGLE PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA838 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

Two TTL level PWM outputs control the upper and lower switches in an inverter arm. This is usually via an external isolation and amplification stage.

Information contained within the pulse width modulated sequences controls the wave shape, power frequency and amplitude of the output waveform. Parameters such as the carrier frequency, minimum pulse width and pulse delay time may be defined during initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in the inverter, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

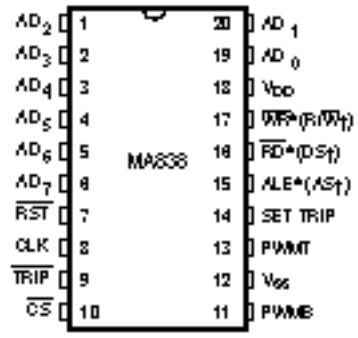
The MA838 is easily controlled by a microprocessor and its fully digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/ controllers.

FEATURES

- Fully Digital Operation
- Interfaces with most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Frequency Control accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered trademark of Motorola corp. and Intel corp.



NOTE
* = Intel bus format
† = Motorola bus format

DP28
MP28/W

Fig.1 Pin connections (top view)

The power frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC-injection braking with no software overhead.

This family is functionally identical to the MA828 PWM generator IC except that only one PWM channel is provided.

ORDERING INFORMATION

MA838-1 PLABA (Commercial, Plastic DIL)
MA838-2 PLABA (Commercial, Plastic DIL)
MA838-1 PLABD (Industrial, Plastic DIL)
MA838-2 PLABD (Industrial, Plastic DIL)
MA838-1 SLABA (Commercial, Plastic Small Outline)
MA838-2 SLABA (Commercial, Plastic Small Outline)
MA838-1 SLABD (Industrial, Plastic Small Outline)
MA838-2 SLABD (Industrial, Plastic Small Outline)

The MA838-1 and MA838-2 are the two standard waveform options offered; refer to **PRODUCT DESIGNATION** section for waveform specifications.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	V_{SS}-0.3V to V_{DD} +0.3V
Current through any I/O pin	±10mA
Storage temperature (see note)	-65°C to +125°C
Operating temperature range (commercial)	0°C to +70°C
Operating temperature range (industrial)	-40°C to +85°C

NOTE: These temperature ranges apply to all package types. Many package types are available and extended temperature ranges can be offered for some packages. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V±5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	V_{IH}	2.0	-	-	V	
Input low voltage	V_{IL}	-	-	0.8	V	
Input leakage current	I_{IN}	-	-	10	µA	$V_{IN} = V_{SS}$ or V_{DD}
Output high voltage	V_{OH}	4.0	>4.5	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	<0.2	0.4	V	I_{OH} = 4mA
Supply current (static) (dynamic)	$I_{DD\ (static)}$ $I_{DD\ (dynamic)}$	- -	- <10	100 20	µA mA	all outputs open circuit CLK = 10MHz
Supply voltage	V_{DD}	2.7	5.0	5.5	V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V±5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Clock frequency	f_{CLK}	-	-	12.5	MHz	M:S ratio 1:1 ±20%
SET TRIP = 0 → Outputs tripped → $\overline{TRIP}$ = 0	t_{TRIP}	 - -	 $2/f_{CLK}$ $2/f_{CLK}$	 $3/f_{CLK}$ $3/f_{CLK}$	 s s	

PRODUCT DESIGNATION

Two standard options exist, defining waveform shape. These are designated MA838-1 and MA838-2 as follows:

MA838-1

Sine + third harmonic at one sixth the amplitude of the fundamental:

$$x(t) = A\left[\sin(\omega t) + \frac{1}{6}\sin 3(\omega t)\right]$$

MA838-2

Pure sinewave:

$$x(t) = A\left[\sin(\omega t)\right]$$

Additional wave shapes can be implemented to order, provided they are symmetrical about the 90°, 180° and 270° axes. Contact your local GEC Plessey Semiconductors Customer Service Centre for further details.

PIN DESCRIPTIONS

Pin No.	Name	Type	Function	Pin No.	Name	Type	Function
1	AD_2	I	Multiplexed Address/Data	12	V_{SS}	S	Negative Power Supply
2	AD_3	I	Multiplexed Address/Data	13	PWMT	O	Top PWM Signal
3	AD_4	I	Multiplexed Address/Data	14	SET TRIP	I	Set Output Trip
4	AD_5	I	Multiplexed Address/Data	15	Intel ALE Motorola AS	I	Intel Address Latch Enable Motorola Address Strobe
5	AD_6	I	Multiplexed Address/Data				
6	AD_7	I	Multiplexed Address/Data (MSB)	16	Intel $\overline{RD}$ Motorola DS	I	Intel Read Strobe Motorola Data Strobe
7	$\overline{RST}$	I	Resets Internal Counters				
8	CLK	I	Clock Input	17	Intel $\overline{WR}$ Motorola R/$\overline{W}$	I	Intel Write Strobe Motorola Read/Write Select
9	$\overline{TRIP}$	O	Output Trip Status				
10	$\overline{CS}$	I	Chip Select	18	V_{DD}	S	Positive Power Supply
				19	AD_0	I	Multiplexed Address/Data(LSB)
11	PWMB	O	Bottom PWM Signal	20	AD_1	I	Multiplexed Address/Data

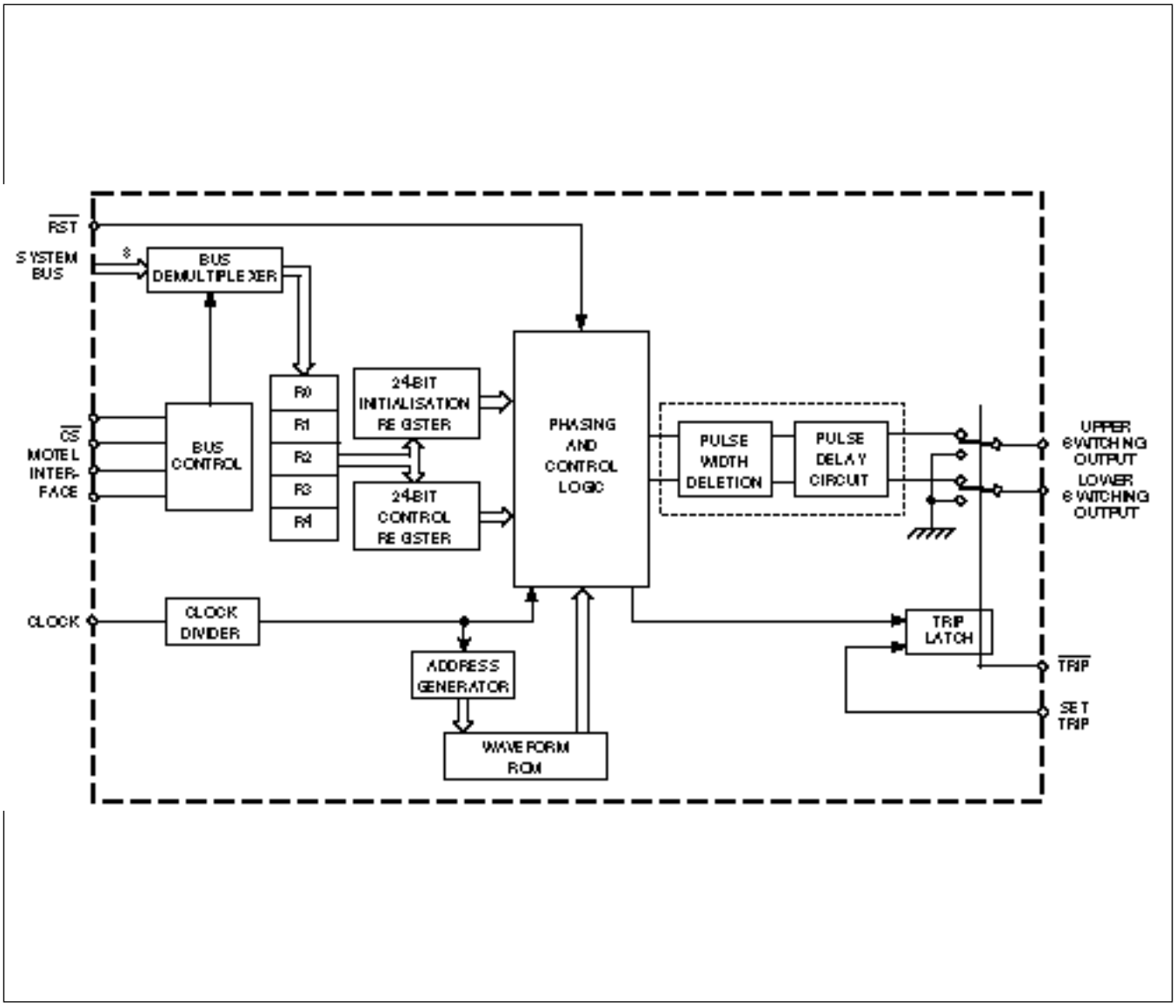


Fig.2 MA838 internal block diagram

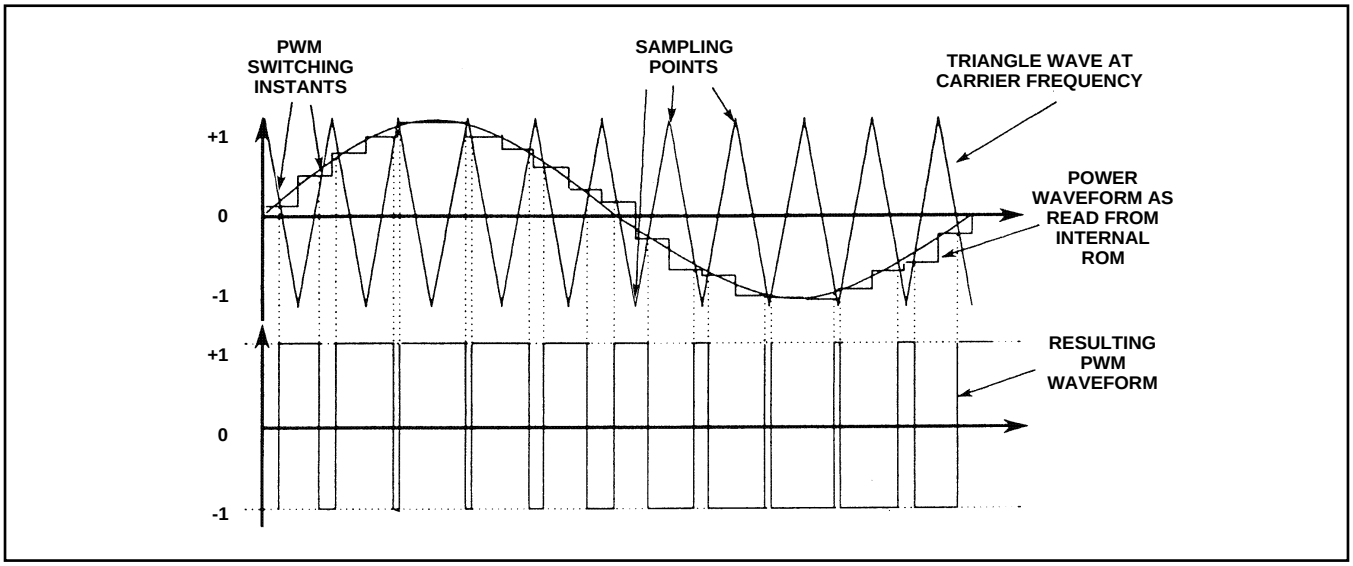


Fig.3 Asynchronous PWM generation with uniform or 'double-edged' regular sampling as used on the MA838

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig. 3. Two standard waveshape options exist so that the device can be adapted to particular applications (see PRODUCT DESIGNATION section for details). In addition, any symmetrical waveshape may be integrated on-chip, to order.

The triangle carrier wave frequency is selectable up to 24kHz (assuming the maximum clock frequency of 12.5MHz is used), enabling ultrasonic operation for noise critical applications. With 12.5MHz clock, power frequency ranges of up to 4kHz are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (deletes all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different systems simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking. Alternatively, braking may be implemented by setting the frequency to 0Hz. This is termed 'DC injection braking', in which the rotation of the motor is opposed by allowing DC to flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

Other possible MA838 applications are as a waveform generator as part of a switched-mode power supply (SMPS) or an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small transformer to be used.

MICROPROCESSOR INTERFACE

The MA838 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information refer to the description relevant to the microprocessor/controller being used.

Industry standard microprocessors such as the 8085, 8088, etc. and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the MA838. This interface consists of 8 data lines, AD_0 - AD_7 (write-only in this instance), which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$, DS and AS in Motorola mode, and a Chip Select input $\overline{CS}$, which allows the MA838 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the MA838 clock input.

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the MA838 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA838 are write only. However, this pin must be connected to $\overline{RD}$ (or tied high) to enable the MA838 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA838 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

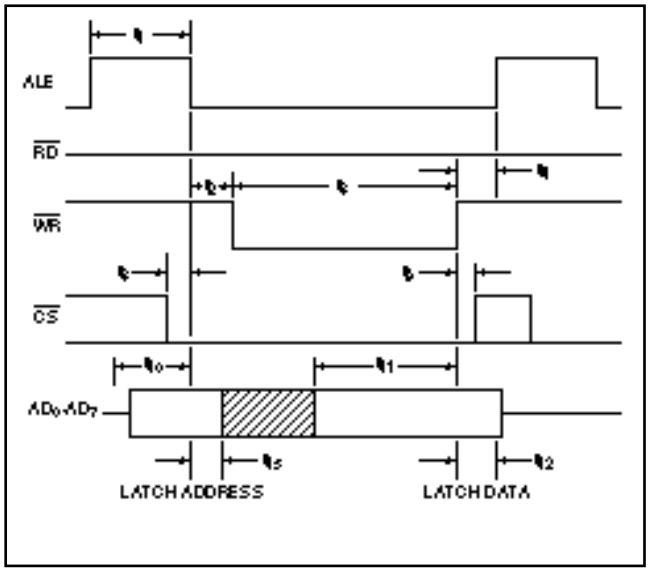


Fig. 4 Intel bus timing definitions

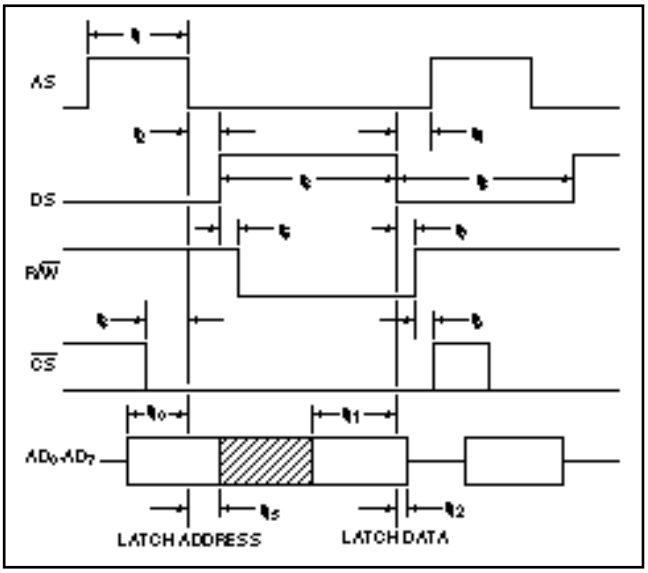


Fig. 5 Motorola bus timing definitions

Parameter	Symbol	Min.	Units
ALE high period	t_1	70	ns
Delay time, ALE to WR	t_2	40	ns
WR low period	t_3	200	ns
Delay time, WR high to ALE high	t_4	40	ns
CS setup time	t_8	20	ns
CS hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	25	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = ¯25°C

Parameter	Symbol	Min.	Units
AS high period	t_1	90	ns
Delay time, as low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/W low setup time	t_6	10	ns
R/W hold time	t_7	10	ns
CS setup time	t_8	20	ns
CS hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = ¯25°C

CONTROLLING THE MA838

The MA838 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded prior to the PWM outputs being activated and sets up the basic operating parameters associated with the load and inverter. This data would not normally be updated during PWM operation.

The control register is used to control the PWM outputs (and hence the load) during operation e.g., stop/start, speed etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit register is first written to three 8-bit temporary registers R0, R1 and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a dummy register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register, while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is written to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted upon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	1	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	1	R3	Transfers control data
1	0	0	R4	Transfers initialisation data

Table 3 MA838 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified while $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whereas high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power Frequency Range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn- off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the MA838 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by writing to the dummy register R4.

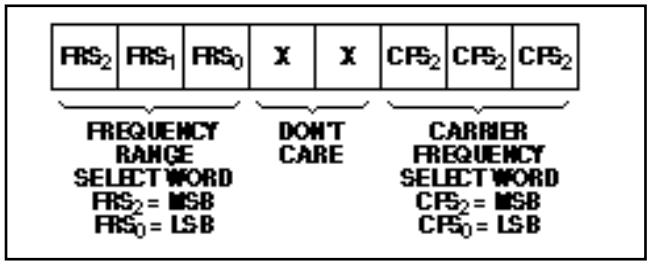


Fig. 6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where *k* = clock frequency and *n* = 1, 2, 4, 8, 16 or 32 (as set by FRS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplicaion factor m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and m = 1, 2, 4, 8, 16, 32 or 64 (as set by FRS).

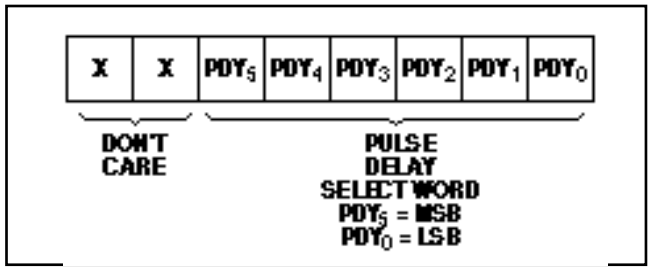


Fig. 7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and *pdy*, defined by the 6-bit pulse delay time select word (PDY). The value of *pdy* is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where *pdy* = 1- 64 (as set by PDY) and f_{CARR} = carrier frequency.

Fig 8 shows the eftect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig. 2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by t_{pd} -t_{pdy}.

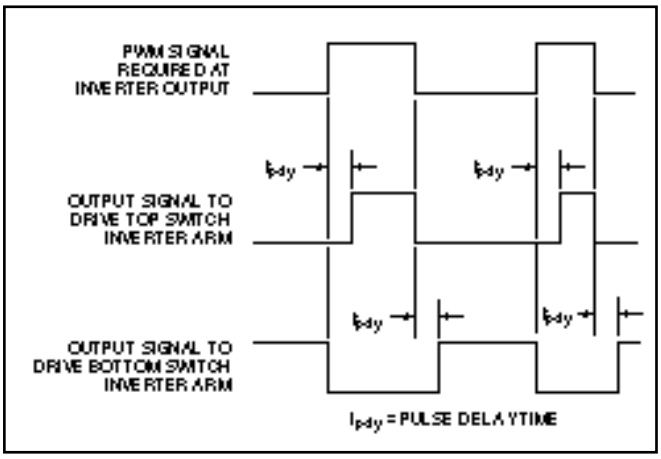


Fig. 8 Effect of pulse delay on PWM pulse train

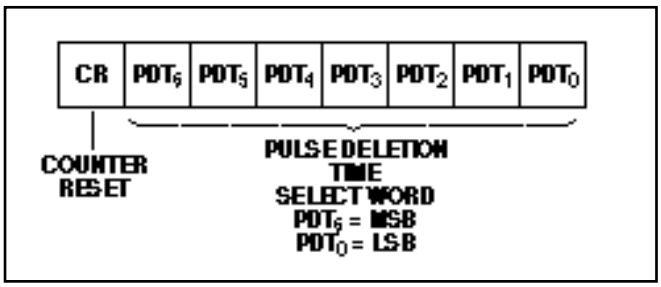


Fig. 9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register. If a pulse (either +ve or -ve) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd} , is a function of the carrier wave frequency and *pdt*, defined by the 7-bit pulse deletion time word (PDT). The value of *pdt* is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where *pdt* = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

Counter reset

When the CR bit is active (i.e., low) the internal power frequency phase counter is set to 0 degrees. The power frequency is then set to 0Hz and cannot be changed via the normal frequency control.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-squarewave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

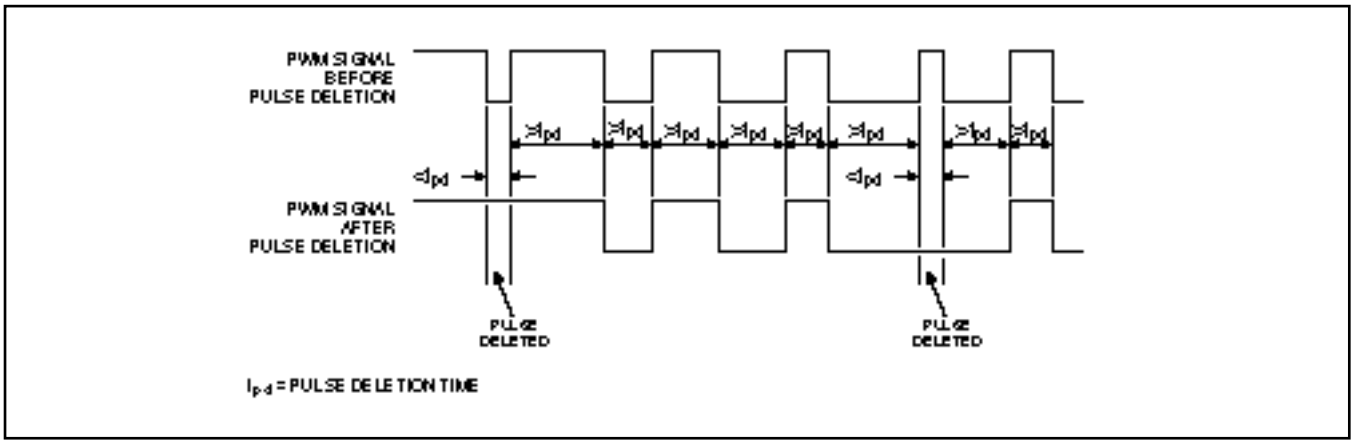


Fig. 10 The effect of the pulse deletion circuit

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the MA838.

As with the initialisation register, control register data is loaded into the three 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by writing to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

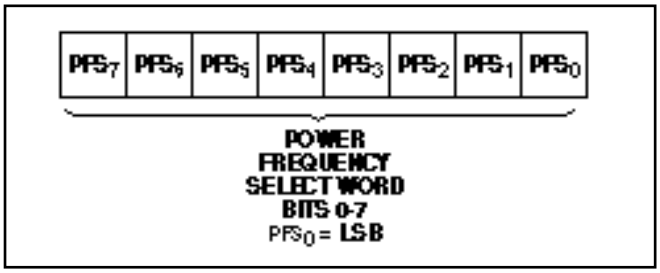


Fig. 11 Temporary register R0

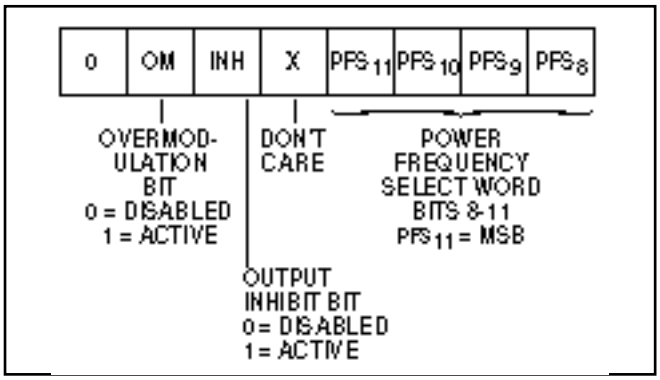


Fig. 12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3.

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where *pfs* = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit OM is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word.

The percentage amplitude control is now given by:

$$\text{Overmodulated Amplitude} = A_{POWER} + 100\%$$

where A_{POWER} = the power amplitude

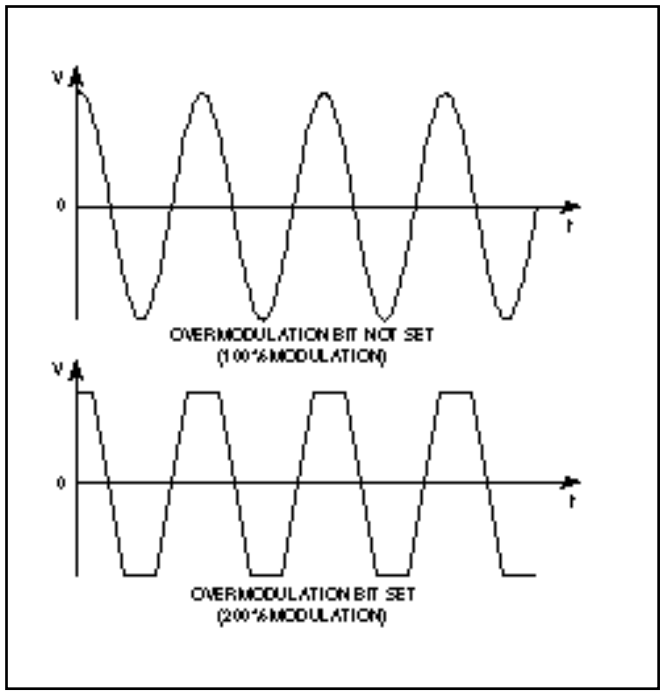


Fig. 13 Voltage waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit

Amplitude selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the internal ROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{255} \times 100\%$$

where *A* = decimal value of AMP.

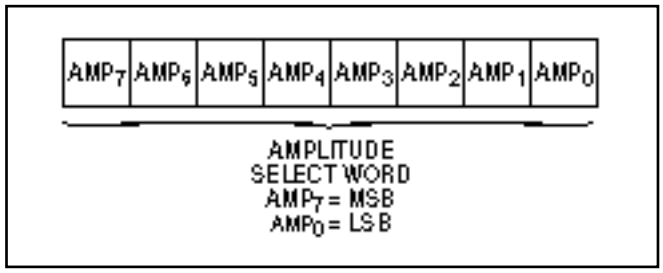


Fig.14 Temporary register R2

POWER-UP C0NDITIONS

All bits in both the Initialisation and Control registers power-up in the low state. This means that Counter Reset (CR) is active and a 50% duty cycle will be output from all PWM outputs until further initialising action is taken. Holding RST low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e., low) during this period.

MA838 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12·288 MHz is used (12·288 MHz crystals are readily available). This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10µs and an underlap of 5µs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of *n* that will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow n = \frac{k}{512 \times f_{CARR}} = \frac{12{\cdot}288 \times 10^6}{512 \times 6 \times 10^3} = 4$$

From Table 4, *n* = 4 corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of *m* that will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

$$\Rightarrow m = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = 16$$

From Table 5, *m* = 16 corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of *pdy* that will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15{\cdot}4}$$

However, the value of *pdy* must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to *pdy* this gives a delay time of 5·2µs. From Table 6, *pdy* = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time must, in this instance, be set 5·2µs longer than the minimum pulse length required

Minimum pulse length required = 10µs

t_{PD} to be set to 10µs + 5·2µs = +15·2µs

Now,

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15{\cdot}2 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{46{\cdot}7}$$

Again, *pdt* must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 46 for *pdt*, this gives a value of t_{pd}, of 15 µs and an actual minimum pulse width of 15 – 5·2µs = 9·8µs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transter into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

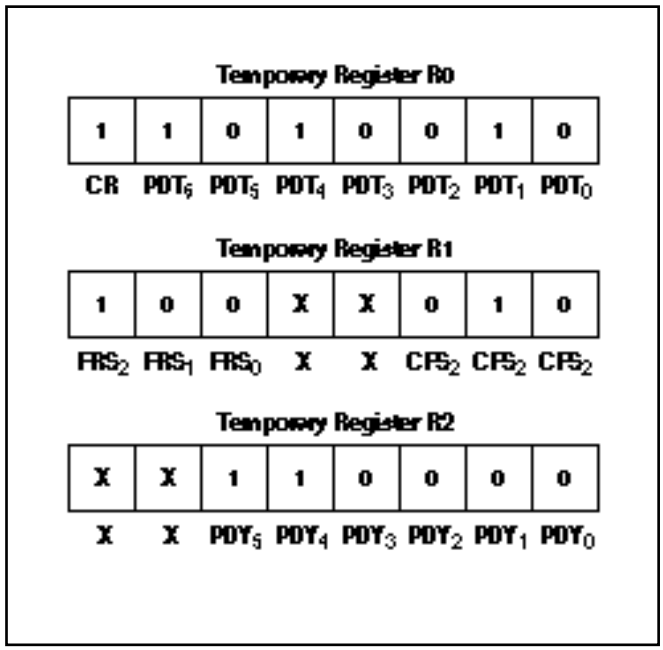


Fig. 15

Control Register Programming Example

The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the initialisation register has already heen programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the ROM. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e 4096 equal steps) from 0Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz, the power frequency can be adjusted in increments of 0·06Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow pfs = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = 1638{\cdot}4$$

We can only have *pfs* as an integer, so if we assign *pfs* = 1638 this gives f_{POWER} = 99.97 Hz.The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, output inhibit

Overmodulation is not required therefore OM = 0.

Output inhibit should be inactive (i e., the outputs should be active), therefore INH= 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{225} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80\ 3x\ 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2. The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

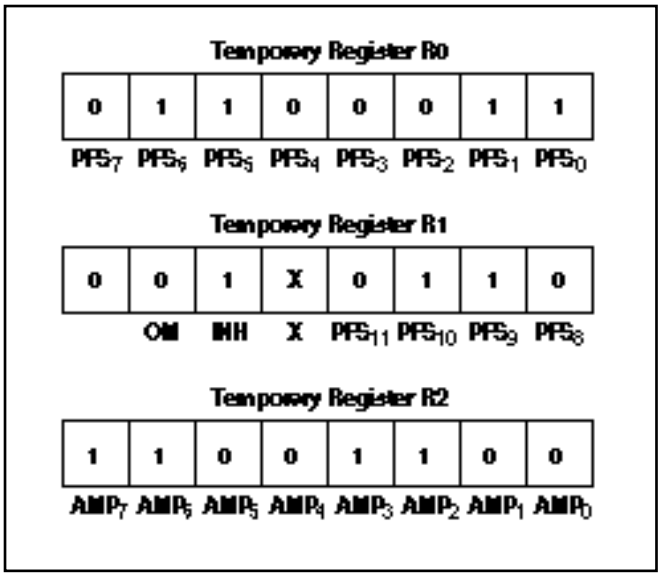


Fig. 16

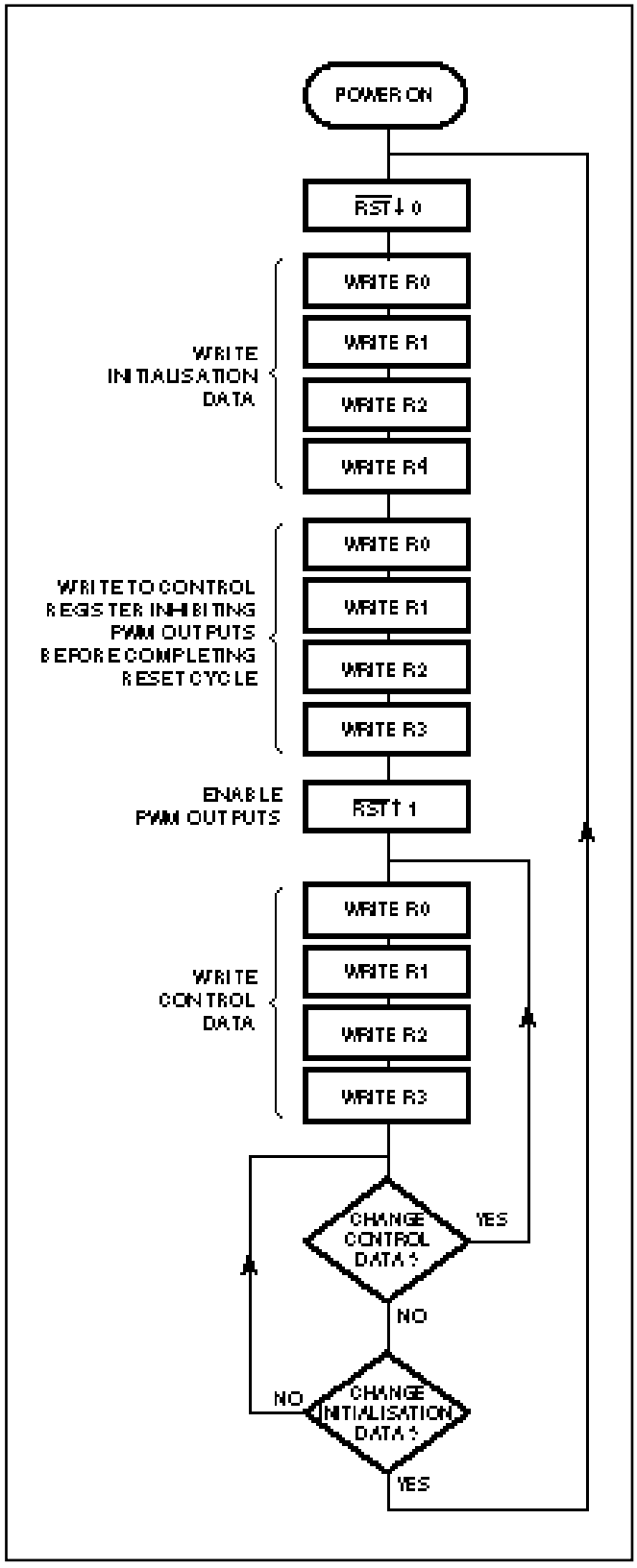


Fig. 17 Typical MA838 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the TRIP output and the PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the RST input.

It is essential that when not in use this pin is tied low and isolated from potential sources of noise; on no account should it be left floating.

SET TRIP is latched internally at the master clock rate in order to reduce noise sensitivity.

Output Trip Status (TRIP output)

The TRIP output indicates the status of the output trip latch and is active low.

Reset (RST input)

The RST input performs the following functions when active (low):

1. PWM outputs are forced low (if not already low) thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. The rising edge of RST reactivates the PWM outputs resetting the output trip and setting the TRIP output high – assuming that the SET TRIP input is inactive (i.e. low).

Clock (CLK input)

The CLK input provides a timing reference used by the MA838 for all timings related to the PWM outputs. The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the MA838 may be run either from the same or from different clocks.

Waveform segment	Sample number
0°- 30°	0 - 127
30·23°- 60°	128 - 255
60·23°- 89·77°	256 - 383

Table 8 90° of the 360° cycle is divided into 384 8-bit samples

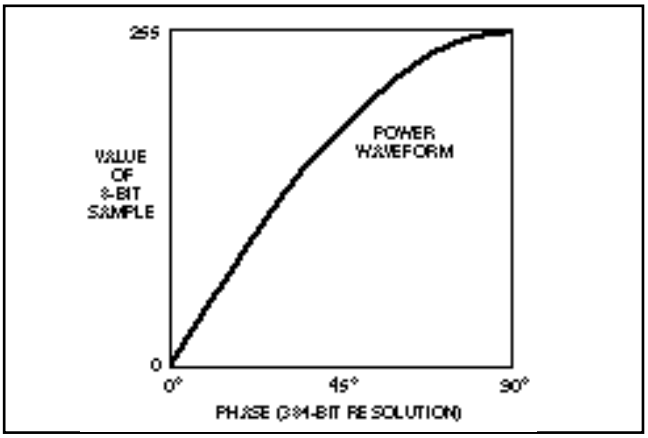


Fig. 18 90° sample of typical power waveform

WAVEFORM DEFINITION

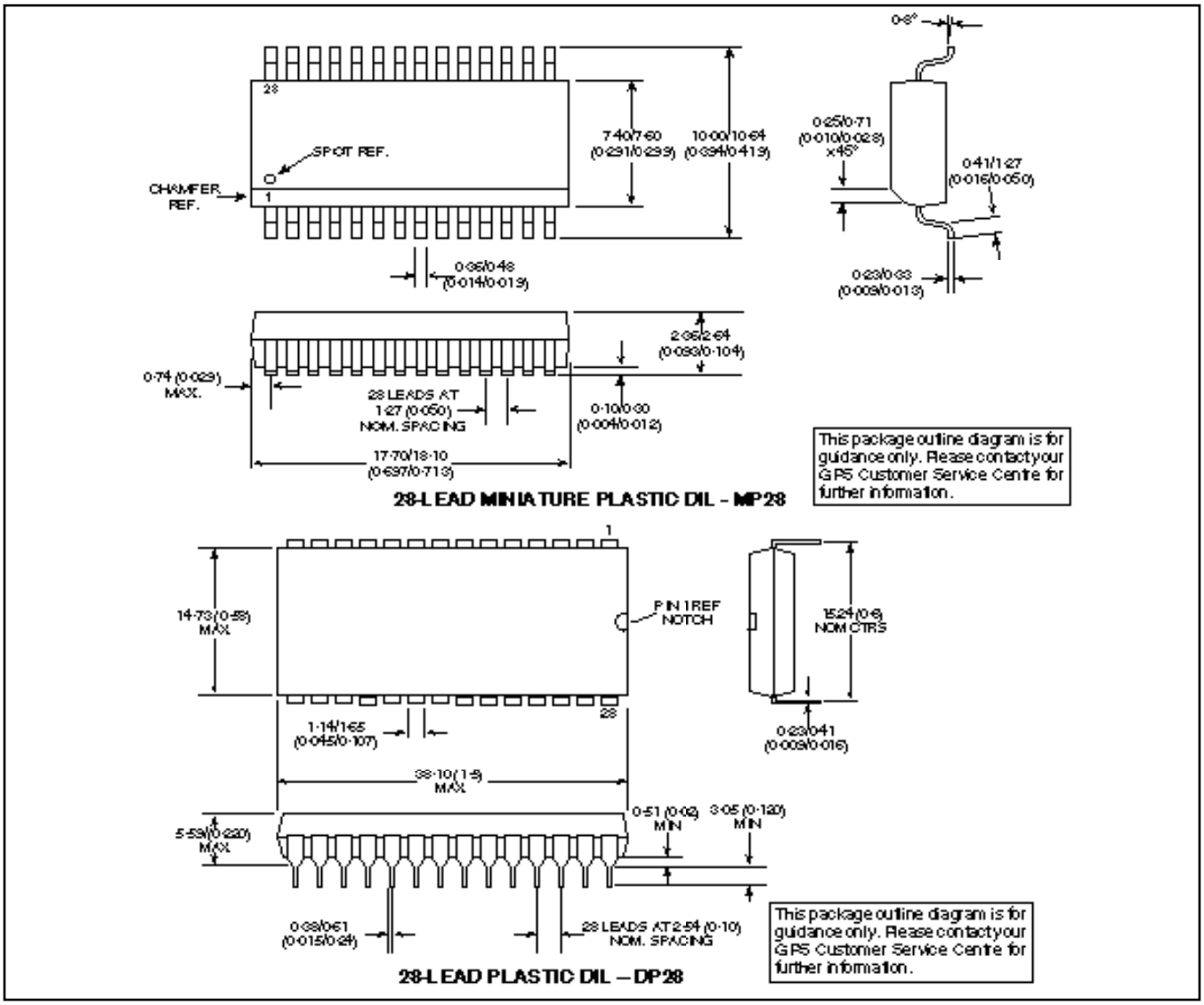
The waveform amplitude data used to construct the PWM output sequence is read from the internal 384 x 8 ROM. This contains the 90° span of the waveform as shown in Fig. 18. Each successive 8-bit sample linearly represents the instantaneous amplitude of the waveform. It is assumed that the waveform is symmetrical about the 90°, 180° and 270° axes.The MA828 reconstructs the full 360° waveform by reading the 0°-90° section held in ROM and assigning negative values for the second half of the cycle.

The 384 8-bit samples are regularly spaced over the 0° to 90° span, giving an angular resolution of approximately 0·23°.

MA838

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



GEC PLESSEY
SEMICONDUCTORS

HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire, United Kingdom SN2 2QW.
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017
1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America.
Tel: (408) 438 2900
Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES
- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 69 18 90 00 Fax: (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 3609 06-0 Fax: (089) 3609 06-55
- **ITALY** Milan Tel: (02) 66040867 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 5276-5501 Fax: (03) 5276-5510
- **NORTH AMERICA** Scotts Valley, USA Tel: (408) 438 2900 Fax: (408) 438 7023
- **SOUTH EAST ASIA** Singapore Tel: (65) 3827708 Fax: (65) 3828872
- **SWEDEN** Stockholm, Tel: 46 8 702 97 70 Fax: 46 8 640 47 36
- **TAIWAN, ROC** Taipei, Tel: 886 2 5461260 Fax: 886 2 7190260
- **UK, EIRE, DENMARK, FINLAND & NORWAY**
  Swindon Tel: (01793) 518510 Fax: (01793) 518582

These are supported by Agents and Distributors in major countries world-wide.

© GEC Plessey Semiconductors 1995 Publication No. DS3798 Issue No. 3.1 July 1995
TECHNICAL DOCUMENTATION - NOT FOR RESALE. PRINTED IN UNITED KINGDOM.

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior notice the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.