GSM Power Management System

ADP3408

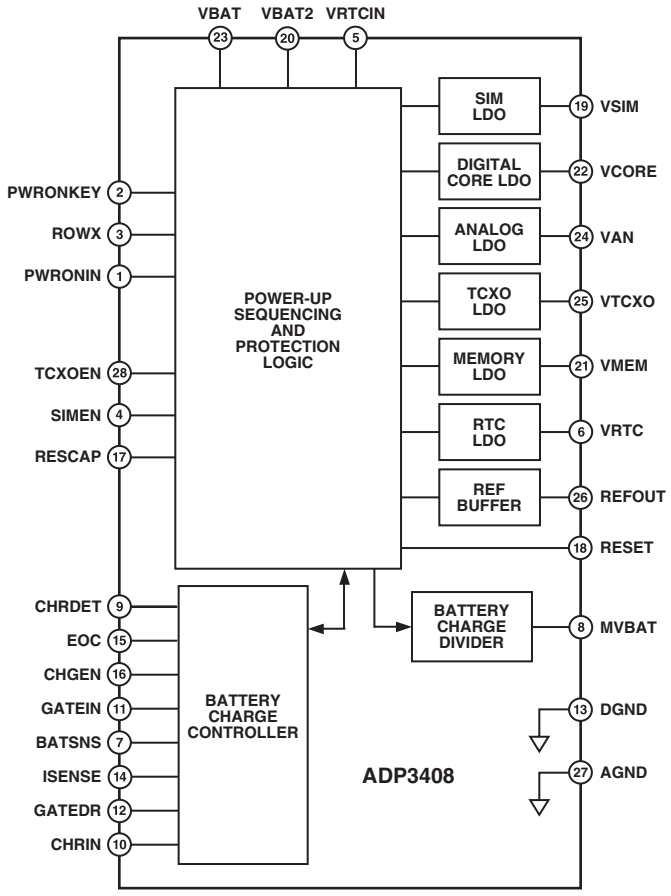
FEATURES

Handles All GSM Baseband Power Management
6 LDOs Optimized for Specific GSM Subsystems
Li-Ion and NiMH Battery Charge Function
Optimized for the AD20msp430 Baseband Chipset

APPLICATIONS

GSM/DCS/PCS/CDMA Handsets

FUNCTIONAL BLOCK DIAGRAM



(Pin Assignment Is for TSSOP Option)

GENERAL DESCRIPTION

The ADP3408 is a multifunction power system chip optimized for GSM handsets, especially those based on the Analog Devices AD20msp430 system solution. It contains six LDOs, one to power each of the critical GSM subblocks. Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm. The charge circuit maintains low current charging during the initial charge phase and provides an end-of-charge signal when a Li-ion battery is being charged.

The ADP3408 is specified over the temperature range of –20°C to +85°C and is available in a narrow body TSSOP 28-lead package or 5 mm × 5 mm LFCSP 32-lead package.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703
© Analog Devices, Inc., 2002

ADP3408–SPECIFICATIONS[1] (–20°C ≤ T_A ≤ +85°C, VBAT = VBAT2 = 3 V–5.5 V, CVSIM = CVCORE = CVAN = CVMEM = 2.2 μF, VTCXO = 0.22 μF, CVRTC = 0.1 μF, CVBAT = 10 μF, minimum loads applied on all outputs, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SHUTDOWN SUPPLY CURRENT	ICC					
VBAT ≤ 2.5 V (Deep Discharged Lockout Active)		VBAT = VBAT2 = 2.3 V		7	20	μA
2.5 V < VBAT ≤ 3.2 V (UVLO Active)		VBAT = VBAT2 = 3.0 V		30	55	μA
VBAT > 3.2 V		VBAT = VBAT2 = 4.0 V		45	80	μA
OPERATING GROUND CURRENT	IGND	VBAT = 3.6 V				
VSIM, VCORE, VMEM, VRTC On		Minimum Loads		225	300	μA
All LDOs On		Minimum Loads		345	450	μA
		Maximum Loads		1.0	3.0	% of max load current
UVLO ON THRESHOLD	VBAT			3.2	3.3	V
UVLO HYSTERESIS	VBAT			200		mV
DEEP DISCHARGED LOCKOUT ON THRESHOLD	VBAT			2.4	2.75	V
DEEP DISCHARGED LOCKOUT HYSTERESIS	VBAT			100		mV
INPUT HIGH VOLTAGE	V_{IH}					
(TCXOEN, SIMEN, CHGEN, GATEIN)			2.0			V
PWRONIN (ADP3408-1.8)			1.1			V
PWRONIN (ADP3408-2.5)			2.0			V
INPUT LOW VOLTAGE (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	V_{IL}				0.3	V
INPUT HIGH BIAS CURRENT (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	I_{IH}				1.0	μA
INPUT LOW BIAS CURRENT (PWRONIN, TCXOEN, SIMEN, CHGEN, GATEIN)	I_{IL}		–1.0			μA
PWRONKEY INPUT HIGH VOLTAGE	V_{IH}		0.7 × VBAT			V
PWRONKEY INPUT LOW VOLTAGE	V_{IL}				0.3 × VBAT	V
PWRONKEY INPUT PULL-UP RESISTANCE TO VBAT			70	100	130	kΩ
THERMAL SHUTDOWN THRESHOLD[2]				160		°C
THERMAL SHUTDOWN HYSTERESIS				45		°C
ROWX CHARACTERISTICS						
ROWX Output Low Voltage	V_{OL}	PWRONKEY = Low				
		I_{OL} = 200 μA			0.4	V
ROWX Output High Leakage Current	I_{IH}	PWRONKEY = High V(ROWX) = 5 V			1	μA
SIM CARD LDO (VSIM)						
Output Voltage	VSIM	Line, Load, Temp	2.80	2.85	2.92	V
Line Regulation	ΔVSIM	Min Load		2		mV
Load Regulation	ΔVSIM	50 μA ≤ I_{LOAD} ≤ 20 mA, VBAT = 3.6 V		1		mV
Output Capacitor Required for Stability	C_O		2.2			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV, I_{LOAD} = 20 mA		35	100	mV
DIGITAL CORE LDO (VCORE)						
Output Voltage						
ADP3408ARU-2.5	VCORE	Line, Load, Temp	2.40	2.45	2.50	V
ADP3408ARU-1.8	VCORE	Line, Load, Temp	1.75	1.80	1.85	V
Line Regulation	ΔVCORE	Min Load		2		mV
Load Regulation	ΔVCORE	50 μA ≤ I_{LOAD} ≤ 100 mA, VBAT = 3.6 V		7		mV
Output Capacitor Required for Stability	C_O		2.2			μF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RTC LDO						
REAL-TIME CLOCK LDO/						
COIN CELL CHARGER (VRTC)						
Maximum Output Voltage						
ADP3408ARU-2.5	VRTC	1 µA ≤ I_{LOAD} ≤ 10 µA	2.39	2.45	2.51	V
ADP3408ARU-1.8	VRTC	1 µA ≤ I_{LOAD} ≤ 10 µA	1.80	1.95	2.1	V
Off Reverse Input Current	I_L	VBAT = 2.15 V, T_A = 25°C			0.5	µA
Output Capacitor Required for Stability	C_O		0.1			µF
ANALOG LDO (VAN)						
Output Voltage	VAN	Line, Load, Temp	2.40	2.45	2.50	V
Line Regulation	ΔVAN	Min Load		2		mV
Load Regulation	ΔVAN	50 µA ≤ I_{LOAD} ≤ 130 mA, VBAT = 3.6 V		8		mV
Output Capacitor Required for Stability	C_O		2.2			µF
Ripple Rejection	ΔVBAT/ ΔVAN	f = 217 Hz VBAT = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 130 mA VBAT = 3.6 V		80		µV rms
TCXO LDO (VTCXO)						
Output Voltage						
ADP3408-2.5	VTCXO	Line, Load, Temp	2.66	2.715	2.77	V
ADP3408-1.8	VTCXO	Line, Load, Temp	2.711	2.750	2.789	V
Line Regulation	ΔVTCXO	Min Load		2		mV
Load Regulation	ΔVTCXO	50 µA ≤ I_{LOAD} ≤ 20 mA, VBAT = 3.6 V		1		mV
Output Capacitor Required for Stability	C_O		0.22			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 20 mA		160	310	mV
Ripple Rejection	ΔVBAT/ ΔVTCXO	f = 217 Hz VBAT = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 20 mA, VBAT = 3.6 V		80		µV rms
MEMORY LDO (VMEM)						
Output Voltage	VMEM	Line, Load, Temp	2.744	2.80	2.856	V
Line Regulation	ΔVMEM	Min Load		2		mV
Load Regulation	ΔVMEM	50 µA < I_{LOAD} < 60 mA, VBAT = 3.6 V		3		mV
Output Capacitor Required for Stability	C_O		2.2			µF
Dropout Voltage		I_{LOAD} = 60 mA		80	180	mV
		I_{LOAD} = 80 mA		107	210	mV
REFOUT						
Output Voltage	VREFOUT	Line, Load, Temp	1.19	1.210	1.23	V
Line Regulation	ΔVREFOUT	Min Load		0.2		mV
Load Regulation	ΔVREFOUT	0 µA < I_{LOAD} < 50 µA VBAT = 3.6 V		0.5		mV
Ripple Rejection	ΔVBAT/ ΔVREFOUT	f = 217 Hz VBAT = 3.6 V, I_{LOAD} = 50 µA	65	75		dB
Maximum Capacitive Load	C_O		100			pF
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz, VBAT = 3.6 V		40		µV rms
RESET GENERATOR (RESET)						
Output High Voltage	V_{OH}	I_{OH} = 500 µA	V_{MEM} – 0.25			V
Output Low Voltage	V_{OL}	I_{OL} = –500 µA			0.25	V
Output Current	I_{OL}	V_{OL} = 0.25 V,		1		mA
	I_{OH}	V_{OH} = V_{MEM} – 0.25 V		1		mA
Delay Time per Unit Capacitance Applied to RESCAP Pin	T_D		0.6	1.2	2.4	ms/nF
BATTERY VOLTAGE DIVIDER						
Divider Ratio	BATSNS/MVBAT	TCXOEN = High	2.32	2.35	2.37	
Divider Impedance at MVBAT	Z_O		59.5	85	110	kΩ
Divider Leakage Current		TCXOEN = Low			1	µA
Divider Resistance		TCXOEN = High	215	300	385	kΩ

Parameter	Symbol	Condition	Min	Typ	Max	Unit
BATTERY CHARGER						
Charger Output Voltage	BATSNS	4.35 V ≤ CHRIN ≤ 10 V[3] CHGEN = Low, No Load	4.150	4.200	4.250	V
		CHRIN = 10 V CHGEN = Low, No Load 0°C < T_A < 50°C	4.155		4.230	V
Load Regulation	ΔBATSNS	CHRIN = 5 V 0 ≤ CHRIN – ISENSE < Current Limit Threshold CHGEN = Low			15	mV
CHRDET On Threshold	CHRIN – BATSNS		30	90	150	mV
CHRDET Hysteresis				40		mV
CHRDET Off Delay[4]		CHRIN < VBAT		6		ms/nF
CHRIN Supply Current		CHRIN = 5 V		0.6		mA
BATTERY CHARGER						
Current Limit Threshold	CHRIN – ISENSE					
High Current Limit (UVLO Not Active)		CHRIN = 5 V DC VBAT = 3.6 V CHGEN = Low	142	160	190	mV
		CHRIN = 5 V DC VBAT = 3.6 V CHGEN = Low 0°C < T_A < 50°C	149	160	180	mV
Low Current Limit (UVLO Active)		VBAT = 2 V CHGEN = Low CHRIN = 5 V		20	35	mV
ISENSE Bias Current				200		µA
End-of-Charge Signal Threshold	CHRIN – ISENSE	CHRIN = 5 V DC VBAT > 4.0 V CHGEN = Low		14	35	mV
EOC Reset Threshold	VBAT	CHGEN = Low	3.82	3.96	4.10	V
GATEDR Transition Time	t_R, t_F	CHRIN = 5 V VBAT > 3.6 V CHGEN = High, C_L = 2 nF	0.1		1	µs
GATEDR High Voltage	V_{OH}	CHRIN = 5 V VBAT = 3.6 V CHGEN = High, GATEIN = High I_{OH} = –1 mA	4.5			V
GATEDR Low Voltage	V_{OL}	CHRIN = 5 V VBAT = 3.6 V CHGEN = High GATEIN = Low I_{OL} = 1 mA			0.5	V
Output High Voltage (EOC, CHRDET)	V_{OH}	I_{OH} = –250 µA	2.4			V
Output Low Voltage (EOC, CHRDET)	V_{OL}	I_{OL} = +250 µA			0.25	V
Battery Overvoltage Protection Threshold (GATEDR → High)	BATSNS	CHRIN = 7.5 V CHGEN = High GATEIN = Low	5.30	5.50	5.70	V
Battery Overvoltage Protection Hysteresis	BATSNS	CHRIN = 7.5 V CHGEN = High GATEIN = Low		200		mV

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]This feature is intended to protect against catastrophic failure of the device. Maximum allowed operating junction temperature is 125°C. Operation beyond 125°C could cause permanent damage to the device.

[3]No isolation diode present between charger input and battery.

[4]Delay set by external capacitor on the RESCAP pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin with respect to
any GND Pin . . . . . –0.3 V to +10 V
Voltage on any pin may not exceed VBAT, with the following exceptions: CHRIN, GATEDR, ISENSE
Storage Temperature Range . . . . . –65°C to +150°C
Operating Ambient Temperature Range . . . . . –20°C to +85°C
Maximum Junction Temperature . . . . . 125°C
θ_{JA}, Thermal Impedance (TSSOP-28)
4-Layer JEDEC PCB . . . . . 68°C/W
2-Layer SEMI PCB . . . . . 98°C/W
θ_{JA}, Thermal Impedance (LFCSP)
4-Layer JEDEC PCB . . . . . 32°C/W
2-Layer SEMI PCB . . . . . 108°C/W
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

Model	Core LDO Output Voltage	Temperature Range	Package Option
ADP3408ARU-2.5	2.5 V	–20°C to +85°C	RU-28
ADP3408ACP-2.5	2.5 V	–20°C to +85°C	CP-32
ADP3408ARU-1.8	1.8 V	–20°C to +85°C	RU-28
ADP3408ACP-1.8	1.8 V	–20°C to +85°C	CP-32

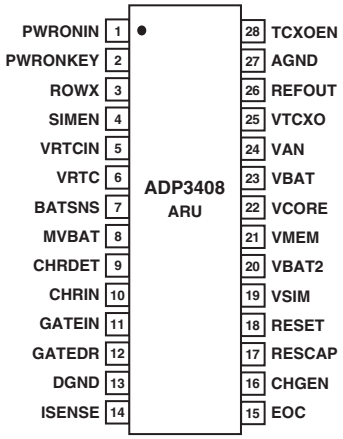
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3408 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

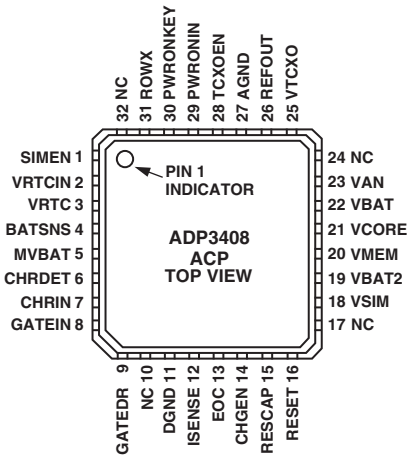


PIN CONFIGURATIONS

TSSOP (RU)



LFCSP (CP)



PIN FUNCTION DESCRIPTIONS

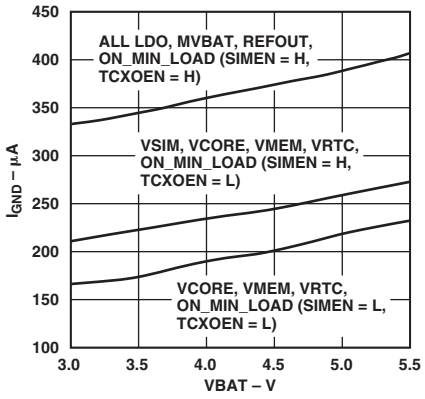
TSSOP Pin	LFCSP Pin	Mnemonic	Function
1	29	PWRONIN	Power On/Off Signal from Microprocessor
2	30	PWRONKEY	Power On/Off Key
3	31	ROWX	Power Key Interface Output
4	1	SIMEN	SIM LDO Enable
5	2	VRTCIN	RTC LDO Input Voltage
6	3	VRTC	Real-Time Clock Supply/Coin Cell Battery Charger
7	4	BATSNS	Battery Voltage Sense Input
8	5	MVBAT	Divided Battery Voltage Output
9	6	CHRDET	Charge Detect Output
10	7	CHRIN	Charger Input Voltage
11	8	GATEIN	Microprocessor Gate Input Signal
12	9	GATEDR	Gate Drive Output
13	11	DGND	Digital Ground
14	12	ISENSE	Charge Current Sense Input
15	13	EOC	End of Charge Signal
16	14	CHGEN	Charger Enable for GATEIN, NiMH Pulse Charging
17	15	RESCAP	Reset Delay Time
18	16	RESET	Main Reset
19	18	VSIM	SIM LDO Output
20	19	VBAT2	Battery Input Voltage 2
21	20	VMEM	Memory LDO Output
22	21	VCORE	Digital Core LDO Output
23	22	VBAT	Battery Input Voltage
24	23	VAN	Analog LDO Output
25	25	VTCXO	TCXO LDO Output
26	26	REFOUT	Output Reference
27	27	AGND	Analog Ground
28	28	TCXOEN	TCXO LDO Enable and MVBAT Enable
	10, 17, 24, 32	NC	No Connection

Table I. LDO Control Logic

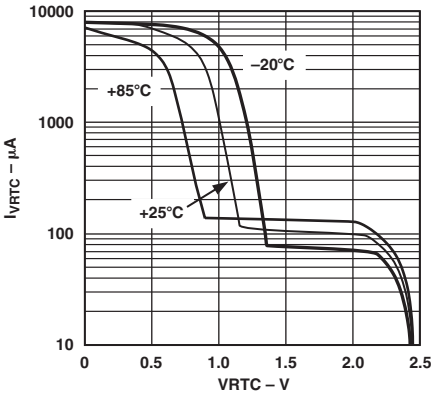
PHONE STATUS	DDLO	UVLO*	CHRDET	PWRONKEY	PWRONIN	TCXOEN	SIMEN	VSIM	VCORE	VAN and REFOUT	VTCXO	VMEM	VRTC	MVBAT
State #1 Battery Deep Discharged	L	X	X	X	X	L	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF
State #2 Phone Off	H	L	X	X	X	L	X	OFF	OFF	OFF	OFF	OFF	ON	OFF
State #3 Phone Off, Turn-On Allowed	H	H	L	H	L	L	X	OFF	OFF	OFF	OFF	OFF	ON	OFF
State #4 Charger Applied	H	H	H	X	X	L	L	OFF	ON	ON	ON	ON	ON	OFF
State #5 Phone Turned On by User Key	H	H	X	L	X	L	L	OFF	ON	ON	ON	ON	ON	OFF
State #6 Phone Turned On by BB	H	H	L	H	H	L	L	OFF	ON	OFF	OFF	ON	ON	OFF
State #7 Enable SIM Card	H	H	L	H	H	L	H	ON	ON	OFF	OFF	ON	ON	OFF
State #8 Phone and TCXO LDO Kept On by BB	H	H	L	H	H	H	H	ON	ON	ON	ON	ON	ON	ON

*UVLO is active only when phone is turned off. UVLO is ignored once the phone is turned on.

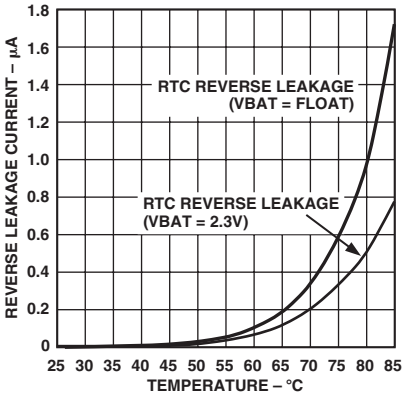
ADP3408–Typical Performance Characteristics



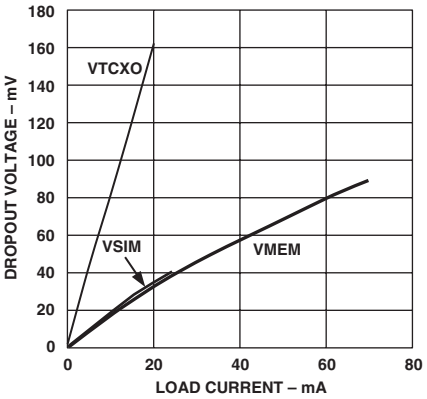
TPC 1. Ground Current vs. Battery Voltage



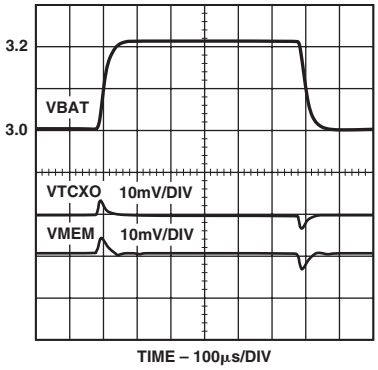
TPC 2. RTC I/V Characteristic



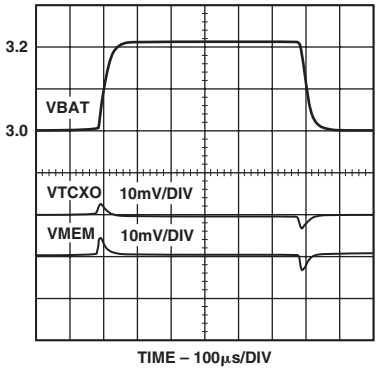
TPC 3. VRTC Reverse Leakage Current vs. Temperature



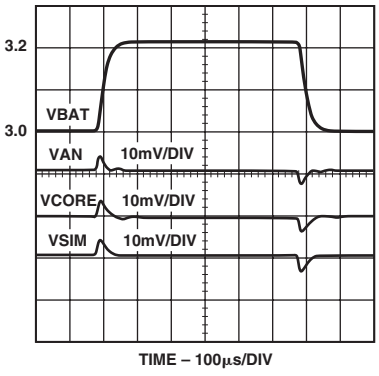
TPC 4. Dropout Voltage vs. Load Current



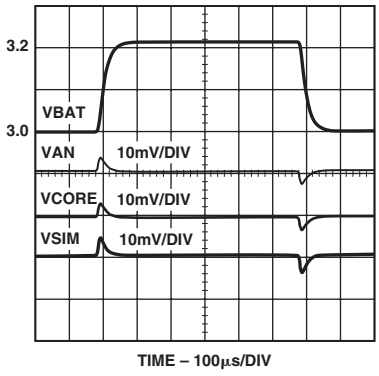
TPC 5. Line Transient Response, Minimum Loads



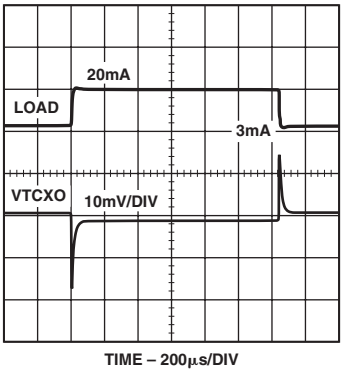
TPC 6. Line Transient Response, Maximum Loads



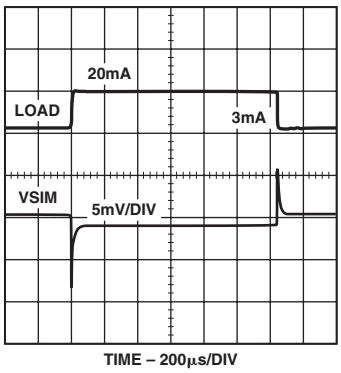
TPC 7. Line Transient Response, Minimum Loads



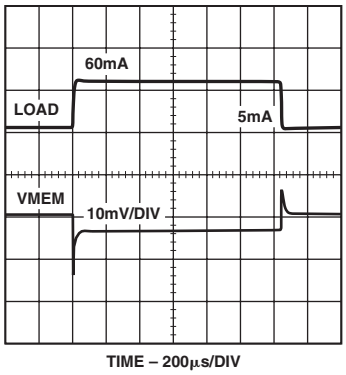
TPC 8. Line Transient Response, Maximum Loads



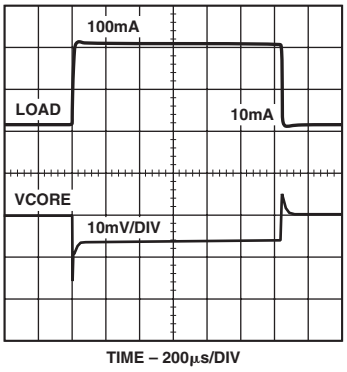
TPC 9. VTCXO Load Step



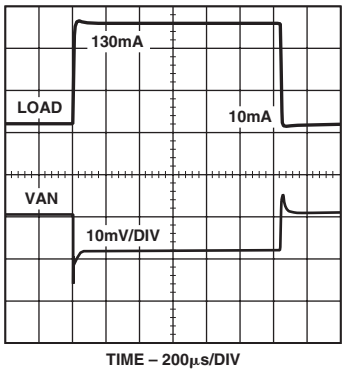
TPC 10. VSIM Load Step



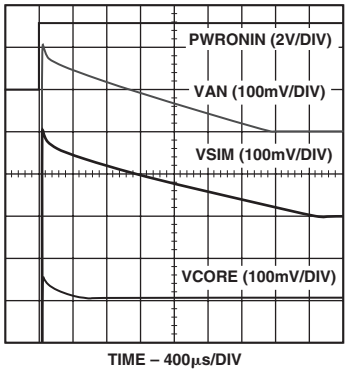
TPC 11. VMEM Load Step



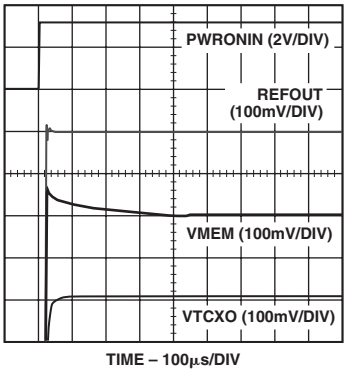
TPC 12. VCORE Load Step



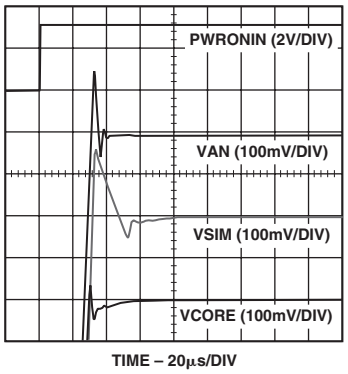
TPC 13. VAN Load Step



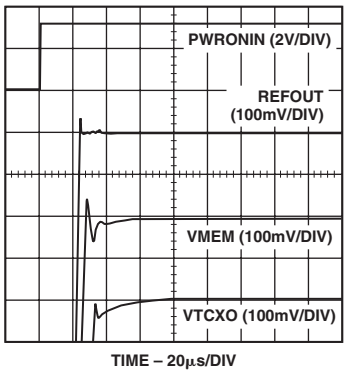
TPC 14. Turn On Transient by PWRONIN, Minimum Load (Part 1)



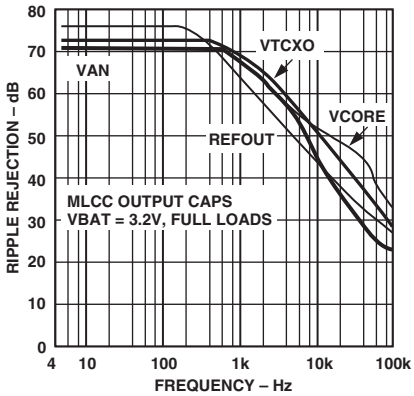
TPC 15. Turn On Transient by PWRONIN, Minimum Load (Part 2)



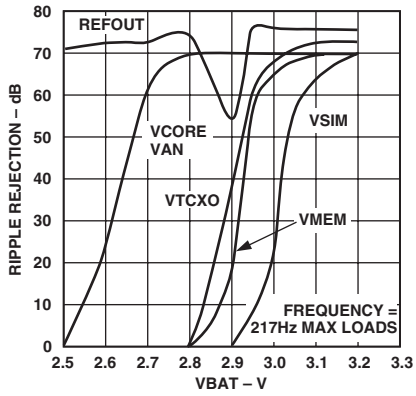
TPC 16. Turn On Transient by PWRONIN, Maximum Load (Part 1)



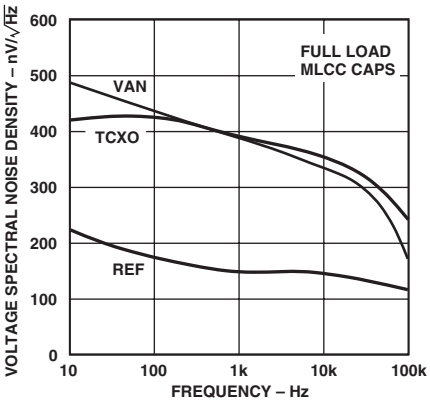
TPC 17. Turn On Transient by PWRONIN, Maximum Load (Part 2)



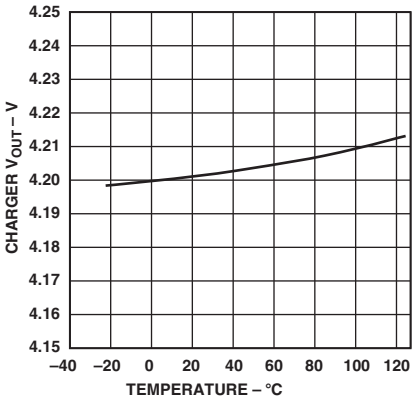
TPC 18. Ripple Rejection vs. Frequency



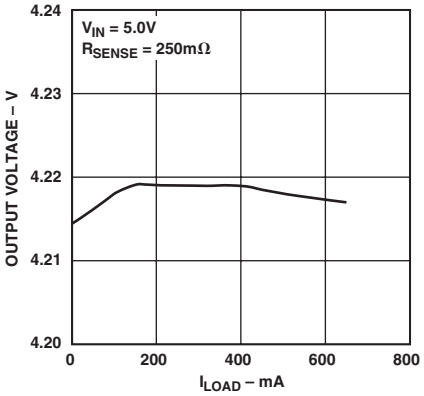
TPC 19. Ripple Rejection vs. Battery Voltage



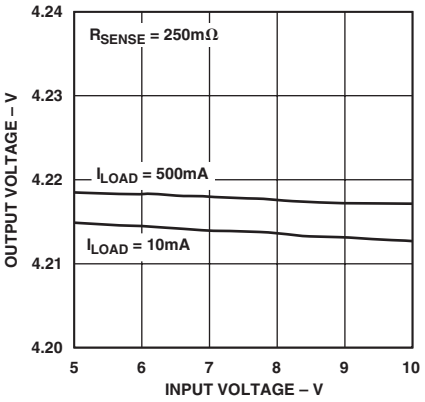
TPC 20. Output Noise Density



TPC 21. Charger V_{OUT} vs. Temperature, V_{IN} = 5.0 V, I_{LOAD} = 10 mA



TPC 22. Charger V_{OUT} vs. I_{LOAD} (V_{IN} = 5.0 V)



TPC 23. Charger V_{OUT} vs. V_{IN}

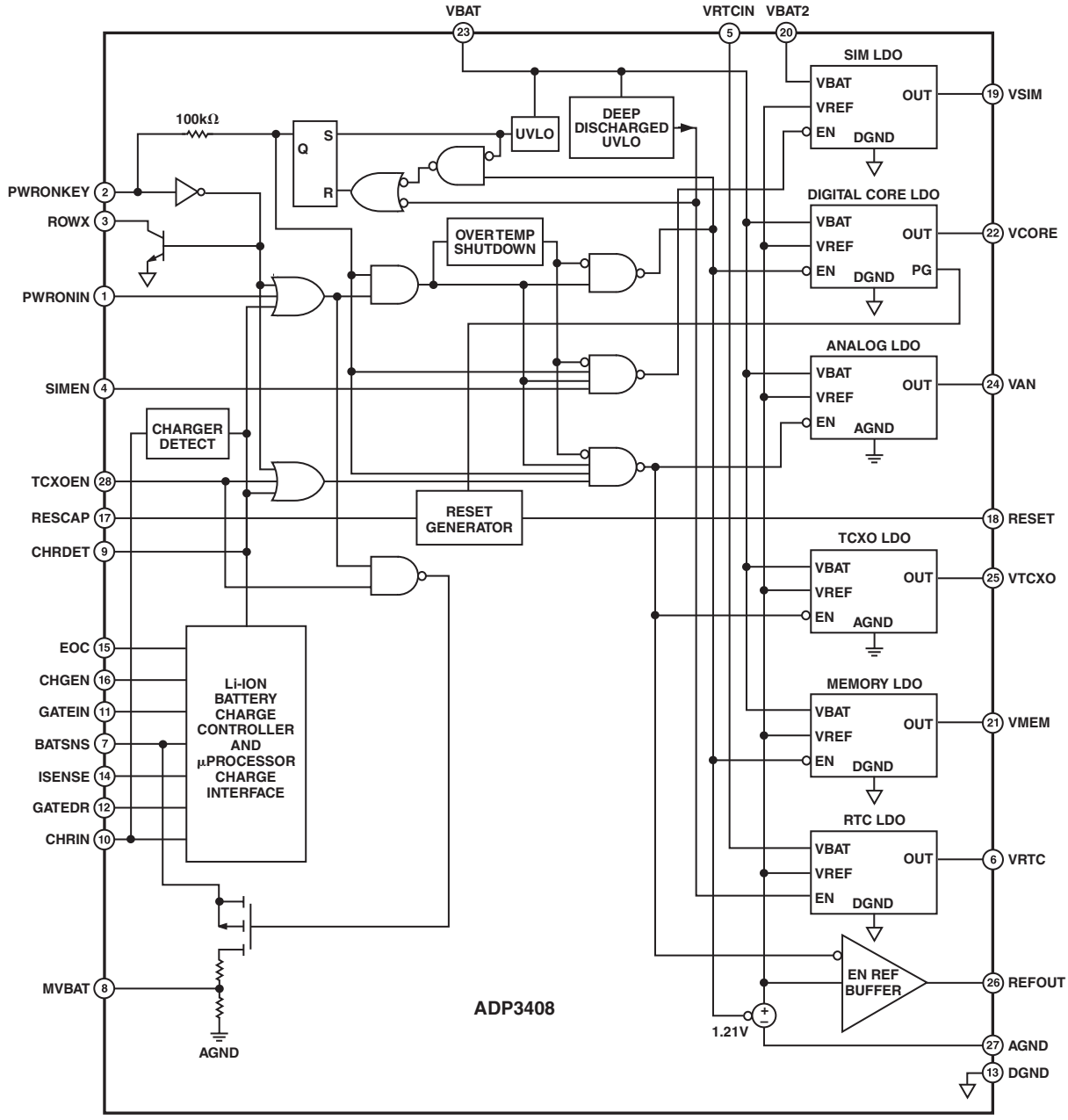


Figure 1. Functional Block Diagram (TSSOP Option Pin Number)

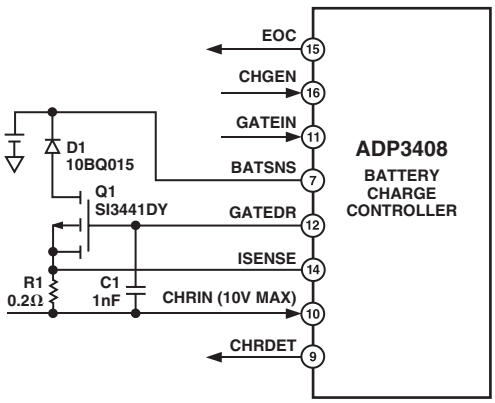


Figure 2. Battery Charger Typical Application (TSSOP Option Pin Number)

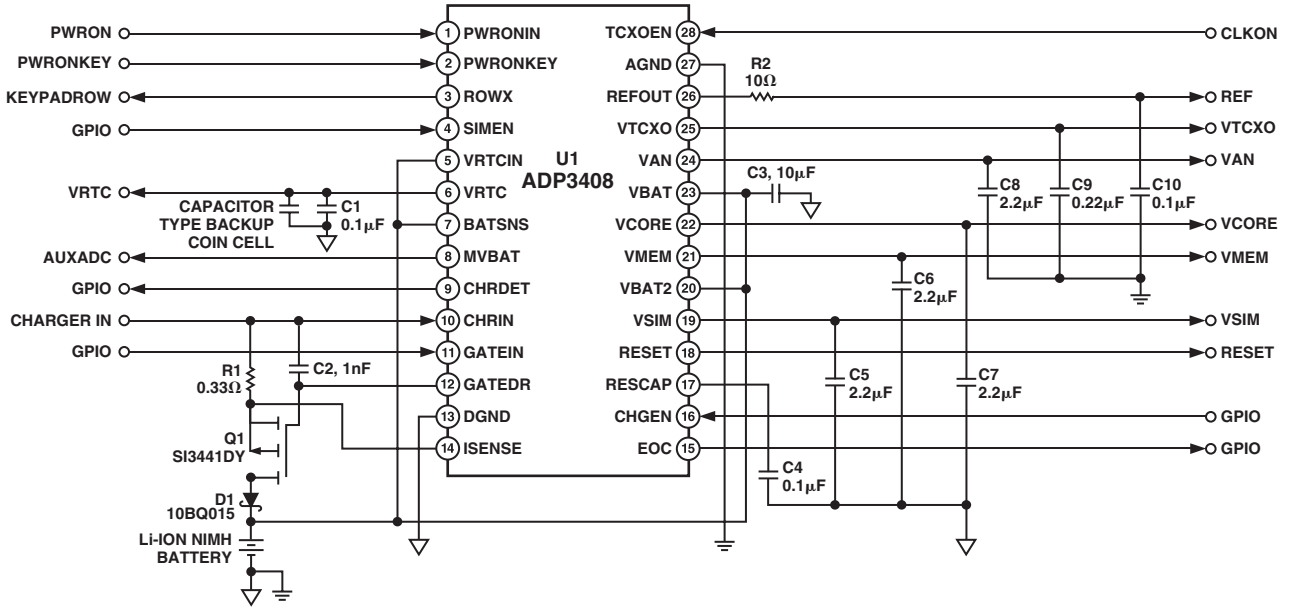


Figure 3a. Typical Application Circuit (TSSOP Option)

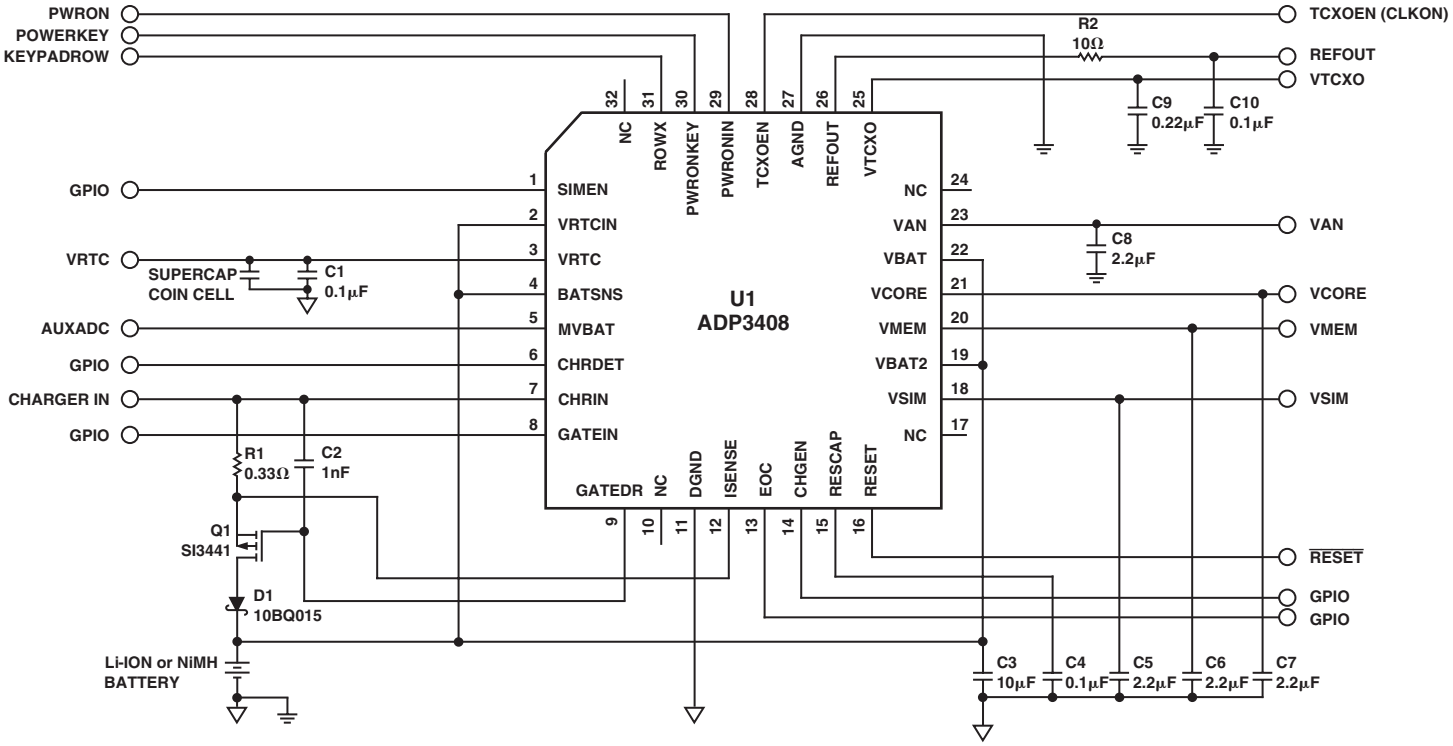


Figure 3b. Typical Application Circuit (LFCSP Option)

THEORY OF OPERATION

The ADP3408 is a power management chip optimized for use with GSM baseband chipsets in handset applications. Figure 1 shows a block diagram of the ADP3408.

The ADP3408 contains several blocks:

- Six Low Dropout Regulators (SIM, Core, Analog, Crystal Oscillator, Memory, Real-Time Clock)
- Reset Generator
- Buffered Precision Reference
- Lithium Ion Charge Controller and Processor Interface
- Power-On/-Off Logic
- Undervoltage Lockout
- Deep Discharge Lockout

These functions have traditionally been done either as a discrete implementation or as a custom ASIC design. The ADP3408 combines the benefits of both worlds by providing an integrated standard product in which every block is optimized to operate in a GSM environment while maintaining a cost competitive solution.

Figure 3 shows the external circuitry associated with the ADP3408. Only a minimal number of support components are required.

Input Voltage

The input voltage range of the ADP3408 is 3 V to 5.5 V and is optimized for a single Li-ion cell or three NiMH cells. The type of battery, the package type, and the Core LDO output voltage all affect the amount of power that the ADP3408 needs to dissipate. The thermal impedance of the TSSOP package is 68°C/W for four-layer boards. The thermal impedance of the CSP package is 32°C/W for four-layer boards.

The end of charge voltage for high capacity NiMH cells can be as high as 5.5 V. This results in a worst-case power dissipation for the ADP3408-1.8 as high as 1.07 W for NiMH cells. The power dissipation for the ADP3408-2.5 is just slightly lower at 1 W.

A fully charged Li-ion battery is 4.25 V, where the ADP3408-2.5 can dissipate a maximum power of 0.56 W in either package. However, the ADP3408-1.8 can have a maximum dissipation of 0.64 W, so only the CSP package can handle the power dissipation at 85°C.

However, high battery voltages normally occur only when the battery is being charged and the handset is not in conversation mode. In this mode, there is a relatively light load on the LDOs. The worst-case power dissipation should be calculated based on the actual load currents and voltages used.

Figure 4a shows the maximum power dissipation as a function of the input voltage. Figure 4b shows the maximum allowable power dissipation as a function of ambient temperature.

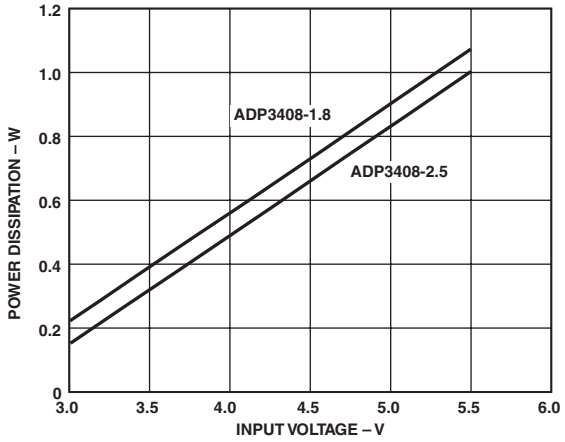


Figure 4a. Power Dissipation vs. Input Voltage

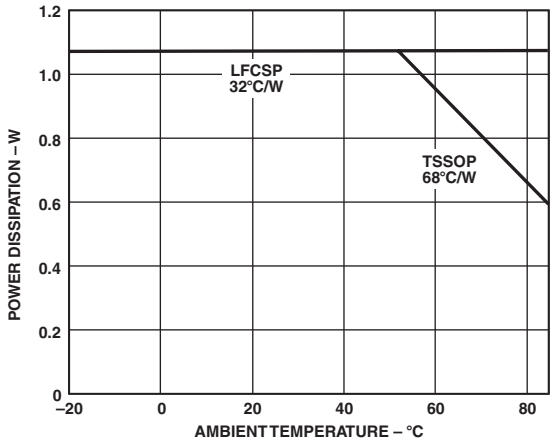


Figure 4b. Allowable Package Power Dissipation vs. Temperature

Low Dropout Regulators (LDOs)

The ADP3408 high performance LDOs are optimized for their given functions by balancing quiescent current, dropout voltage, regulation, ripple rejection, and output noise. 2.2 µF tantalum or MLCC ceramic capacitors are recommended for use with the core, memory, SIM, and analog LDOs. A 0.22 µF capacitor is recommended for the TCXO LDO.

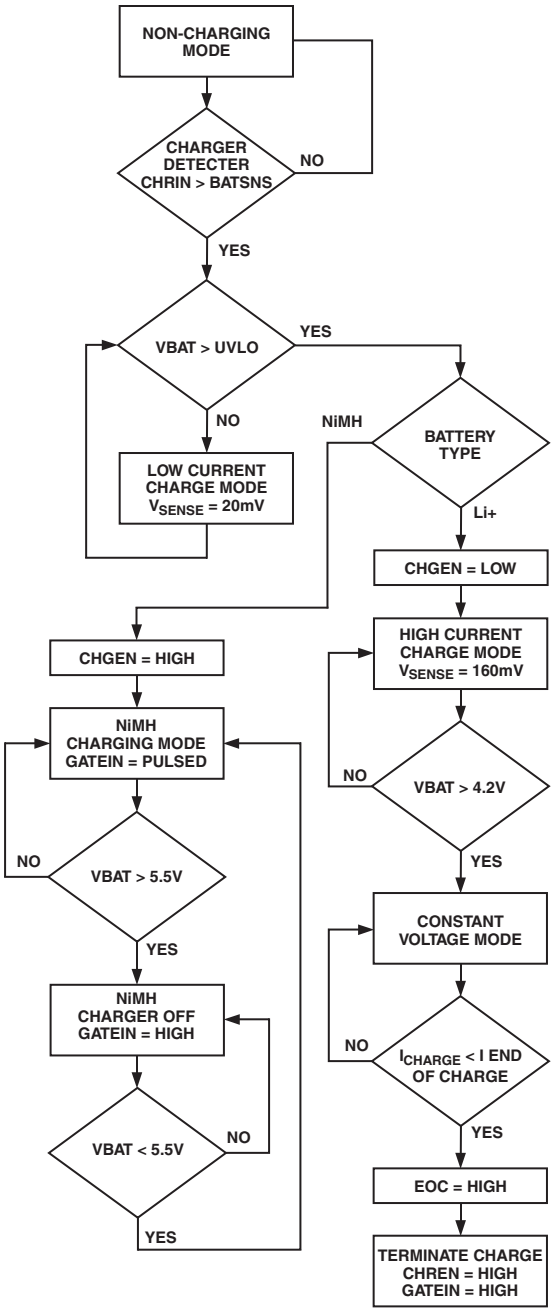


Figure 5. Battery Charger Flow Chart

Digital Core LDO (VCORE)
The digital core LDO supplies the baseband circuitry in the handset (baseband processor and baseband converter). The LDO has been optimized for very low quiescent current at light loads, as this LDO is on at all times.

Memory LDO (VMEM)
The memory LDO supplies the peripheral subsystems of the baseband processor including GPIO, display, and SIM interfaces as well as memory. The LDO has also been optimized for low quiescent current and will power up at the same time as the core LDO.

Analog LDO (VAN)
This LDO has the same features as the core LDO. It has furthermore been optimized for good low frequency ripple rejection for use with the baseband converter sections in order to reject the ripple coming from the RF power amplifier. VAN is rated to a 130 mA load, which is sufficient to supply the complete analog section of the baseband converter, such as the AD652l.

TCXO LDO (VTCXO)
The TCXO LDO is intended as a supply for a temperature-compensated crystal oscillator, which needs its own ultralow noise supply. VTCXO is rated for 5 mA of output current and is turned on along with the analog LDO when TCXOEN is asserted. Note that for the ADP3408-2.5, the TCXO output has been optimized for the AD6524 (Othello), while the ADP3408-1.8 has been optimized for the AD6534 (Othello One).

RTC LDO (VRTC)
The RTC LDO charges up a capacitor-type backup coin cell to run the Real-Time Clock module. It has been designed to charge electric double layer capacitors such as the PAS621 from Kanebo. The PAS621 has a small physical size (6.8 mm diameter) and a nominal capacity of 0.3 F, giving many hours of backup time.

The ADP3408 supplies current both for charging the coin cell and for the RTC module. In addition, it features a very low quiescent current since this LDO is running all the time, even when the handset is switched off. It also has reverse current protection with low leakage, which is needed when the main battery is removed and the coin cell supplies the RTC module.

SIM LDO (VSIM)
The SIM LDO generates the voltage needed for 3 V SIMs. It is rated for 20 mA of supply current and can be controlled completely independently of the other LDOs.

Reference Output (REFOUT)
The reference output is a low noise, high precision reference with a guaranteed accuracy of 1.5% over temperature. The reference can be used with the baseband converter. Note that the reference in the AD6521 has an initial accuracy of 10%, but can be calibrated to within 1%.

Power ON/OFF
The ADP3408 handles all issues regarding the powering ON and OFF of the handset. It is possible to turn on the ADP3408 in three different ways:

- Pulling the PWRONKEY Low
- Pulling PWRONIN High
- CHRIN exceeds CHRDET Threshold

Pulling the PWRONKEY low is the normal way of turning on the handset. This will turn on all the LDOs , except the SIM LDO, as long as the PWRONKEY is held low. When the VCORE LDO comes into regulation, the RESET timer is started. After timing out, the RESET pin goes high, allowing the baseband processor to start up. With the baseband processor running, it can poll the ROWX pin of the ADP3408 to determine if the PWRONKEY has been depressed and pull PWRONIN high. Once the PWRONIN is taken high, the PWRONKEY can be released. Note that by monitoring the ROWX pin, the baseband processor can detect a second PWRONKEY press and turn the LDOs off in an orderly manner. In this way, the PWRONKEY can be used for ON/OFF control.

Pulling the PWRONIN pin high is how the alarm in the Real-Time Clock module will turn the handset on. Asserting PWRONIN will turn on the core and memory LDOs, starting up the baseband processor.

Applying an external charger can also turn on the handset. This will turn on all the LDOs, except the SIM LDO, again starting up the baseband processor. Note that if the battery voltage is below the undervoltage lockout threshold, applying the adapter will not start up the LDOs.

Deep Discharge Lockout (DDLO)
The DDLO block in the ADP3408 has two functions:

- To shut off the VRTC LDO in the event that the main battery discharges to below the RTC LDO's output voltage. This will force the Real-Time Clock to run off the backup coin cell or double layer capacitor.
- To shut down the handset in the event that the software fails to turn off the phone when the battery drops below 2.9 V to 3.0 V. The DDLO will shut down the handset when the battery falls below 2.4 V to prevent further discharge and damage to the cells.

Undervoltage Lockout (UVLO)
The UVLO function in the ADP3408 prevents startup when the initial voltage of the battery is below the 3.2 V threshold. If the battery voltage is this low with no load, there is insufficient capacity left to run the handset. When the battery voltage is greater than 3.2 V, for example, when inserting a fresh battery, the UVLO comparator trips and the threshold is reduced to 3.0 V. This allows the handset to start normally until the battery decays to below 3.0 V. Note that the DDLO has enabled the RTC LDO under this condition.

Once the system is started and the core and memory LDOs are up and running, the UVLO function is disabled. The ADP3408 is then allowed to run until the battery voltage reaches the DDLO threshold, typically 2.4 V. Normally, the battery voltage is monitored by the baseband processor and usually shuts off the phone at around 3.0 V.

If the handset is off, and the battery voltage drops below 3.0 V, the UVLO circuit disables startup and puts the ADP3408 into UVLO shutdown mode. In this mode the ADP3408 draws very low quiescent current, typically 30 μA. The RTC LDO is still running until the DDLO disables it. In this mode the ADP3408 draws 5 μA of quiescent current. NiMH batteries can reverse polarity if the three-cell battery voltage drops below 3.0 V, which will degrade the batteries' performance. Lithium ion batteries will lose their capacity if repeatedly overdischarged, so minimizing the quiescent currents helps prevent battery damage.

RESET
The ADP3408 contains a reset circuit that is active at both power-up and power-down. The RESET pin is held low at initial power-up. An internal power good signal is generated by the core LDO when its output is up, which starts the reset delay timer. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.2\frac{ms}{nF} \times C_{RESCAP} \quad (1)$$

At power-off, RESET will be kept low to prevent any baseband processor starts.

Overtemperature Protection
The maximum die temperature for the ADP3408 is 125°C. If the die temperature exceeds 160°C, the ADP3408 will disable all the LDOs except the RTC LDO. The LDOs will not be re-enabled before the die temperature is below 125°C, regardless of the state of PWRONKEY, PWRONIN, and CHRDET. This ensures that the handset will always power-off before the ADP3408 exceeds its absolute maximum thermal ratings.

Battery Charging
The ADP3408 battery charger can be used with lithium ion (Li+) and nickel metal hydride (NiMH) batteries. The charger initialization, trickle charging, and Li+ charging are implemented in hardware. Battery type determination and NiMH charging must be implemented in software.

The charger block works in three different modes:

- Low Current (Trickle) Charging
- Lithium Ion Charging
- Nickel Metal Hydride Charging

Charge Detection
The ADP3408 charger block has a detection circuit that determines if an adapter has been applied to the CHRIN pin. If the adapter voltage exceeds the battery voltage by 90 mV, the CHRDET output will go high. If the adapter is then removed and the voltage at the CHRIN pin drops to only 45 mV above the BATSNS pin, CHRDET goes low.

Trickle Charging
When the battery voltage is below the UVLO threshold, the charge current is set to the low current limit, or about 10% of the full charge current. The low current limit is determined by the voltage developed across the current sense resistor. Therefore, the trickle charge current can be calculated by:

$$I_{CHR(TRICKLE)} = \frac{20\ mV}{R_{SENSE}} \quad (2)$$

Trickle charging is performed for deeply discharged batteries to prevent undue stress on either the battery or the charger. Trickle charging will continue until the battery voltage exceeds the UVLO threshold.

Once the UVLO threshold has been exceeded, the charger will switch to the default charge mode, the LDOs will start up, and the baseband processor will start to run. The processor must then poll the battery to determine which chemistry is present and set the charger to the proper mode.

Lithium Ion Charging
For lithium ion charging, the CHGEN input must be low. This allows the ADP3408 to continue charging the battery at the full current. The full charge current can be calculated by using:

$$I_{CHR(FULL)} = \frac{160\ mV}{R_{SENSE}} \quad (3)$$

If the voltage at BATSNS is below the charger's output voltage of 4.2 V, the battery will continue to charge in the constant current mode. If the battery has reached the final charge voltage, a constant voltage is applied to the battery until the charge current has reduced to the charge termination threshold. The charge termination threshold is determined by the voltage across the sense resistor. If the battery voltage is above 4.0 V and the voltage across the sense resistor has dropped to 14 mV, an End-of-Charge signal is generated and the EOC output goes high. See Figure 6.

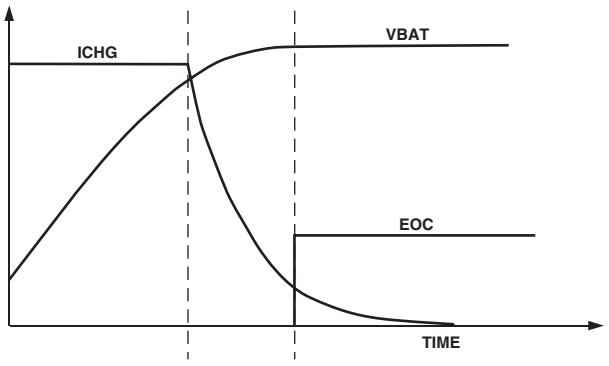


Figure 6. End of Charge

The baseband processor can either let the charger continue to charge the battery for an additional amount of time or terminate the charging. To terminate the charging, the processor must pull the GATEIN and CHGEN pins high.

NiMH Charging

For NiMH charging, the processor must pull the CHGEN pin high. This disables the internal Li+ mode control of the gate drive pin. The gate drive must now be controlled by the baseband processor. By pulling GATEIN high, the GATEDR pin is driven high, turning the PMOS off. By pulling the GATEIN pin low, the GATEDR pin is driven low, and the PMOS is turned on. So, by pulsing the GATEIN input, the processor can charge a NiMH battery. Note that when charging NiMH cells, a current-limited adapter is required.

During the PMOS off periods, the battery voltage needs to be monitored through the MVBAT pin. The battery voltage is continually polled until the final battery voltage is reached, at which time the charge can either be terminated or the frequency of the pulsing reduced. An alternative method of determining the end of charge is to monitor the temperature of the cells and terminate the charging when a rapid rise in temperature is detected.

Battery Voltage Monitoring

The battery voltage can be monitored at MVBAT during charging and discharging to determine the condition of the battery. An internal resistor divider can be connected to BATSNS when both the digital and analog baseband sections are powered up. To enable MVBAT, both PWRONIN and TCXOEN must be high.

The ratio of the voltage divider is selected so that the 2.4 V maximum input of the AD6521's auxiliary ADC will correspond with the maximum battery voltage of 5.5 V. The divider will be disconnected from the battery when the baseband sections are powered down.

APPLICATION INFORMATION

Input Capacitor Selection

For the input (VBAT, VBAT2, and VRTCIN) of the ADP3408, a local bypass capacitor is recommended. Use a 10 µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size, but may not be cost effective. A lower cost alternative may be to use a 10 µF tantalum capacitor with a small (1 µF to 2 µF) ceramic in parallel.

Separate inputs for the SIM LDO and the RTC LDO are supplied for additional bypassing or filtering. The SIM LDO has VBAT2 as its input and the RTC LDO has VRTCIN.

LDO Capacitor Selection

The performance of any LDO is a function of the output capacitor. The core, memory, SIM, and analog LDOs require a 2.2 µF capacitor, and the TCXO LDO requires a 0.22 µF capacitor. Larger values may be used, but the overshoot at startup will increase slightly. If a larger output capacitor is desired, be sure to check that the overshoot and settling time are acceptable for the application.

All the LDOs are stable with a wide range of capacitor types and ESR (anyCAP® technology). The ADP3408 is stable with extremely low ESR capacitors (ESR ~ 0), such as Multilayer Ceramic Capacitors (MLCC), but care should be taken in their selection. Note that the capacitance of some capacitor types show wide variations over temperature or with dc voltage. A good quality dielectric capacitor, X7R or better, is recommended.

The RTC LDO can have a rechargeable coin cell or an electric double-layer capacitor as a load, but an additional 0.1 µF ceramic capacitor is recommended for stability and best performance.

RESET Capacitor Selection

RESET is held low at power-up. An internal power good signal starts the reset delay when the core LDO is up. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.2\frac{ms}{nF} \times C_{RESCAP} \quad (4)$$

A 100 nF capacitor will produce a 120 ms reset delay. The current capability of RESET is minimal (a few hundred nA) when VCORE is off to minimize power consumption. When VCORE is on, RESET is capable of driving 500 µA.

Setting the Charge Current

The ADP3408 is capable of charging both lithium ion and NiMH batteries. For NiMH batteries, the charge current is limited by the adapter. For lithium ion batteries, the charge current is programmed by selecting the sense resistor, R1.

The lithium ion charge current is calculated using:

$$I_{CHR} = \frac{V_{SENSE}}{R1} = \frac{160\ mV}{R1} \quad (5)$$

Where V_{SENSE} is the high current limit threshold voltage. Or if the charge current is known, $R1$ can be found.

$$R1 = \frac{V_{SENSE}}{I_{CHR}} = \frac{160\ mV}{I_{CHR}} \quad (6)$$

Similarly, the trickle charge current and the end of charge current can be calculated:

$$I_{TRICKLE} = \frac{V_{SENSE}}{R1} = \frac{20\ mV}{R1}, I_{EOC} = \frac{14\ mV}{R1} \quad (7)$$

Example: Assume an 800 mAh capacity lithium ion battery and a 1C charge rate. $R1$ = 200 mΩ, $I_{TRICKLE}$ = 100 mA, and I_{EOC} = 70 mA.

anyCAP is a registered trademark of Analog Devices Inc.

Appropriate sense resistors are available from the following vendors:

Vishay Dale
IRC
Panasonic

Charger FET Selection

The type and size of the pass transistor is determined by the threshold voltage, input-output voltage differential, and charge current. The selected PMOS must satisfy the physical, electrical, and thermal design requirements.

To ensure proper operation, the minimum V_{GS} the ADP3408 can provide must be enough to turn on the FET. The available gate drive voltage can be estimated using the following:

$$V_{GS} = V_{ADAPTER(MIN)} - V_{GATEDR} - V_{SENSE} \quad (8)$$

where:

$V_{ADAPTER(MIN)}$ is the minimum adapter voltage, V_{GATEDR} is the gate drive "low" voltage, 0.5 V, and V_{SENSE} is the maximum high current limit threshold voltage.

The difference between the adapter voltage ($V_{ADAPTER}$) and the final battery voltage ($VBAT$) must exceed the voltage drop due to the blocking diode, the sense resistor, and the on resistance of the FET at maximum charge current, where:

$$V_{DS} = V_{ADAPTER(MIN)} - V_{DIODE} - V_{SENSE} - VBAT \quad (9)$$

The $R_{DS(ON)}$ of the FET can then be calculated.

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} \quad (10)$$

The thermal characteristics of the FET must be considered next. The worst-case dissipation can be determined using:

$$P_{DISS} = \left(V_{ADAPTER\,(MAX)} - V_{DIODE} - V_{SENSE} - UVLO\right) \times I_{CHR} \quad (11)$$

It should be noted that the adapter voltage can be either preregulated or nonregulated. In the preregulated case, the difference between the maximum and minimum adapter voltage is probably not significant. In the unregulated case, the adapter voltage can have a wide range specified. However, the maximum voltage specified is usually with no load applied. So, the worst-case power dissipation calculation will often lead to an over-specified pass device. In either case, it is best to determine the load characteristics of the adapter to optimize the charger design.

For example:

$V_{ADAPTER(MIN)}$ = 5.0 V
$V_{ADAPTER(MAX)}$ = 6.5 V
V_{DIODE} = 0.5 V at 800 mA
V_{SENSE} = 160 mV
V_{GATEDR} = 0.5 V
V_{GS} = 5 V – 0.5 V – 160 V = 4.34 V

Therefore, choose a low threshold voltage FET.

$$V_{DS} = V_{ADAPT(MIN)} - V_{DIODE} - V_{SENSE} - VBAT$$
$$= 5V - 0.5V - 0.160V - 4.2V = 140\,mV$$
$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} = \frac{140\,mV}{800\,mA} = 175\,m\Omega$$
$$P_{DISS} = \left(V_{ADAPT(MAX)} - V_{DIODE} - V_{SENSE} - UVLO\right) \times I_{CHR}$$
$$P_{DISS} = \left(6.5V - 0.5V - 0.160V - 3.2\right) \times 0.8\,A = 2.11\,W$$

Appropriate PMOS FETs are available from the following vendors:

Siliconix
IR
Fairchild

Charger Diode Selection

The diode, D1, shown in Figure 2, is used to prevent the battery from discharging through the PMOS's body diode into the charger's internal bias circuits. Choose a diode with a current rating high enough to handle the battery charging current and a voltage rating greater than VBAT. The blocking diode is required for both lithium and nickel battery types.

Printed Circuit Board Layout Considerations

Use the following general guidelines when designing printed circuit boards:

1. Connect the battery to the VBAT, VBAT2, and VRTCIN pins of the ADP3408. Locate the input capacitor as close to the pins as possible.
2. VAN and VTCXO capacitors should be returned to AGND.
3. VCORE, VMEM, and VSIM capacitors should be returned to DGND.
4. Split the ground connections. Use separate traces or planes for the analog, digital, and power grounds and tie them together at a single point, preferably close to the battery return.
5. Run a separate trace from the BATSNS pin to the battery to prevent voltage drop error in the MVBAT measurement.
6. Kelvin-connect the charger's sense resistor by running separate traces to the CHRIN and ISENSE pins. Make sure that the traces are terminated as close to the resistor's body as possible.
7. Use the best industry practice for thermal considerations during the layout of the ADP3408 and charger components. Careful use of copper area, weight, and multilayer construction all contribute to improved thermal performance.

LFCSP Layout Consideration

The CSP package has an exposed die paddle on the bottom that efficiently conducts heat to the PCB. To achieve the optimum performance from the CSP package, special consideration must be given to the layout of the PCB. Use the following layout guidelines for the CSP package:

1. The pad pattern is given in Figure 7. The pad dimension should be followed closely for reliable solder joints while maintaining reasonable clearances to prevent solder bridging.

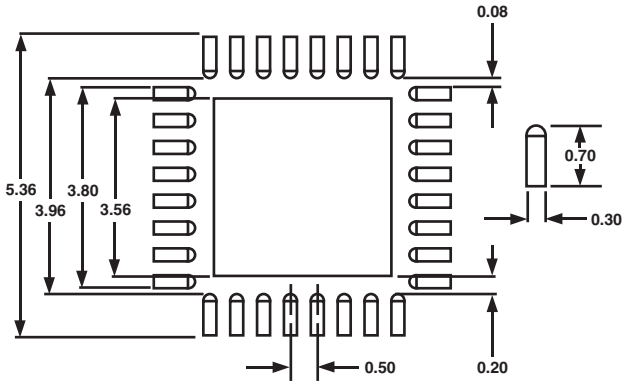


Figure 7. LFCSP Pad Pattern (Dimensions Shown in Millimeters)

2. The thermal pad of the CSP package provides a low thermal impedance path to the PCB. Therefore, the PCB must be properly designed to effectively conduct the heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. See Figure 8 for the recommended via pattern. Note that the via diameter is small. This is to prevent the solder from flowing through the via and leaving voids in the thermal pad solder joint.

   Note that the thermal pad is attached to the die substrate, so the thermal planes that the vias attach the package to must be electrically isolated or connected to VBAT. **Do not connect the thermal pad to ground.**

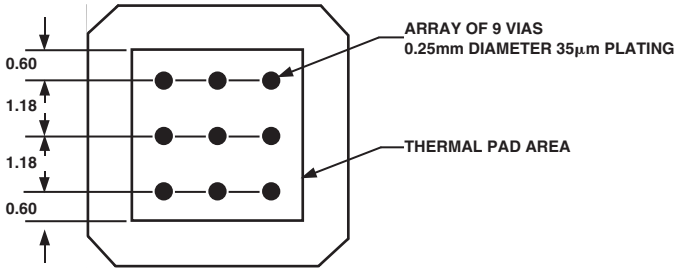


Figure 8. LFCSP via Pattern (Dimensions Shown in Millimeters)

3. The solder mask opening should be about 120 microns (4.7 mils) larger than the pad size resulting in minimum 60 microns (2.4 mils) clearance between the copper pad and solder mask.

4. The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm.

   The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the large size of the thermal pad, eliminating voids may not be possible. Also, if the solder paste coverage is too large, solder joint defects may occur. Therefore, it is recommended to use multiple small openings over a single big opening in designing the paste mask. The recommended paste mask pattern is given in Figure 9. This pattern will result in about 80% coverage, which should not degrade the thermal performance of the package significantly.

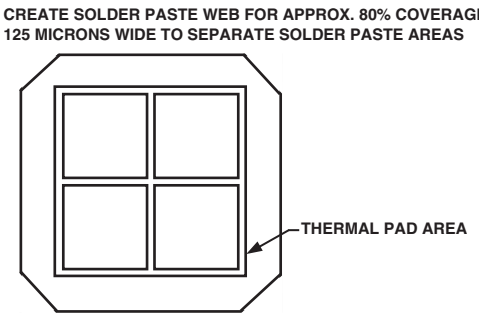


Figure 9. LFCSP Paste Mask Pattern

5. The recommended paste mask stencil thickness is 0.125 mm. A laser cut stainless steel stencil with trapezoidal walls should be used.

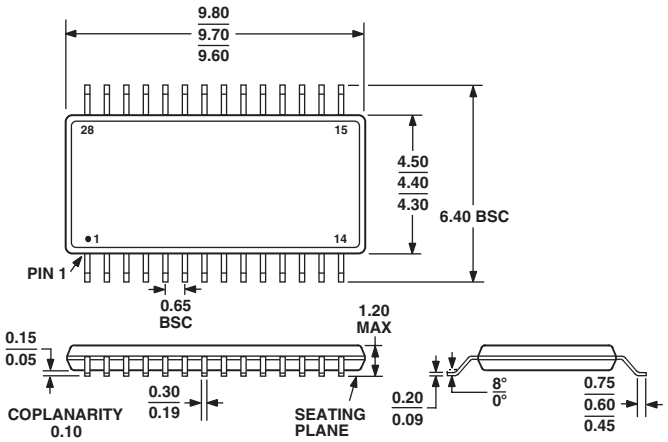
   A "No Clean," Type 3 solder paste should be used for mounting the LFCSP package. Also, a nitrogen purge during the reflow process is recommended.

6. The package manufacturer recommends that the reflow temperature should not exceed 220°C and the time above liquidus is less than 75 seconds. The preheat ramp should be 3°C/second or lower. The actual temperature profile depends on the board's density and must be determined by the assembly house as to what works best.

OUTLINE DIMENSIONS

28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)

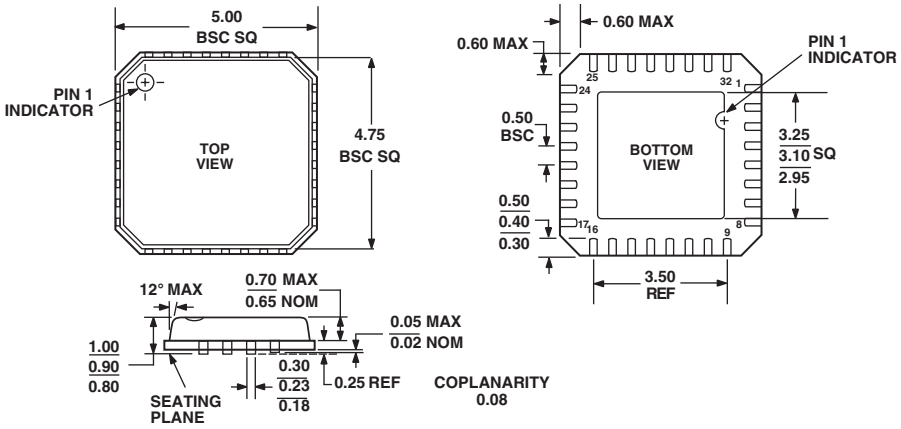
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AE

32-Lead Frame Chip Scale Package [LFCSP]
(CP-32)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Revision History

Location	Page
11/02—Data Sheet changed from REV. 0 to REV. A	
Changes to GENERAL DESCRIPTION	1
Note added to FUNCTIONAL BLOCK DIAGRAM	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	5
Changes to ORDERING GUIDE	5
Updated PIN CONFIGURATIONS added	6
Changes to PIN FUNCTION DESCRIPTIONS	6
Edits to Figures 1 and 2 captions	11
Edit to Figure 2	11
Edits to Figure 3 (changed to Figure 3a)	12
Figure 3b added	12
Figure 4 replaced with Figures 4a and 4b	13
Changes to Input Voltage section	13
Text added to TCXO LDO (VTCXO) section	14
Edits to RTC LDO (VRTC) section	14
Edits to Reference Output (REFOUT) section	14
Edits to Trickle Charging section	15
Edits to Equation 7	16
Edit to Settling the Charge Current section	16
Addition of LFCSP Layout Considerations section	18
New Figure 7	18
New Figure 8	18
New Figure 9	18
Add 32-Lead LFCSP Package Outline	19

C02623–0–12/02(A)

PRINTED IN U.S.A.