



2.5V CLOCK BUFFER

IDT2305Nzt

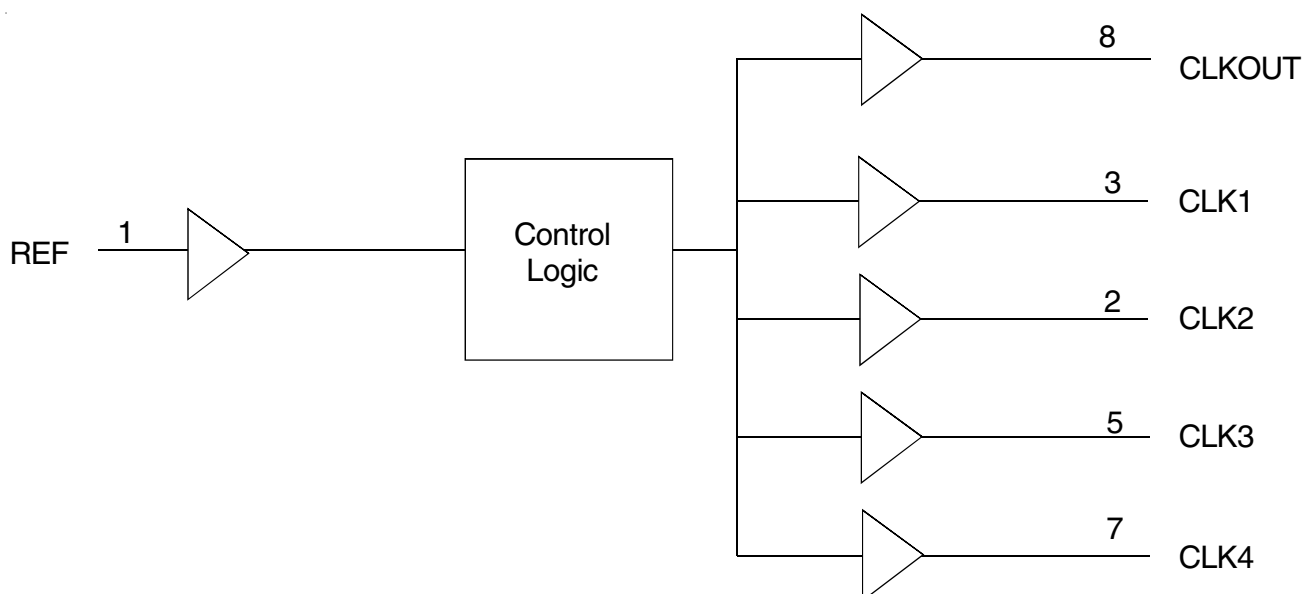
FEATURES:

- Clock Distribution
- 10MHz to 133MHz operating frequency
- Distributes one clock input to one bank of five outputs
- Output Skew < 250ps
- No external RC network required
- Operates at 2.5V V_{DD}
- Available in SOIC package

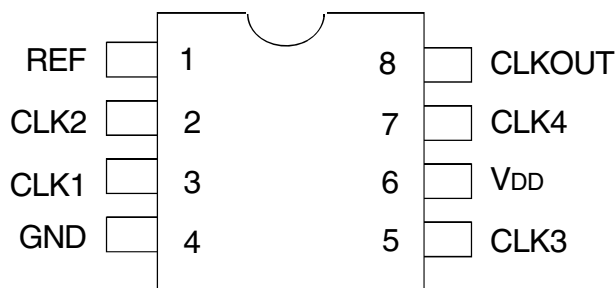
DESCRIPTION:

The IDT2305Nzt is a high-speed clock buffer, designed to address high-speed clock distribution applications. IDT2305Nzt accepts one reference input, and drives out five low skew clocks.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max.	Unit
V _{DD}	Supply Voltage Range	−0.5 to +4.6	V
V _I ⁽²⁾	Input Voltage Range (REF)	−0.5 to +5.5	V
V _I	Input Voltage Range (except REF)	−0.5 to V _{DD} +0.5	V
I _{IK} (V _I < 0)	Input Clamp Current	−50	mA
I _O (V _O = 0 to V _{DD})	Continuous Output Current	±50	mA
V _{DD} or GND	Continuous Current	±100	mA
T _A = 55°C (in still air) ⁽³⁾	Maximum Power Dissipation	0.7	W
T _{STG}	Storage Temperature Range	−65 to +150	°C
Operating Temperature	Commercial Temperature Range	0 to +70	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

PIN DESCRIPTION

Pin Name	Pin Number	Type	Functional Description
REF ⁽¹⁾	1	IN	Input reference clock, 3.3V tolerant input
CLK2 ⁽²⁾	2	OUT	Output clock
CLK1 ⁽²⁾	3	OUT	Output clock
GND	4	GND	Ground
CLK3 ⁽²⁾	5	OUT	Output clock
V _{DD}	6	PWR	2.5V Supply
CLK4 ⁽²⁾	7	OUT	Output clock
CLKOUT ⁽²⁾	8	OUT	Output clock

NOTES:

- Weak pull down.
- Weak pull down on all outputs.

OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply Voltage	2.3	2.7	V
T _A	Operating Temperature (Ambient Temperature)	0	+70	°C
C _L	Load Capacitance 10MHz - 133MHz	—	15	pF
C _{IN}	Input Capacitance	—	7	pF

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{IL}	Input LOW Voltage Level		—	0.7	V
V _{IH}	Input HIGH Voltage Level		1.7	—	V
I _{IL}	Input LOW Current	V _{IN} = 0V	—	50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}	—	100	μA
V _{OL}	Output LOW Voltage	Standard Drive, I _{OL} = 8mA	—	0.3	V
V _{OH}	Output HIGH Voltage	Standard Drive, I _{OH} = -8mA	2	—	V
I _{DD_PD}	Power Down Current	REF = 0MHz	—	12	μA
I _{DD}	Supply Current	Unloaded Outputs at 66.66MHz	—	32	mA

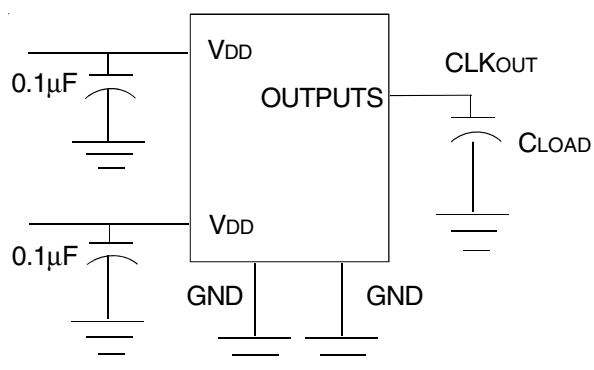
SWITCHING CHARACTERISTICS^(1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _i	Output Frequency	15pF Load	10	—	133	MHz
	Duty Cycle = t ₂ ÷ t ₁	Measured at V _{DD} /2, F _{OUT} = 66.66MHz	40	50	60	%
t ₃	Rise Time	Measured between 0.7V and 1.7V	—	—	2.5	ns
t ₄	Fall Time	Measured between 0.7V and 1.7V	—	—	2.5	ns
t ₅	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t ₆	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2	—	0	8.7	ns
t ₇	Device-to-Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices	—	0	700	ps

NOTES:

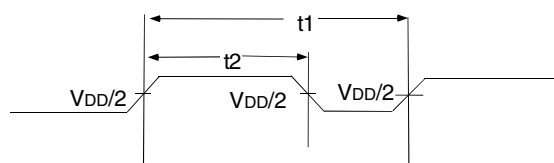
1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

TEST CIRCUIT

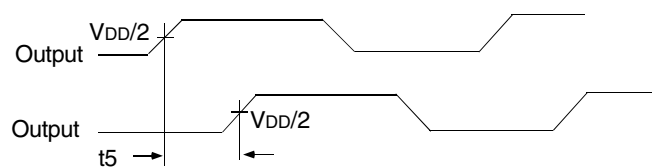


Test Circuit for All Parameters

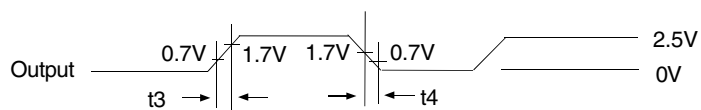
SWITCHING WAVEFORMS



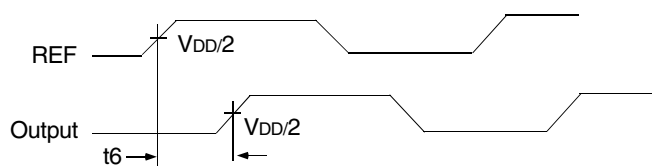
Duty Cycle Timing



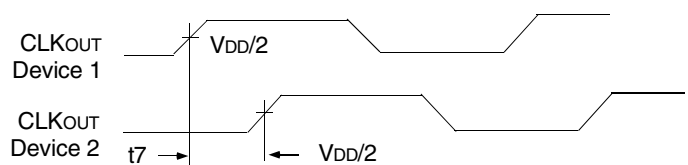
Output to Output Skew



All Outputs Rise/Fall Time



Input to Output Propagation Delay



Device to Device Skew

ORDERING INFORMATION

IDT	XXXXX	XX	X		
Device Type	Package	Process			
			Blank		Commercial (0°C to +70°C)
			DC DCG		Small Outline SOIC - Green
			2305NZT-1		2.5V Clock Buffer



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