TLS202B1

Fixed Linear Voltage Post Regulator

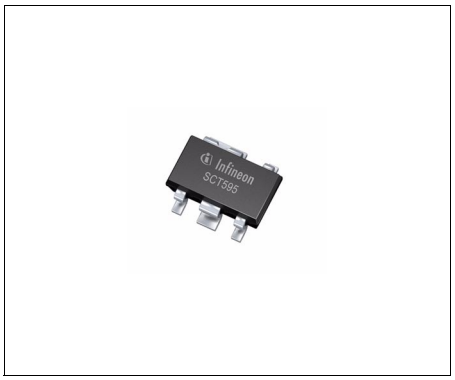
TLS202B1MBV33

Data Sheet

Rev. 1.0, 2015-06-23

Automotive Power

1 Overview



PG-SCT595

Features

- Output Voltage: 3.3 V
- Output Voltage Accuracy of ±3 %
- Output Currents up to 150 mA
- Extended Input Voltage Operating Range of 2.7 V to 18 V
- Enable Functionality
- Low Dropout Voltage: typ. 290mV
- Very Low Current Consumption: typ. 50 µA
- Very Low Shutdown Current: typ. 0.01 µA
- Very High PSRR: typ. 63dB at 10 kHz
- Output Current Limitation
- Short Circuit protected
- Overtemperature Shutdown
- Wide Temperature Range From -40 °C up to 150 °C
- Suitable for Use in Automotive Electronics as Post Regulator
- Green Product (RoHS compliant)
- AEC Qualified

Functional Description

The TLS202B1 is a monolithic integrated fixed linear voltage post regulator for load currents up to 150 mA. The IC regulates an input voltage V_I up to 18 V to a fixed output voltage of 1.2 V to 5.25 V with a precision of ±3 %. The TLS202B1 is especially designed for applications requiring very low standby currents, e.g. with a permanent connection to the preregulators like DCDC converters. The regulator is not designed to operate with a direct connection to the battery. The component can be enabled/disabled via the Enable input. The device is available in a very small surface mounted PG-SCT595 package. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLS202B1 can be also used in all other applications requiring a stabilized 1.2 V to 5.25 V voltage.

Choosing External Components

The input capacitor C_I is recommended for compensating line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **“Functional Range” on Page 6** within the whole operating temperature range.

Type	Package	Marking
TLS202B1MBV33	PG-SCT595	21

2 Block Diagram

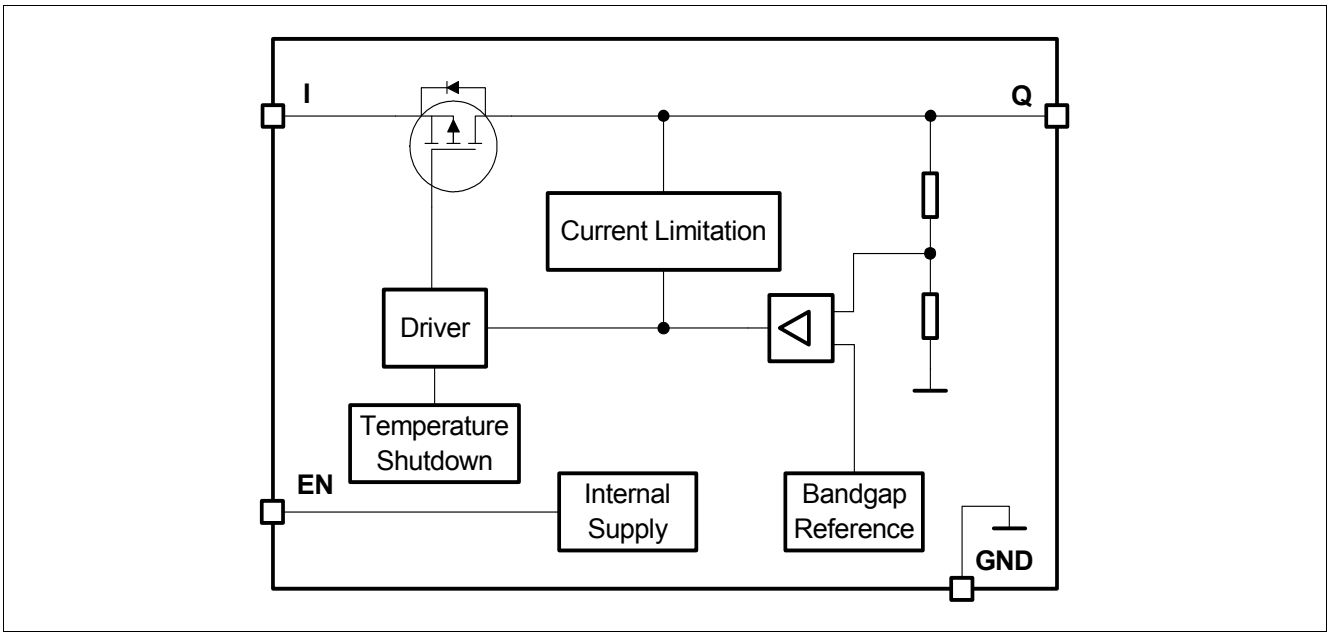


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-SCT595

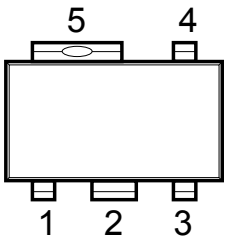


Figure 2 Pin Configuration Package PG-SCT595-5

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	I	**Input.** **IC supply.** For compensating line influences, a capacitor of 220 nF close to the IC pin is recommended.
2	GND	**Ground Reference.** Internally connected to Pin 5. Connect to heatsink area. For thermal reasons both ground Pins 2 and 5 have to be soldered.
3	Q	**Output.** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the **“Functional Range” on Page 6**”.
4	EN	**Enable.** A low signal disables the IC. A high signal switches it on. Connect to the input I, if the enable functionality is not required.
5	GND	**Ground Reference.** Internally connected to Pin 2. Connect to heatsink area. For thermal reasons both ground Pins 2 and 5 have to be soldered.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings [1] T_j = -40 °C to +150 °C; all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	20	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	5.5	V	–	P_4.1.2
Enable EN							
Voltage	V_{EN}	-0.3	–	20	V	–	P_4.1.3
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD Susceptibility							
ESD Absorption	$V_{ESD,HBM}$	-4	–	4	kV	Human Body Model (HBM) [2]	P_4.1.6
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge Device Model (CDM) [3] at all pins	P_4.1.7

1) not subject to production test, specified by design

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	2.7		18	V	–	P_4.2.1
Output Capacitor Requirements for Stability	C_Q	1		–	µF	1)	P_4.2.2
Output Capacitor Requirements for Stability	$ESR(C_Q)$	–		10	Ω	2)	P_4.2.3
Junction temperature	T_j	-40		150	°C	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Ambient	R_{thJA}	–	81	–	K/W	2s2p board 1)	P_4.3.1
Junction to Ambient	R_{thJA}	–	217	–	K/W	Footprint only 2)	P_4.3.2
Junction to Ambient	R_{thJA}	–	117	–	K/W	300 mm^2 PCB heatsink area 2)	P_4.3.3
Junction to Ambient	R_{thJA}	–	103	–	K/W	600 mm^2 PCB heatsink area 2)	P_4.3.4
Junction to Soldering Point	R_{thJSP}	–	30	–	K/W	Pins 2, 5 fixed to T_A	P_4.3.5

1) Specified R_{thJA} value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array next to the package contacted to the first inner copper layer.

2) Package mounted on PCB FR4; 80 x 80 x 1.5 mm; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow. Not subject to production test; specified by design.

5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled as follows: It is divided by the resistor divider. This fraction is then compared to an internal reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the circuit design. To ensure stable operation, the requirements for output capacitance and equivalent series resistance ESR, given in **“Functional Range” on Page 6**, have to be maintained. For details see also the typical stability graph of ESR versus load current on **Page 10**. As the output capacitor also has to buffer load steps it should be sized according to the needs of the application.

An input capacitor C_I is recommended to compensate line influences. Connect the capacitors close to the terminals of the component.

In case the load current is above the specified limit, e.g. in case of a short circuit, the output current limitation limits the current. The output voltage is therefore decreasing at the same time.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC’s lifetime.

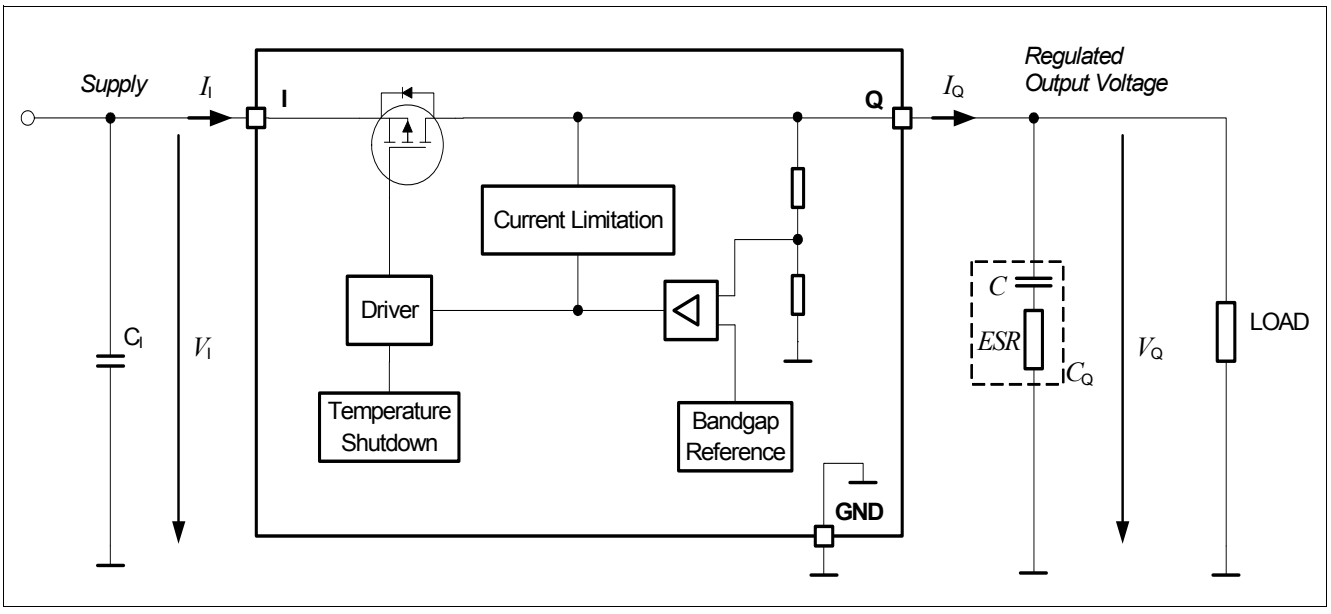


Figure 3 Block Diagram Voltage Regulator Circuit

5.2 Electrical Characteristics Voltage Regulator

Table 4 Electrical Characteristics V_I = 4.3 V; T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage	V_Q	3.2	3.3	3.4	V	I_Q = 10 mA ; T_j = 25 °C	P_5.2.1
Output Voltage	V_Q	3.17	3.3	3.43	V	I_Q = 10 mA	P_5.2.2
Dropout Voltage [1]	V_{dr}	–	290	570	mV	I_Q = 150 mA	P_5.2.3
Load Regulation	ΔV_Q	-80	-25	–	mV	I_Q = 1 mA to 150 mA	P_5.2.4
Line Regulation	ΔV_Q	–	1.88	37.6	mV	V_I = 4.3 V to 10 V ; I_Q = 1 mA	P_5.2.5
Output Current Limitation	I_Q	151	300	–	mA	0 V ≤ V_Q ≤ 3.0 V	P_5.2.6
Power Supply Ripple Rejection [2]	PSRR	–	63	–	dB	f_f = 10 kHz ; I_Q = 50 mA ; T_j = 25 °C ; V_{in} = 4.3 V ; ΔV_I = 1 V_{pp} ; C_{out} = 1 µF (Ceramic Capacitor)	P_5.2.7
Overtemperature Shutdown Threshold [2]	$T_{j,sd}$	151	170	190	°C	–	P_5.2.8

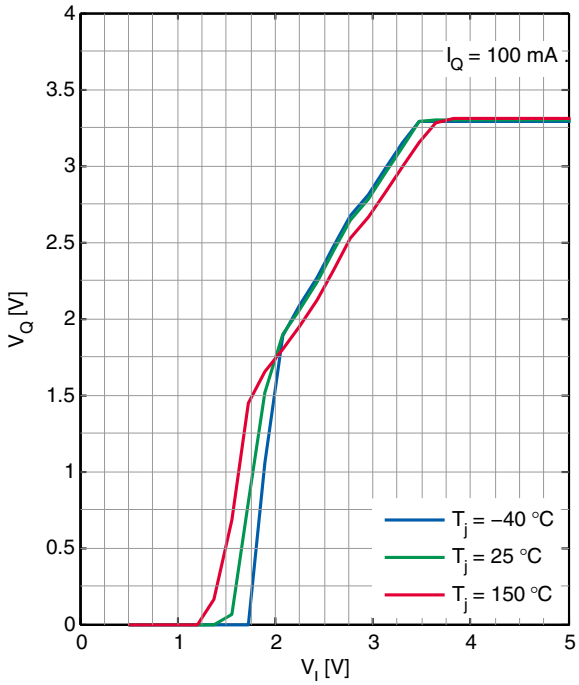
1) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at V_I = $V_{Q,nom}$ + 1 V, I_{Load} = 150mA.

2) Parameter is not subject to production test, specified by design

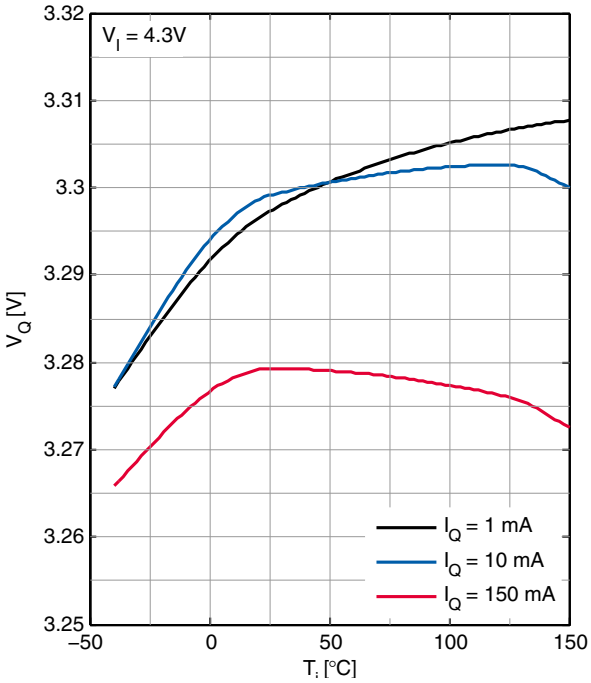
5.3 Typical Performance Characteristics Voltage Regulator

V_{EN} = 5 V (unless otherwise noted)

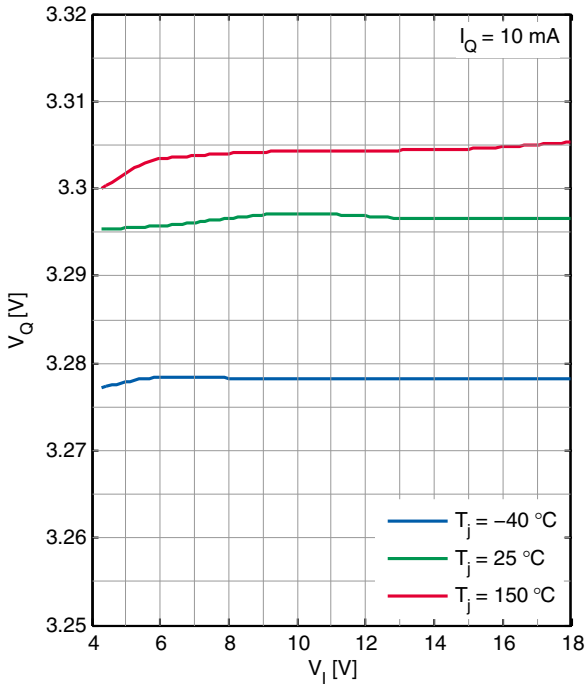
Output Voltage V_Q vs. Input Voltage V_I (TLS202B1MBV33)



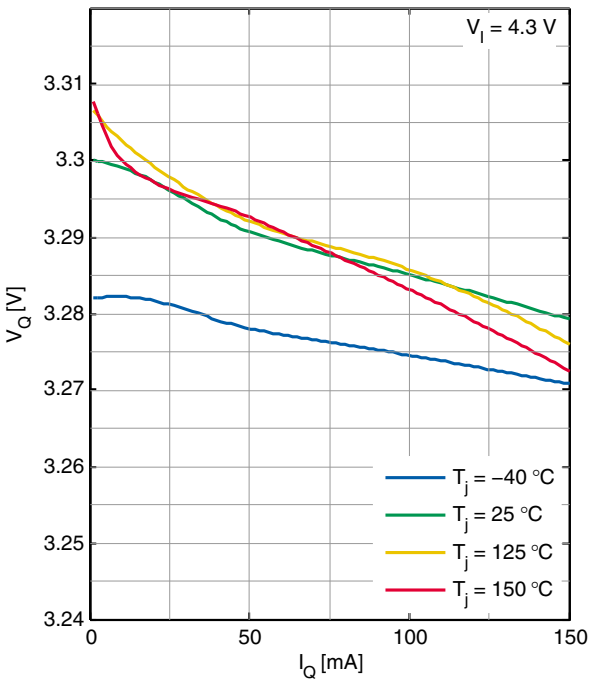
Output Voltage V_Q vs. Junction Temperature T_j (TLS202B1MBV33)



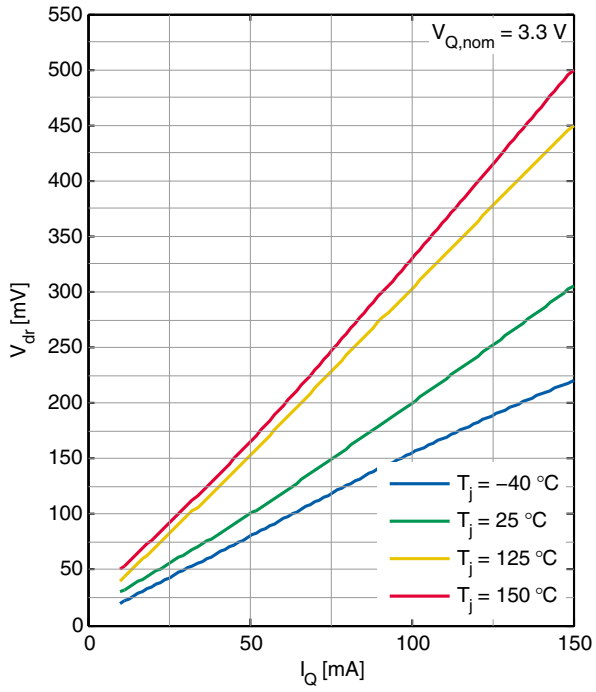
Line Regulation Output Voltage V_Q vs. Input Voltage V_I (TLS202B1MBV33)



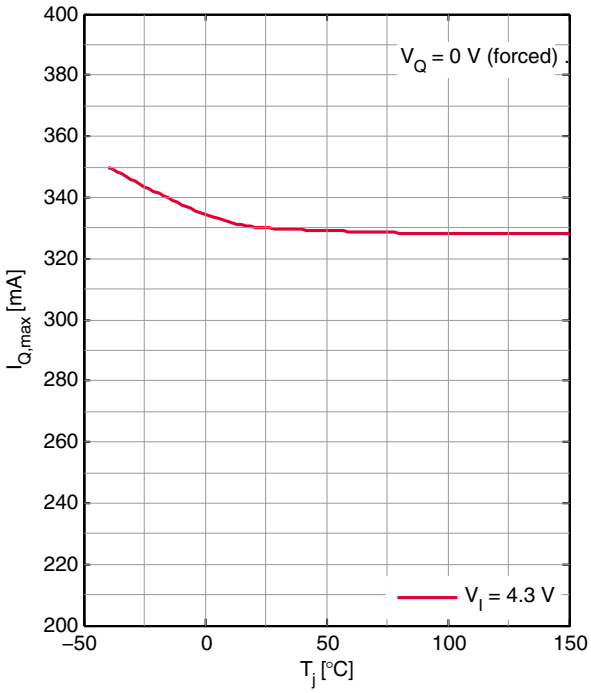
Load Regulation Output Voltage V_Q vs. Load Current I_Q (TLS202B1MBV33)



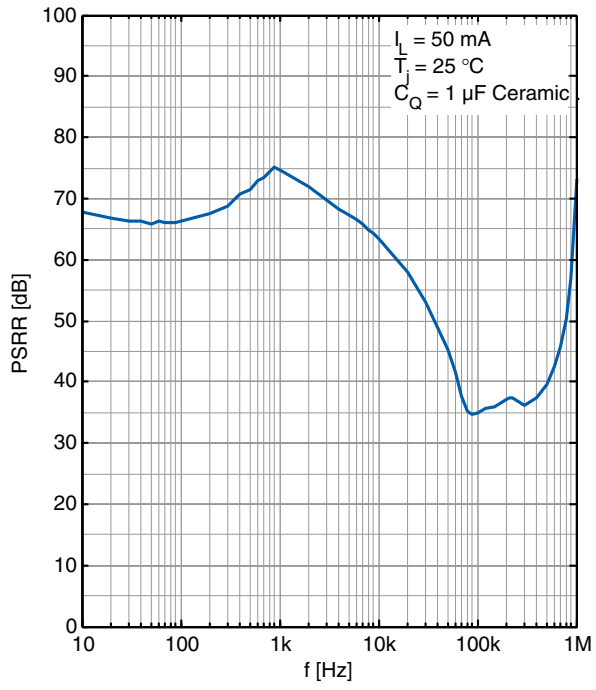
Dropout Voltage V_{dr} vs. Load Current I_Q (TLS202B1MBV33)



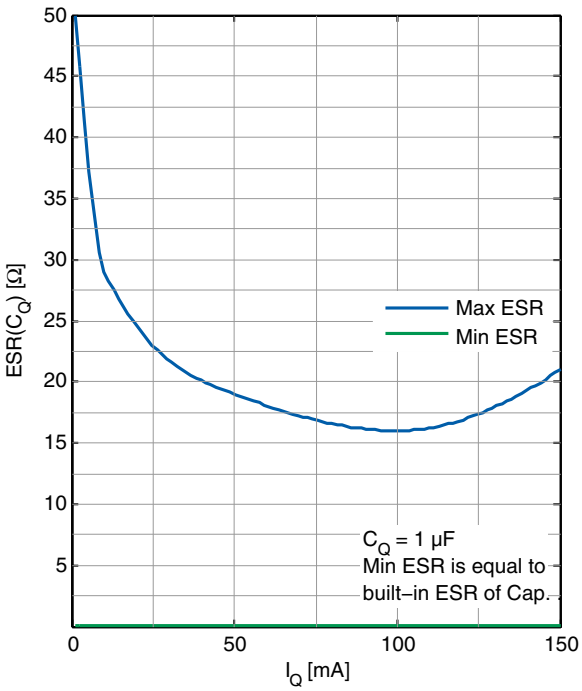
Qutput Current Limitation $I_{Q,max}$ vs. Junction Temperature T_j (TLS202B1MBV33)



PSRR vs. Frequency (TLS202B1MBV33)



Output Capacitor Series Resistance ESR(C_Q) vs. Output Current I_Q (TLS202B1MBV33)



6 Current Consumption

6.1 Description Current Consumption

The Current Consumption of the device is characterizing the current the device needs to operate. The Quiescent Current is describing the Current Consumption in a very low load condition (e.g. the supplied microcontroller is in sleep mode). The TLS202B1 has an Enable functionality to shutdown the device, in case it is not needed. During shutdown the device has a very low Current Consumption. The Current Consumption of the device can be determined by measuring the Current flowing out of the GND Pin and defined as the delta between I_I and (I_Q+I_{EN}).

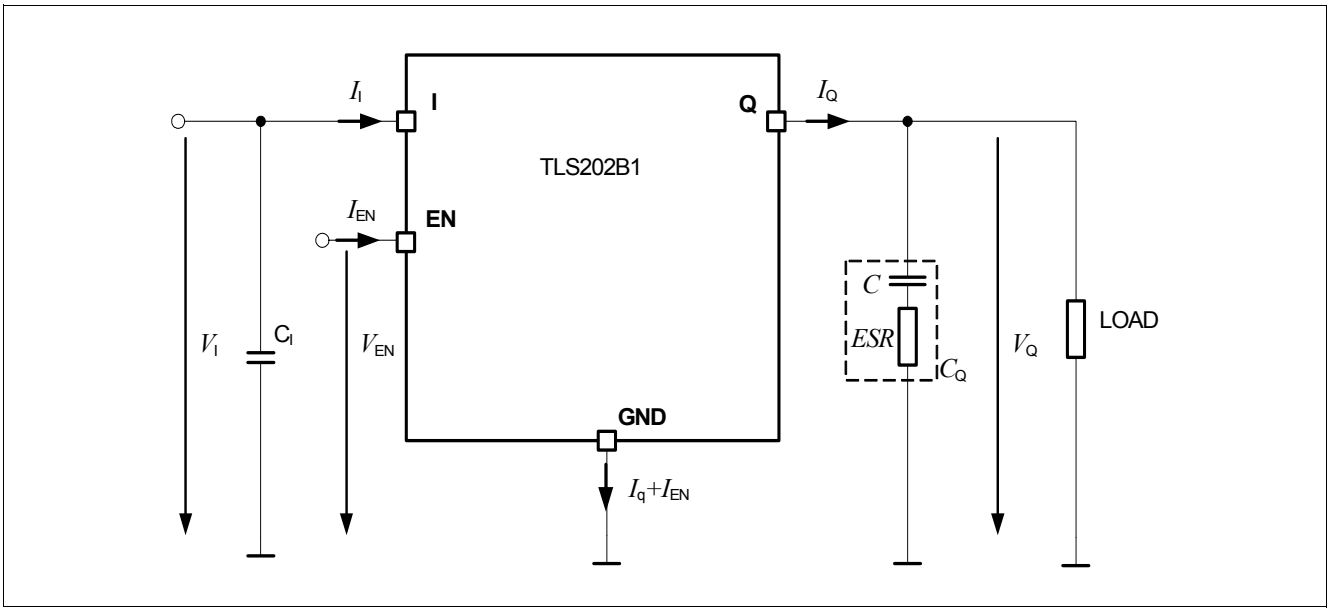


Figure 4 Parameter Definition Current Consumption

6.2 Electrical Characteristics Current Consumption

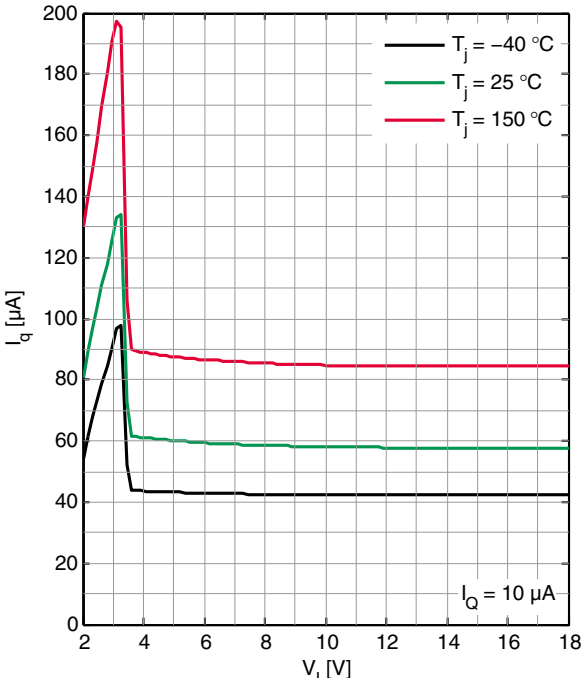
Table 5 Electrical Characteristics V_I = 4.3 V; T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent Current $I_q = I_I - I_Q$	I_q	–	50	75	µA	I_Q = 10 µA ; T_j = 25 °C	P_6.2.1
Quiescent Current $I_q = I_I - I_Q$	I_q	–	–	100	µA	I_Q = 10 µA ; T_j ≤ 125 °C	P_6.2.2
Current Consumption $I_q = I_I - I_Q$	I_q	–	150	200	µA	I_Q = 50 mA	P_6.2.3
Quiescent Current in Shutdown	$I_{q,off}$	–	0.01	1	µA	V_I = 6 V ; V_{EN} = 0 V ; T_j ≤ 125 °C ; V_Q = 0 V	P_6.2.4

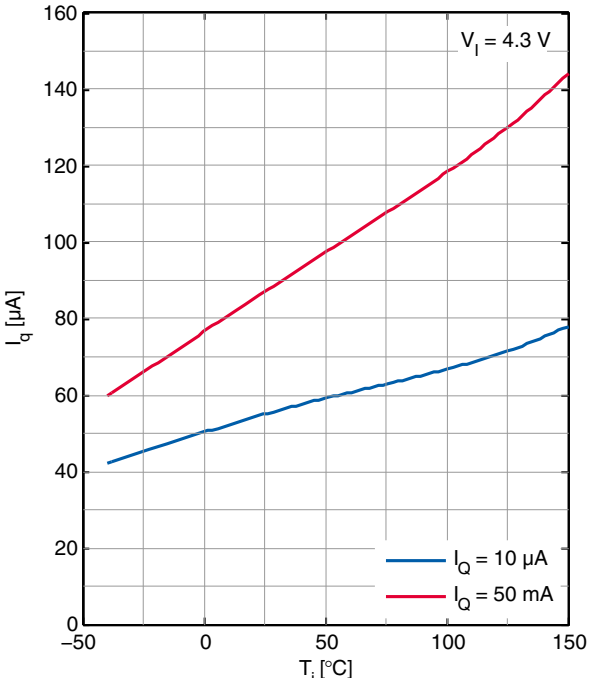
6.3 Typical Performance Characteristics Current Consumption

V_{EN} = 5 V (unless otherwise noted)

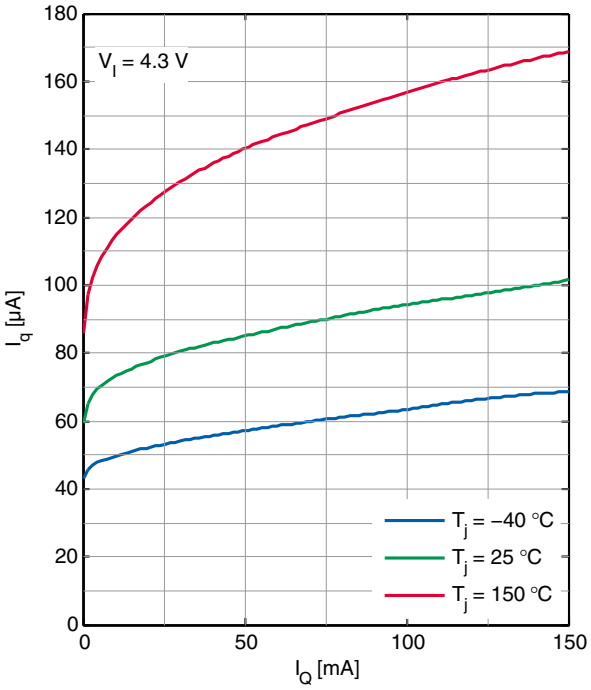
Quiescent Current I_q vs. Input Voltage V_I (TLS202B1MBV33)



Current Consumption I_q vs. Junction Temperature T_J (TLS202B1MBV33)



Current Consumption I_q vs. Load Current I_Q (TLS202B1MBV33)



7 Enable Function

7.1 Description Enable Function

The TLS202B1 can be turned on or turned off by the EN Input. The parameter V_{EN} is the voltage provided to the EN Pin as shown in **Figure 4 "Parameter Definition Current Consumption" on Page 11**.

With voltage levels lower than $V_{EN,Lo}$ applied to the EN Input the device will be turned off. During this state the device is in shutdown with a very low current consumption $I_{q,off}$.

By changing the voltage at the EN Input from $V_{EN,Hi}$ to $V_{EN,Lo}$ will trigger the start-up of the device. For voltages higher than $V_{EN,Hi}$ the device will regulate the output voltage to the nominal value as described in **Chapter 5 Voltage Regulator**.

7.2 Electrical Characteristics Enable Function

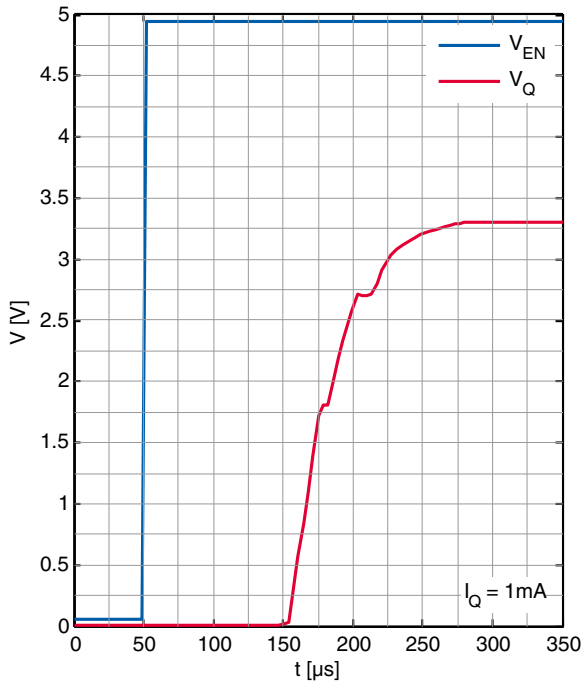
Table 6 Electrical Characteristics V_I = 4.3 V; T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable High Voltage Level	$V_{EN,Hi}$	2	–	–	V	$V_{Q,on}$ ≥ 3.135 V	P_7.2.1
Enable Low Voltage Level	$V_{EN,Lo}$	–	–	0.4	V	$V_{Q,off}$ ≤ 200 mV	P_7.2.2
Enable Pin Current [1]	I_{EN}	–	–	5	µA	V_{EN} = 5 V	P_7.2.3

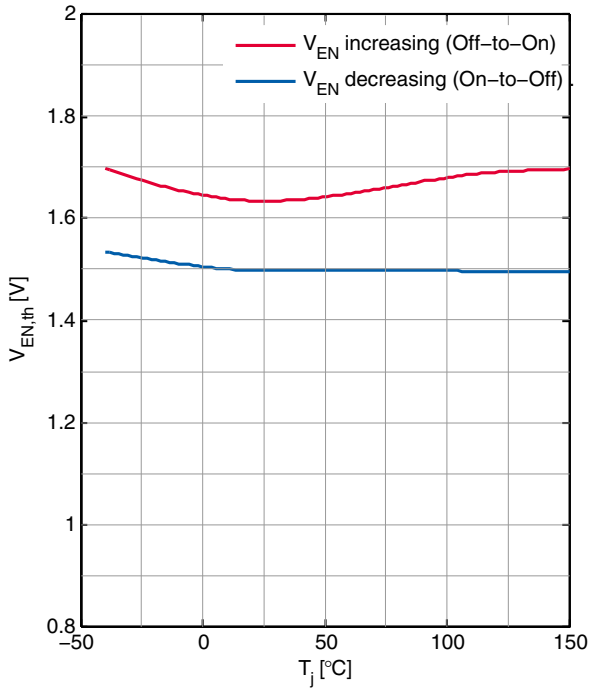
1) Enable pin current flows into the EN pin.

7.3 Typical Performance Characteristics Enable Function

Power Up Timing (TLS202B1MBV33)



Enable Thresholds V_{EN} vs. Junction Temperature T_j (TLS202B1MBV33)



8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

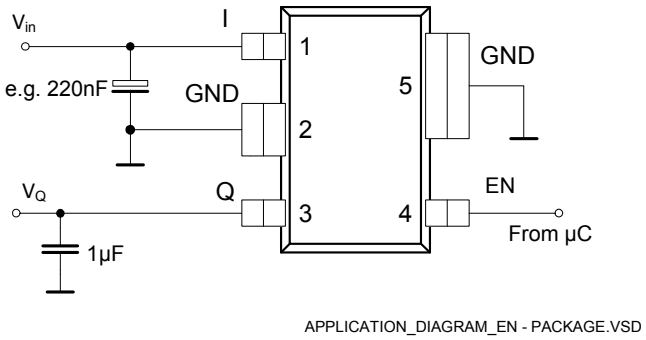


Figure 5 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

A typical application circuit of the TLS202B1 is shown in **Figure 5**. It shows a generic configuration of the voltage regulator, with the recommendable minimum number of components one should use. Theoretically, if there is no risk of high frequency noise at all, even the small input filter capacitor can be omitted. For a normal operation mode of the device only an output capacitor and a small ceramic input capacitor are needed. Depending on the application's environment, additional components like an input buffer capacitor or a reverse polarity protection diode can be considered as well.

Input Filter Capacitor C_I

A small ceramic capacitor (e.g. 220nF in **Figure 5**) at the device input helps filtering high frequency noise. To reach the best filter effect, this capacitor should be placed as close as possible to the input pin. The input filter capacitor does not have an influence on the stability of the regulation loop of the device, but in case of fast load changes an input capacitor can buffer the input voltage. Otherwise the parasitic inductance of the input line length can drop the input voltage at the IC terminals and influence the output voltage.

Output Capacitor C_Q

The output capacitor is the external component that is required in any case as it is a part of the device's regulation loop. To maintain stability of this loop, the TLS202B1 requires at least an output capacitor respecting the values given in **"Functional Range" on Page 6**. The given parameters ensure a stable regulation loop in general, in case of fast load changes in the application the output capacitance may have to be increased according to the requirements for load responses.

9 Package Outlines

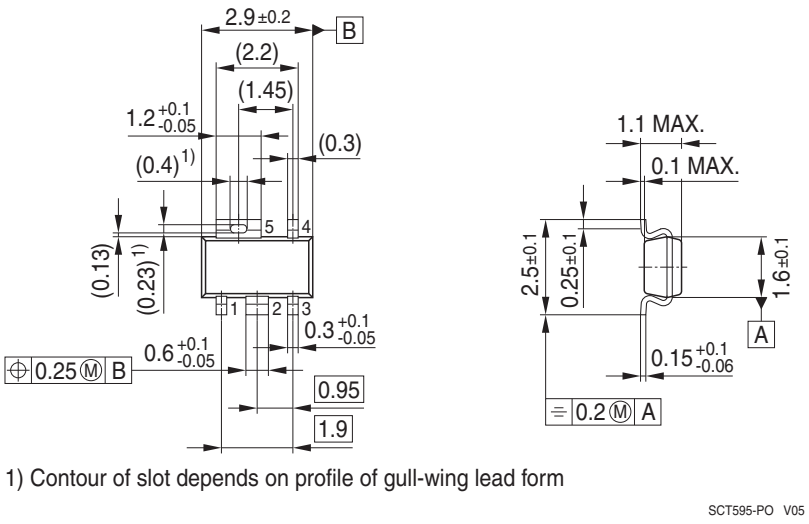


Figure 6 PG-SCT595

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.0	2015-06-23	Initial Data Sheet.

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