PDSP16256/A

Programmable FIR Filter

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Features

- Sixteen MACs in a Single Device
- Basic Mode is 16-Tap Filter at up to 25MHz Sample Rates
- Programmable to give up to 128 Taps with Sampling Rates Proportionally Reducing to 3·125MHz
- 16-bit Data and 32-bit Accumulators
- Can be configured as One Long Filter or Two Half-Length Filters
- Decimate-by-two Option will Double the Filter Length
- Coefficients supplied from Host System or local EPROM

Applications

- High Performance Digital Filters

Ordering Information

Commercial (0°C to +70°C)
PDSP16256A/C0/AC 25MHz, PGA package
Industrial (-40°C to +85°C)
PDSP16256 B0/AC 20MHz, PGA package
PDSP16256 B0/GC 20MHz, QFP package
Military (-55°C to +125°C)
PDSP16256 MC/AC1R 20MHz, MIL-STD-883* (latest revision), PGA package
PDSP16256 MC/GC1R 20MHz, MIL-STD-883* (latest revision), QFP package

*See notes following Electrical Characteristics for further information on MIL-STD-883 screening

Associated Products

PDSP16350 I/Q Splitter/NCO
PDSP16510A FFT Processor

Description

The PDSP16256 contains sixteen multiplier - accumulators, which can be multi cycled to provide from 16 to 128 stages of digital filtering. Input data and coefficients are both represented by 16-bit two's complement numbers with coefficients converted internally to 12 bits and the results being accumulated up to 32 bits.

In 16-tap mode the device samples data at the system clock rate of up to 25MHz. If a lower sample rate is acceptable then the number of stages can be increased in powers of two up to a maximum of 128. Each time the number of stages is doubled, the sample clock rate must be halved with respect to the system clock. With 128 stages the sample clock is therefore one eighth of the system clock.

In all speed modes devices can be cascaded to provide filters of any length, only limited by the possibility of accumulator overflow. The 32-bit results are passed between cascaded devices without any intermediate scaling and subsequent loss of precision.

The device can be configured as either one long filter or two separate filters with half the number of taps in each. Both networks can have independent inputs and outputs.

Both single and cascaded devices can be operated in decimate-by-two mode. The output rate is then half the input rate, but twice the number of stages are possible at a given sample rate. A single device with a 20MHz clock would then, for example, provide a 128-stage low pass filter, with a 5MHz input rate and 2·5MHz output rate.

Coefficients are stored internally and can be down loaded from a host system or an EPROM. The latter requires no additional support, and is used in stand alone applications. A full set of coefficients is then automatically loaded at power on, or at the request of the system. A single EPROM can be used to provide coefficients for up to 16 devices.

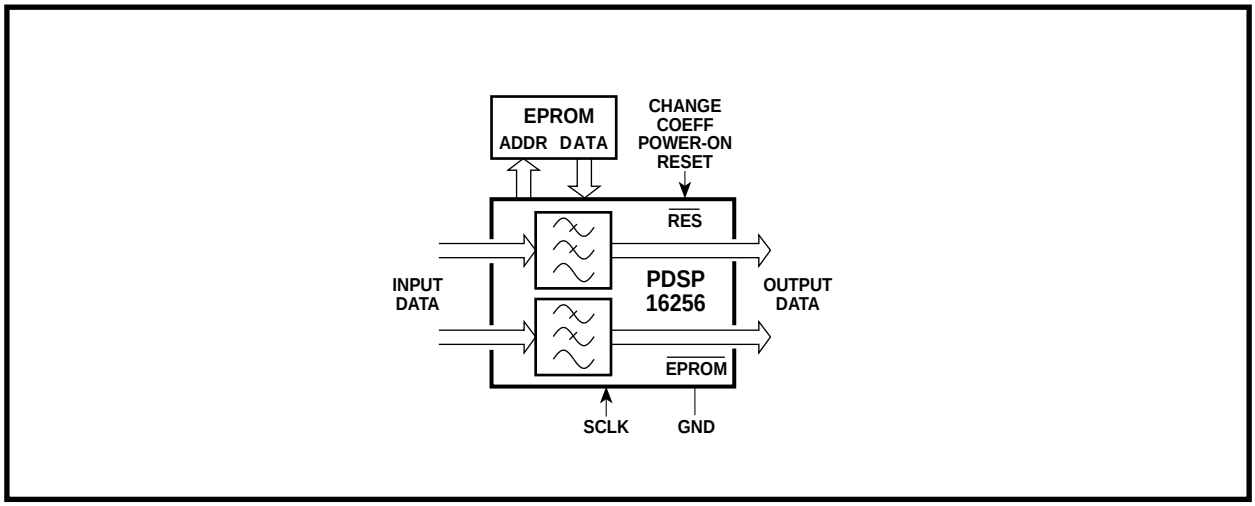


Figure. 1 A dual filter application

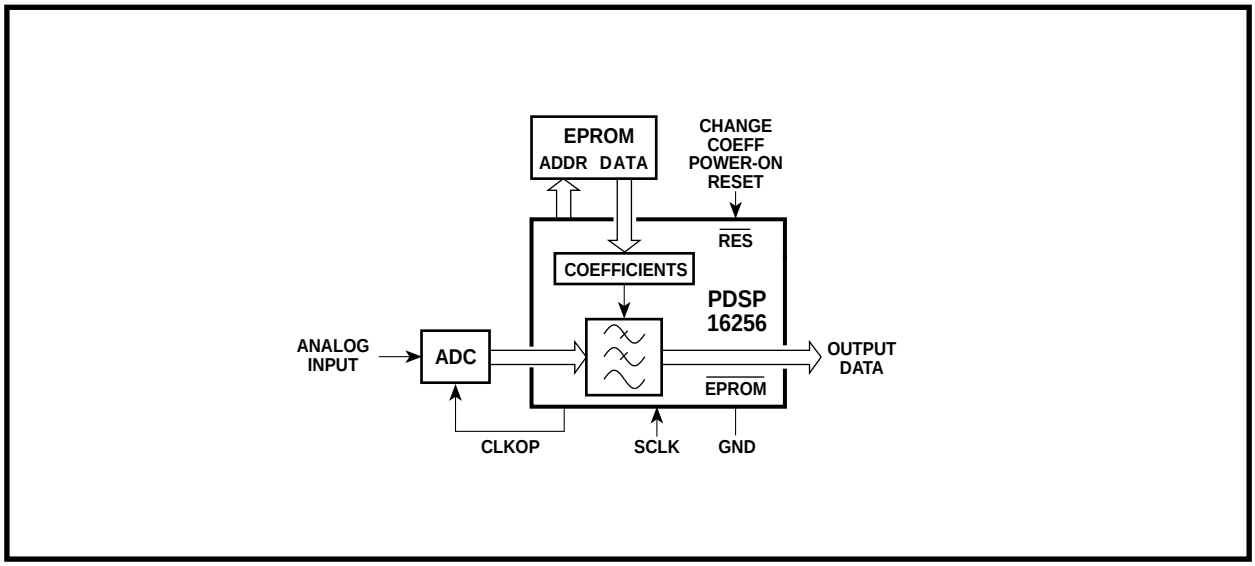


Figure. 2 Typical system application

Signal	Description
DA15:0	16-bit data input bus to Network A.
DB15:0	Delayed data output bus in the single filter mode. Connected to the data input bus of the next device in a cascaded chain. Input to Network B in the dual filter modes.
X31:0	Expansion input bus in the single filter mode. Connected to the previous filter output in a cascaded chain. The inputs are not used on a single device system or on the Termination device in a cascaded chain. The X bus provides the output from Network B in both dual modes.
F31:0	In single filter mode this bus holds the main device output. In dual mode it holds the output from Network A.
FEN	Filter enable. The first high present on an SCLK rising edge defines the first data sample. The control register and coefficient memory must be configured befor FEN is enabled.The signal must stay active whilst valid data is being received and must be low if FRUN is high.
DFEN	Delayed filter enable. This output is connected to the Filter Enable input of the next device in a cascaded chain when moving towards the termination device and with multiple stand-alone EPROM-loaded configurations. It is used to coordinate the control logic within each device.
SWAP	Selects either the upper or lower set of coefficients for Bank Swap. A low selects the lower bank, a high the upper bank.
FRUN	In EPROM load mode, when high this signal allows continuous filter operations to occur without the need for the initial FEN edge. If the device is not a single, interface or master device then this pin must be tied low.
$\overline{\text{DCLR}}$	A low on this signal on the SCLK rising edge will clear all the internal accumulators. $\overline{\text{DCLR}}$ need only remain low for a single cycle, signal BUSY will indicate when the internal clearing is complete. After a clear the device must be re-synchronised to the data stream using FEN. It is recommended that FEN is taken low at the same time as clear. FEN may then be taken high to synchronise the data stream once BUSY has returned low.
C15:0	16-bit coefficient input bus. In the Byte mode of operation, C15:8 have alternative uses as explained in the text.
A7:0	Coefficient address bus. In the EPROM mode A7:0 are address outputs for an EPROM. In the remote host mode they are inputs from the host. A7 is not used when coefficients are loaded as 16-bit words.
CCS	This pin is similar in operation to A7:0 and provides a higher order address bit. When low the coefficients are loaded, when high the control register is loaded.
$\overline{\text{WEN}}$	In the remote mode this pin is an input which when low enables the load operation. In the EPROM mode it is an output which provides the write enable for other slave devices.
$\overline{\text{CS}}$	This pin is always an input and must also be low for the internal write operation to occur.
$\overline{\text{BYTE}}$	When this pin is tied low, coefficients are loaded as two 8-bit bytes. When the pin is high they are loaded as 16-bit words. In the EPROM mode this pin is ignored.
$\overline{\text{EPROM}}$	When this pin is tied low coefficients are loaded as bytes from an external EPROM. The device outputs an address on A7:0. When the pin is high coefficients must be loaded from a remote master. They can then be transferred individually rather than as a complete set.
SCLK	The main system clock; all operations are synchronous with this clock. The clock rate must be either 1, 2, 4, or 8 times the required data sampling rate. The factor used depends on the required filter length.
CLKOP	This output, when used to enable SCLK, can provide a data sampling clock. It has the effect of dividing the SCLK rate by 1, 2, 4 or 8 depending on the filter mode selected.
$\overline{\text{OEN}}$	Tri-state enable for the F bus. When high the outputs will be high impedance. $\overline{\text{OEN}}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge
BUSY	A high on this signal indicates that the device is completing internal operations and is not yet able to accept new data. The signal is used during automatic EPROM loading, reset and accumulator clearing.
$\overline{\text{RES}}$	When this pin is low the control logic and accumulators are reset. In the EPROM mode it will initiate a load sequence when it goes high.

NOTES
1. Unused buses (e.g. X31:0 when the device is configured in single or termination mode) can be set to any value. They should however be maintained at a valid logic level to avoid an increase in power consumption.
2. To ensure correct input voltage thresholds are maintained all the V_{DD} and GND pins must be connected to adequate power and ground planes.

Table 1 Pin descriptions

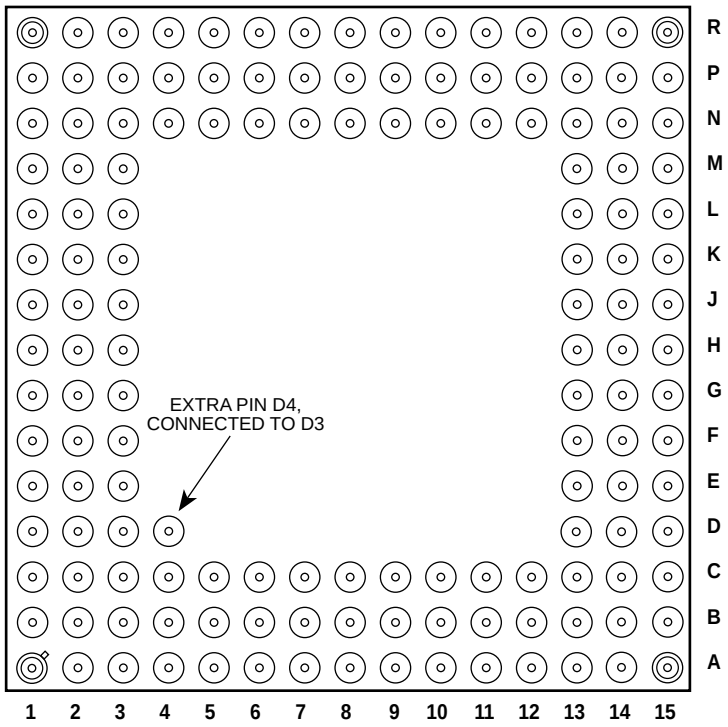


Fig. 3a Pin connections for 144 pin PGA package (bottom view)

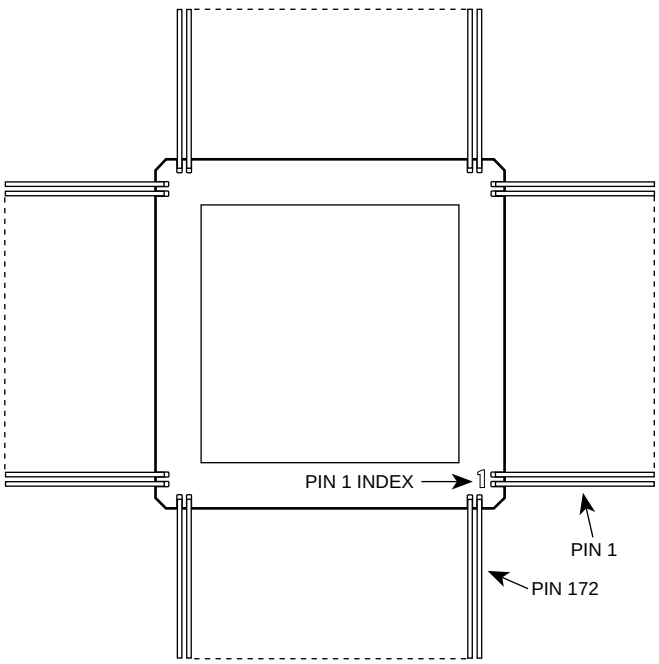


Fig. 3b Pin connections for 172 pin QFP (top view)

Figure. 3 Pin connection diagrams (not to scale). See Table 1 for signal descriptions and Table 2 for pinouts.

GG	AC	Signal	GG	AC	Signal	GG	AC	Signal	GG	AC	Signal
1	A15	F0	44	R14	SWAP	87	P1	C15	130	-	GND
2	B15	F1	45	-	GND	88	-	GND	131	A1	BUSY
3	D13	F2	46	N12	$\overline{OEN}$	89	-	GND	132	A2	X0
4	C14	F3	47	P13	CLKOP	90	N2	$\overline{WEN}$	133	-	V_{DD}
5	G15	V_{DD}	48	-	V_{DD}	91	N1	CCS	134	C4	X1
6	C15	F4	49	R13	DA0	92	M2	$\overline{CS}$	135	B3	X2
7	D14	F5	50	P12	DA1	93	-	V_{DD}	136	A3	X3
8	J15	GND	51	N11	DA2	94	L3	$\overline{RES}$	137	B4	X4
9	E13	F6	52	R12	DA3	95	M1	SLCK	138	C5	X5
10	D15	F7	53	P11	DA4	96	M3	GND	139	A4	X6
11	E14	F8	54	R11	DA5	97	-	V_{DD}	140	-	GND
12	E15	F9	55	R9	GND	98	L2	$\overline{BYTE}$	141	B5	X7
13	F13	F10	56	N10	DA6	99	L1	$\overline{EPROM}$	142	A5	X8
14	F14	F11	57	P10	DA7	100	K3	A0	143	A7	V_{DD}
15	F15	F12	58	R10	DA8	101	K2	A1	144	C6	X9
16	-	GND	59	P9	DA9	102	K1	A2	145	B6	X10
17	G14	F13	60	R7	V_{DD}	103	J2	A3	146	A6	X11
18	G13	F14	61	N9	DA10	104	J3	A4	147	B7	X12
19	H14	F15	62	P8	DA11	105	G1	V_{DD}	148	C7	X13
20	-	V_{DD}	63	R8	DA12	106	H2	A5	149	B8	X14
21	H15	F16	64	N8	DA13	107	H1	A6	150	A9	GND
22	H13	F17	65	P7	DA14	108	J1	GND	151	A8	X15
23	J14	F18	66	R6	DA15	109	H3	A7	152	C8	X16
24	K15	F19	67	-	GND	110	G2	DB0	153	B9	X17
25	-	V_{DD}	68	N7	C0	111	F1	DB1	154	A10	X18
26	J13	F20	69	P6	C1	112	G3	DB2	155	C9	X19
27	K14	F21	70	R5	C2	113	-	GND	156	B10	X20
28	-	GND	71	N6	C3	114	F2	DB3	157	A11	X21
29	L15	F22	72	P5	C4	115	E1	DB4	158	C10	X22
30	K13	F23	73	R4	C5	116	F3	DB5	159	-	GND
31	L14	F24	74	-	V_{DD}	117	E2	DB6	160	B11	X23
32	M15	F25	75	N5	C6	118	D1	DB7	161	A12	X24
33	L13	F26	76	P4	C7	119	-	V_{DD}	162	C11	X25
34	M14	F27	77	R3	C8	120	E3	DB8	163	-	V_{DD}
35	N15	F28	78	P3	C9	121	D2	DB9	164	B12	X26
36	-	GND	79	N4	C10	122	C1	DB10	165	A13	X27
37	N14	F29	80	-	GND	123	C2	DB11	166	B13	X28
38	M13	F30	81	R2	C11	124	D3	DB12	167	C12	X29
39	P15	F31	82	P2	C12	125	B1	DB13	168	A14	X30
40	-	V_{DD}	83	N3	C13	126	B2	DB14	169	-	GND
41	P14	FEN	84	-	V_{DD}	127	-	GND	170	B14	X31
42	N13	DFEN	85	-	GND	128	C3	DB15	171	-	V_{DD}
43	R15	$\overline{DCLR}$	86	R1	C14	129	-	V_{DD}	172	C13	FRUN

NOTE. All GND and V_{DD} pins must be used

Table 2 Pin connections for AC144 and GC172 packages

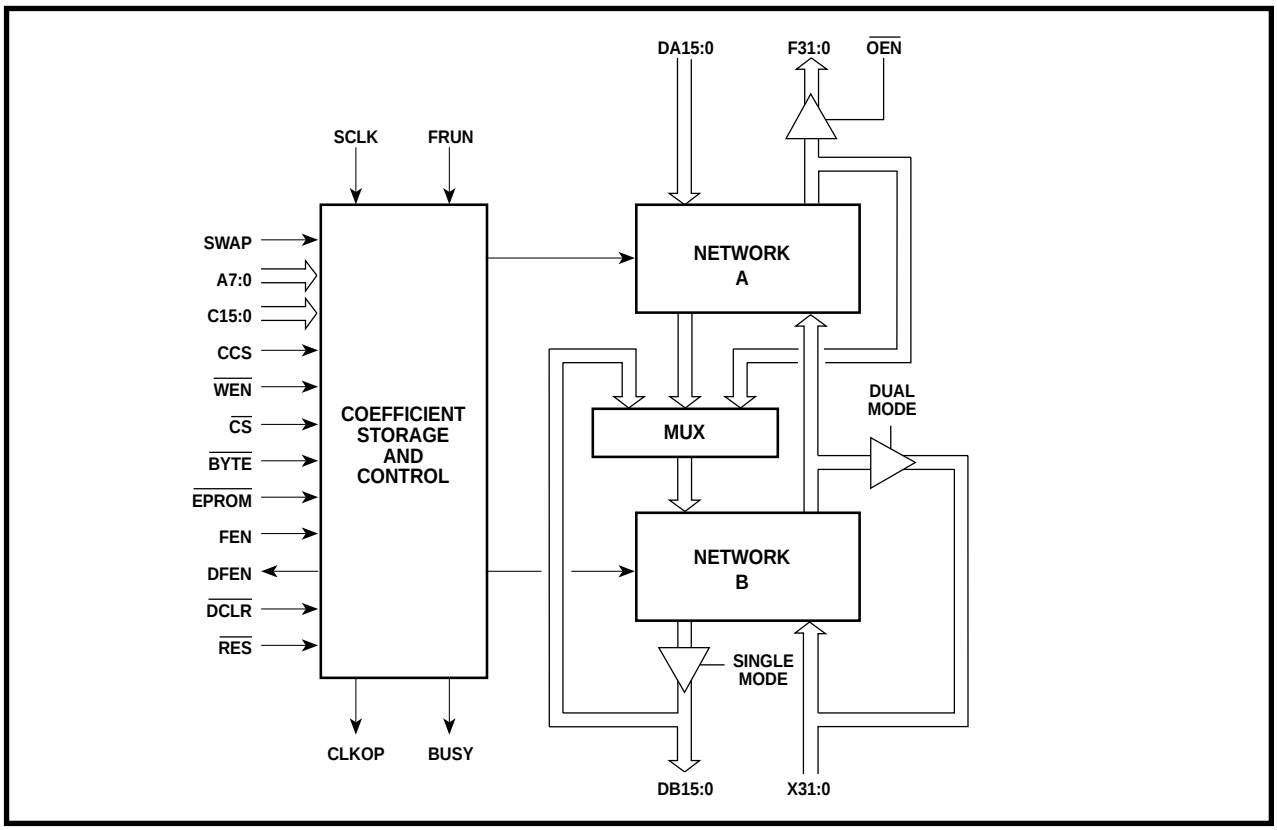


Figure. 4 Block Diagram

Operational Overview

The PDSP16256 is an application specific FIR filter for use in high performance digital signal processing systems. Sampling rates can be up to 25MHz. The device provides the filter function without any software development, and the options are simply selected by loading a control register. The device can be user configured as either a single filter, or as two separate filters. The latter can provide two independent filters for the in-phase and quadrature channels after IQ splitting, or can provide two filters in cascade for greater stop band rejection.

The device operates from a system clock, with rates up to 25MHz. This clock must be 1, 2, 4, or 8 times the required sampling frequency, with the higher multiplication rates producing longer filter networks at the expense of lower sampling rates. Devices can be connected in cascade to produce longer filter lengths. This can be accomplished without the need for any additional external data delays, and all the single device options remain available.

Continuous inputs are accepted, and continuous results produced after the internal pipeline delay. Connection can be made directly to an A-D converter. The filter operation can be synchronised to a Filter Enable signal (FEN) whose positive going edge marks the first data sample. The internal multiplier accumulator array can be cleared with a dedicated input. This is necessary if erroneous results obtained during the normal data 'flush through' are not permissible in the system.

Coefficients can be loaded from a host system using a conventional peripheral interface and separate data bus. Alternatively, they can be loaded as a complete set from a byte wide EPROM. The device produces addresses for the EPROM and a BUSY output indicates that the transfer is occurring. Up to sixteen devices can have their coefficients supplied from a single EPROM. These devices need not necessarily be part of the same filter network.

Each of the filter networks shown in Fig. 4 contains eight systolic multiplier accumulator stages; an example with four stages is shown in Fig. 5. Input data flows through the delay lines and is presented for multiplication with the required coefficient. This is added to either the last result from this accumulator or the result from the previous accumulator. The filter results progress along the adders at the data sample rate. If the sample rate equals SCLK divided by four, for example, then the accumulated result is passed onto the next stage every fourth cycle. The structure described is highly efficient when used to calculate filtered results from continuous input data.

A comprehensive digital filter design program is available for PC compatible machines. This will optimise the filter coefficients for the filter type required and number of taps available at the selected sample rate within the PDSP16256 device. An EPROM file can be automatically generated in Motorola S-record format.

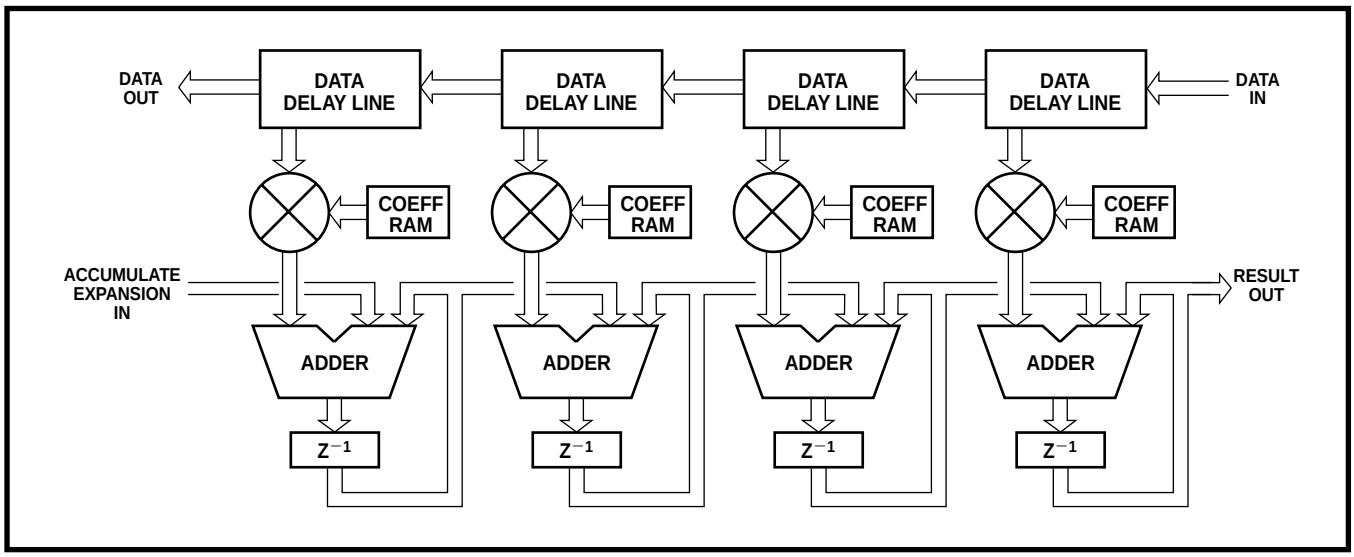


Figure. 5 Filter network diagram

Single Filter Options

When operating as a single filter the device accepts data on the 16-bit DA bus at the selected sample rate, see Figs. 5 and 6. Results are presented on the 32-bit F bus, which may be tristated using the $\overline{OEN}$ input. Signal $\overline{OEN}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge. Devices may be cascaded this allows filters with more taps than available from a single device. To accomplish this two further buses are utilised. The DB bus presents the input data to the next device in cascade after the appropriate delay, while, partial results are accepted on the X bus.

Single filter mode is selected by setting control register bit 15 to a one. The required filter length is then selected using control register bits 14 and 13 as summarised in Table 3. The options define the number of times each multiplier accumulator is used per sample clock period. This can be once, twice, four times, or eight times.

In addition a normal/decimate bit (CR12) allows the filter length to be doubled at any sample rate. This is possible when the filter coefficients are selected to produce a low pass filter, since the filtered output would then not contain the higher frequency components present in the input. The Nyquist criterion, specifying that the sampling rate must be at least double the highest frequency component, can still then be satisfied even though the sampling rate has been halved.

The system clock latency for a single device is shown in Table 3. This is defined as the delay from a particular data sample being available on the input pins to the first result including that input appearing on the output pins. It does not include the delay needed to gather N samples, for an N tap filter, before a mathematically correct result is obtained.

CR 14	CR 13	CR 12	Input Rate	Output Rate	Filter Length	Setup Latency
0	0	0	SCLK	SCLK	16 Taps	16
0	0	1	SCLK	SCLK/2	32 Taps	17
0	1	0	SCLK/2	SCLK/2	32 Taps	16
0	1	1	SCLK/2	SCLK/4	64 Taps	18
1	0	0	SCLK/4	SCLK/4	64 Taps	20
1	0	1	SCLK/4	SCLK/8	128 Taps	24
1	1	0	SCLK/8	SCLK/8	128 Taps	24

Table 3 Single Filter options

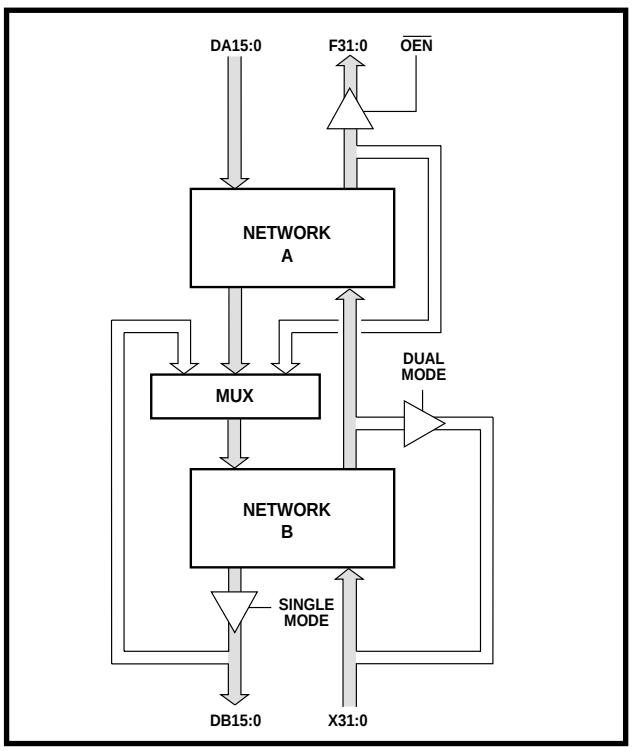


Figure. 6 Single Filter bus utilisation

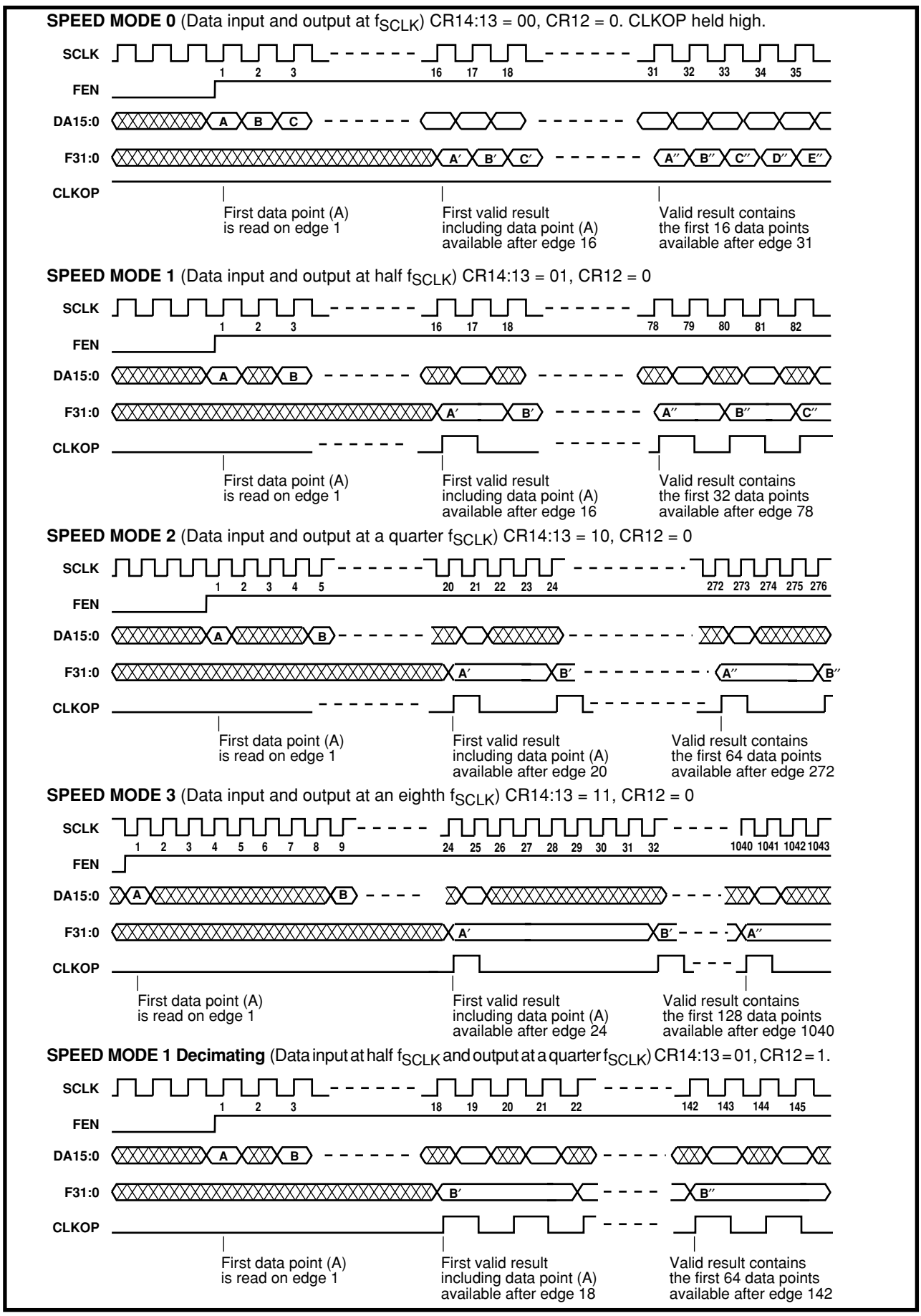


Figure. 7 Single Filter timing diagrams

Dual Indipendant Filter Options

When operating as two independent filters the device accepts 16 bit data on both the DA and DB buses at the selected sample rate, see Fig. 8. Results are available from both the F and X buses. The F bus may be tristated using the $\overline{OEN}$ input. Signal $\overline{OEN}$ is registered onto the device and does not therefore take effect until the first SCLK rising edge

Each filter must be configured in the same manner, and multiple device expansion is not possible due to the pin re-organization. The latter requirement can, of course, still be satisfied by several devices configured as single filters.
Dual independent filter mode is selected by setting control register bits 15 and 4 to a zero. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. As in single filter mode normal or decimate-by-two operation can be selected using control register bit 12.

CR 14 13 12	Input Rate	Output Rate	Filter Length	Setup Latency	
				Ind	Cas
0 0 0	SCLK	SCLK	8 Taps	16	27
0 0 1	SCLK	SCLK/2	16 Taps	17	-
0 1 0	SCLK/2	SCLK/2	16 Taps	16	28
0 1 1	SCLK/2	SCLK/4	32 Taps	18	-
1 0 0	SCLK/4	SCLK/4	32 Taps	20	36
1 0 1	SCLK/4	SCLK/8	64 Taps	24	-
1 1 0	SCLK/8	SCLK/8	64 Taps	24	40

Table 4. Dual Filter options

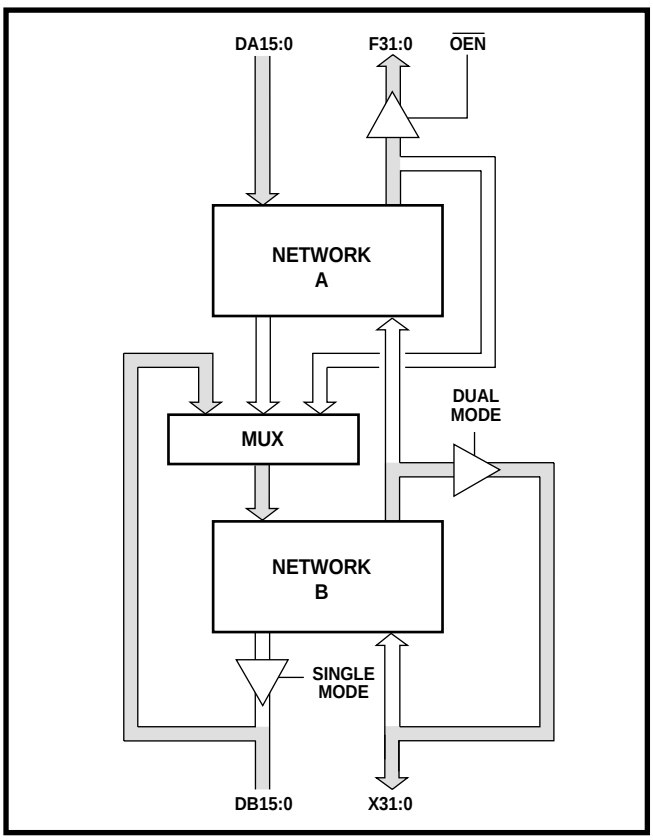


Figure. 8 Dual independent filter bus utilisation

Dual Cascaded Filter Options

When operating as two cascaded filters the device accepts 16 bit data on the DA bus at the selected sample rate. Results are presented on the 32-bit X bus, see Fig. 9. Each filter must be configured in the same manner. Multiple device expansion is not possible in this mode.

Dual cascaded filter mode is selected by setting control register bit 15 to a zero and bit 4 to a one. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. The decimate-by-two option is not available in this mode.
The data for the second filter network is extracted as the middle 16 bits from the first networks accumulated result. For successful operation the first filter network must have unity gain. See the section on filter accuracy for more details.

The cascade option is used to increase the stop band rejection in a practical filter application. Theoretically, increasing the number of taps in an FIR filter will increase the stop band rejection, but this assumes floating point calculations with no accuracy limitations. In practice, with fixed point arithmetic, better performance is achieved with two smaller filters in series.

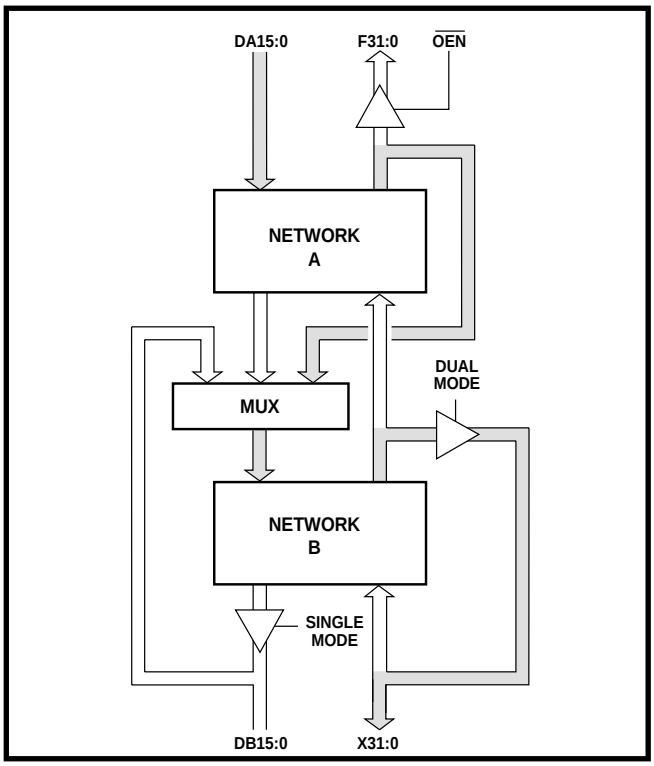


Figure. 9 Dual cascaded filter bus utilisation

Filter Accuary

Input data and coefficients are both represented by 16-bit two's complement numbers. The coefficients are converted to twelve bits by rounding towards zero. This is achieved as follows. If the coefficient is positive then the least significant 4 bits are discarded. If the coefficient is negative then the logical 'OR' of the least significant 4 bits are added to the remainder of the word. Twelve bit coefficients can be used directly provided the least significant four bits are set to zero.

The FIR filter results are calculated using a multiplier accumulator structure as shown in Fig. 10. The truncation and word growth allowed for in the data path are explained in Fig. 10. The 16-bit data and 12-bit coefficient inputs (each with one sign bit before the binary point), are presented to the multiplier. This produces a 28-bit result with two bits before the binary point. Producing the full 28-bit result ensures that if both the data and coefficients are set to logic 1 a valid result is generated. Prior to entering the accumulator the least significant 4 bits of the multiplier result are truncated and the resulting 24 bits sign extended to 32 bits. The final accumulator result is 32 bits with 10 bits before the binary point. Thus 9 bits of word growth are allowed within the accumulator. All accumulator bits are made available on the output pins.

In cascade mode the middle 16 bits from the network A accumulator are fed round to the network B data inputs, see Fig. 11.

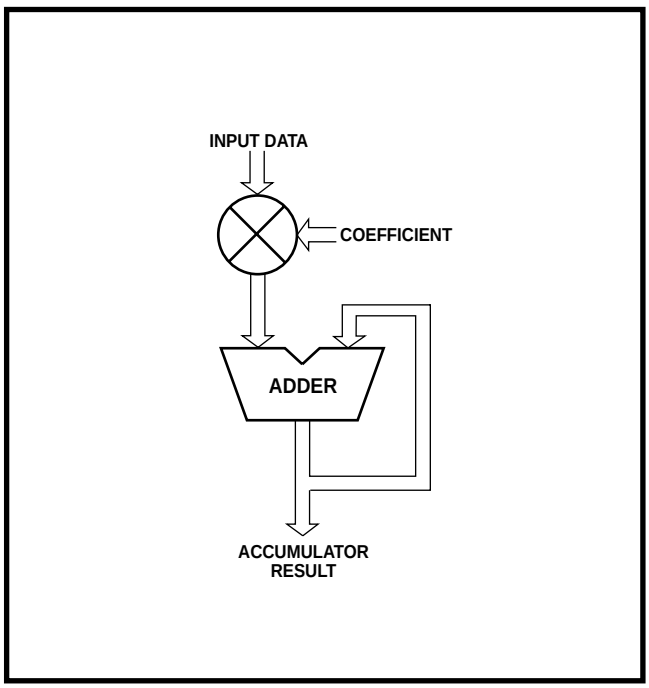


Figure. 10 Multiplier Accumulator

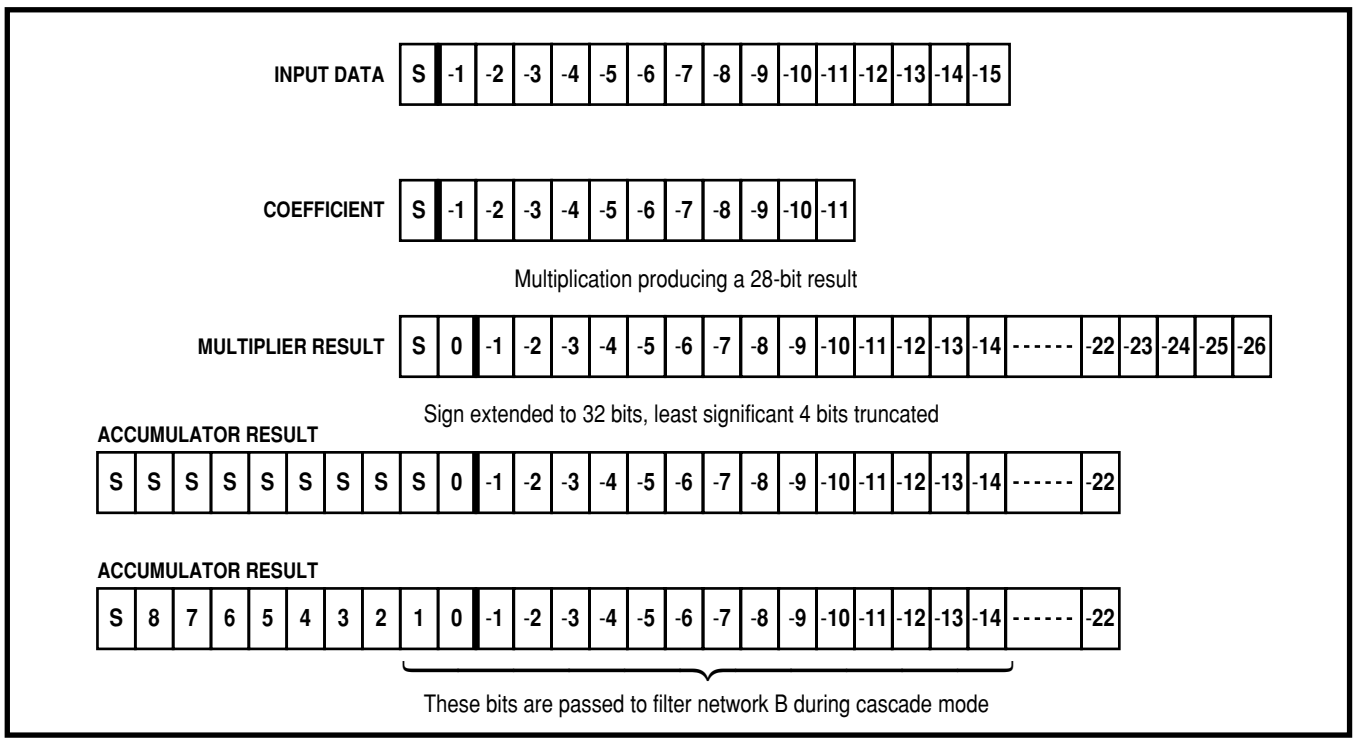


Figure. 11 Filter accuracy

Cascading Devices

When the filter requirements are beyond the capabilities of a single device, it is possible to connect several devices in cascade increasing the number of taps available at the required sample rate. Within each device all filter length, decimate, and bank swap options are still possible, but each device in the chain must be similarly programmed and configured as a single filter.

The number of devices which can be cascaded is only limited by the possibility of overflow in the 32-bit intermediate accumulations. If more than sixteen devices are cascaded in auto EPROM load mode, then an additional EPROM will be needed.

In modes where the data sample rate does not equal the clock rate. Then the cascade arrangement shown in Fig. 12 is used. Delayed data is passed from device to device in one direction, while intermediate results flow in the opposite direction. The interface device both accepts the input data and produces the final result. It is not necessary for each device to know its exact position in the chain, but the device which receives the input data and produces the final result must be identified, as must the device which terminates the chain. The former is known as the Interface device and the latter as the Termination device, all others are Intermediate devices. Control Register bits CR11:10 are used to define these positions as shown in Table 6.
The control logic in each of the devices must be synchronised with respect to the Interface device. This is achieved by connecting the Delayed Filter Enable output (DFEN) to the Filter Enable input (FEN) of the next device in the chain. The Interface device, itself, needs a FEN signal produced by the system, unless in EPROM mode, where FRUN may be pulled high. Even when the latter is true, the FEN connection must be made between the remaining devices in the chain. By effectively extending the filter length, the cascade latency is therefore the same as for the single device in the same mode. Once the pipeline is initially flushed the latency is as given in Table 3.

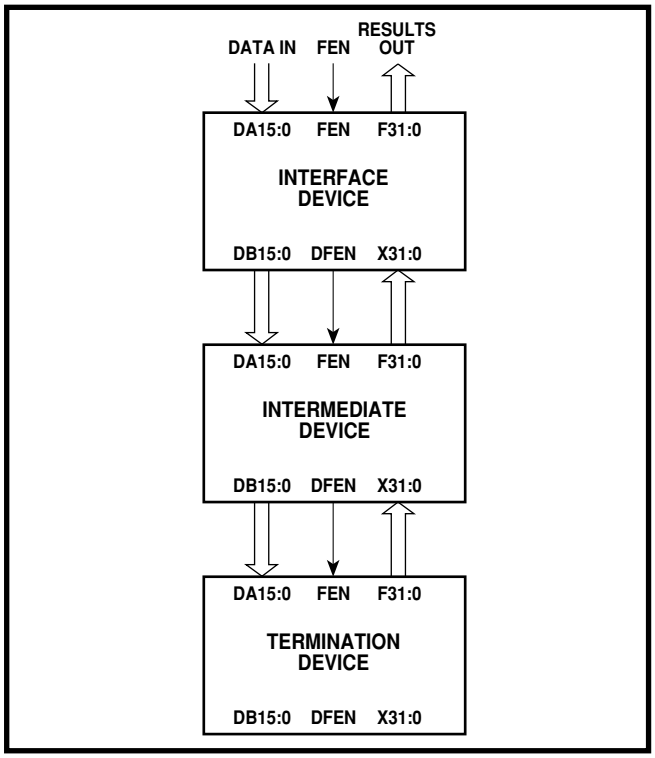


Figure. 12 Three-device cascaded system

When devices are cascaded such that the data sample rate equals the clock rate, (Control register bits 14:13 = 00), then a different cascade configuration must be used. This is shown in Fig. 13. The number of devices that can be cascaded is, again, only limited by the 32-bit accumulators.

In this mode the delayed data is passed from device to device in the same direction as the intermediate results. The device which accepts the input data is now at the opposite end of the chain to the device which produces the final result. The control logic in each of the devices must be synchronised this is achieved by connecting all the device FEN inputs to the global FEN. The cascade latency for the complete filter is built up from the 12 delays from the termination device, 8 delays from the interface device and additional intermediate devices each adding 4 delays.

Avalable Options

No more than 128 coefficients can be stored internally. This limits the filter length / decimate / bank swap options to those which do not require more than that number of coefficients. Thus when a filter with 128 taps is to be implemented in a single device, it is not possible to decimate or bank swap. When a filter with 64 taps is implemented, decimate or bank swap are possible, but not both. With all other filter lengths, all decimate and bank swap configurations are possible.

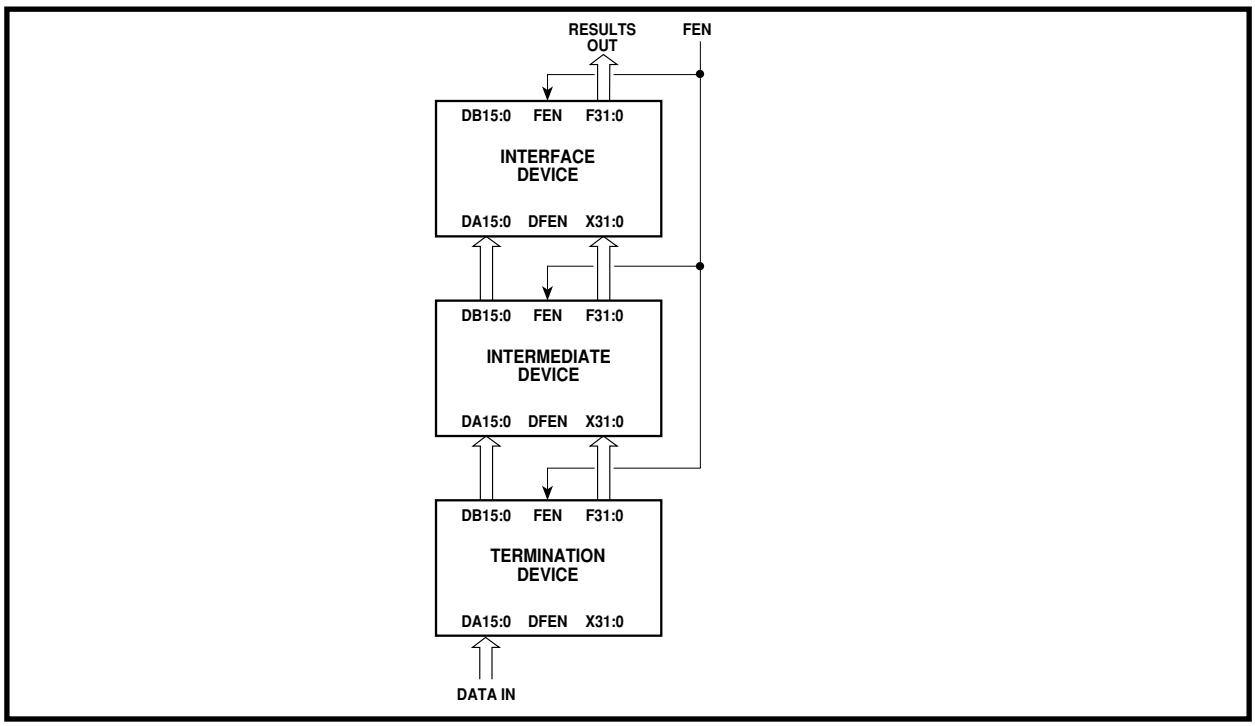


Figure. 13 Full speed cascaded system

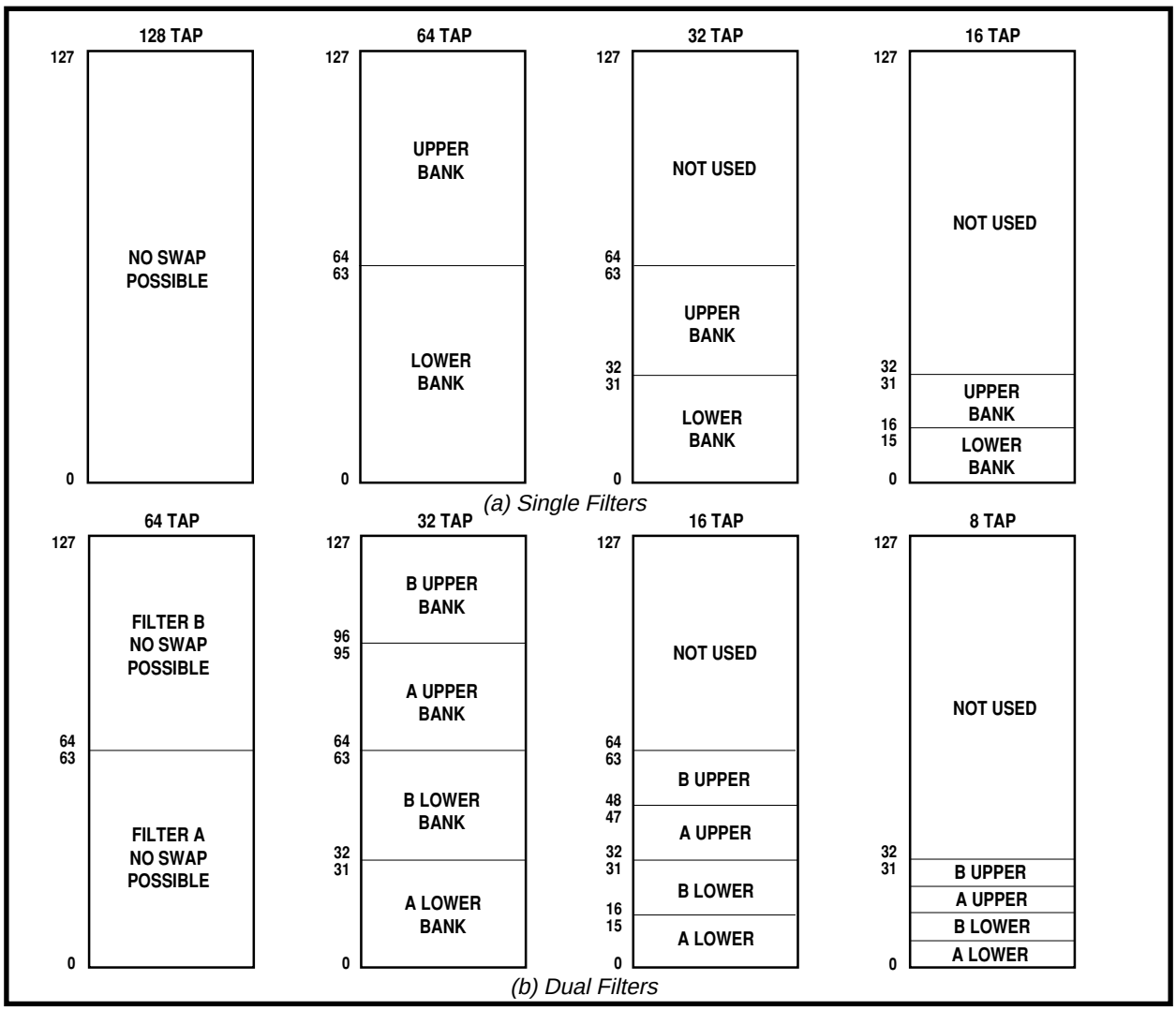


Figure. 14 Coefficient memory map

Filter Control

Two control modes are available selected by input signal FRUN. In EPROM load mode, when FRUN is tied high the device will commence operation once the coefficients have been loaded. The CLKOP signal indicates when new input data is required and that new results are available, see Fig. 7. In both EPROM and remote master load modes, when FRUN is tied low filter operation will not commence until a high has been detected on signal FEN. This mode allows synchronisation to an existing data stream. FEN should be taken high when the first valid data sample is available so that both are read into the device on the next SCLK rising edge. Proper device operation requires FEN to be low during control register and coefficient loading both in EPROM mode and Remote Master mode. After loading coefficients, filter operation is determined by FRUN and FEN as described above.

During device reset $\overline{RES}$ must be held low for a minimum of 16 SCLK cycles. After a reset the control register returns to its default state of $8C80_{HEX}$. This places the device into the following mode :

- Single filter
- Sample rate equal to the clock rate
- Non-decimating
- A single device (Not in a cascade chain)
- Bank swap selected by bit in the control register

Coeficient Bank Swap

A Bank Swap feature is provided which allows all coefficients to be simultaneously replaced with a different set. A bit in the Control Register (CR7) allows the swap to be controlled by either input signal SWAP or Control Register bit (CR6). The latter is useful if the device is controlled by a microprocessor, when driving a separate pin would entail additional address decoding logic and an external latch.

If SWAP or bit CR6 is low, the coefficients used will be those loaded into the lower banks illustrated in Fig. 14. When the SWAP or CR6 is high, the upper banks are used.

The actual swap will occur when the next sampling clock active going transition occurs. This can be up to seven system clocks later than the swap transition, and is filter length dependent. The first valid filtered output will then occur after the pipeline latencies given in Tables 3 and 4.

Loading Coefficients

When the device is to operate in a stand alone application then the coefficients can be down loaded as a complete set from a previously programmed EPROM. Alternatively if the system contains a microprocessor they can be individually transferred from a remote master under software control. In any mode the system clock must be present and stable during the transfer, and the addressing scheme is such that the least significant address specifies the coefficient applied to the first multiplier seen by incoming data. The addresses used during the load operation are those illustrated in Fig. 15. The Control Register is loaded when CCS is high. In byte mode address A0 is used to select the portion of control register loaded, otherwise the address bits are redundant. When an EPROM is used to provide coefficients, this redundancy causes the number of locations needed for any device to be double that for the coefficients alone.

Auto EPROM LOAD

When $\overline{EPROM}$ is tied low, the PDSP16256 assumes the role of a master device in the system and controls the loading of coefficients from an external EPROM, see Fig.15. A load sequence commences when the $\overline{RES}$ input goes high, and will continue until every coefficient has been loaded. BUSY goes high to indicate that a load sequence is occurring and the filter output is invalid. The device will not commence a filter operation until the FEN edge is received after BUSY has gone low. This requirement can be avoided if FRUN is tied high.

The address bus pins become outputs on the Master device, and produce a new address every four system clock periods. This four clock interval, minus output delays and the data set up time, defines the available EPROM access time.

The coefficients are always loaded as bytes. The state ofb the $\overline{BYTE}$ pin on the master device is ignored. This arrangement also allows the eight most significant coefficient bus pins (C15:8) to be used for other purposes as described later. Since the 16-bit coefficients are loaded in two bytes the A0 pin specifies the required byte. The maximum number of stored coefficients is 128, eight address outputs are therefore provided for the EPROM. These eight outputs from the Master must also drive the address inputs on the slave devices.

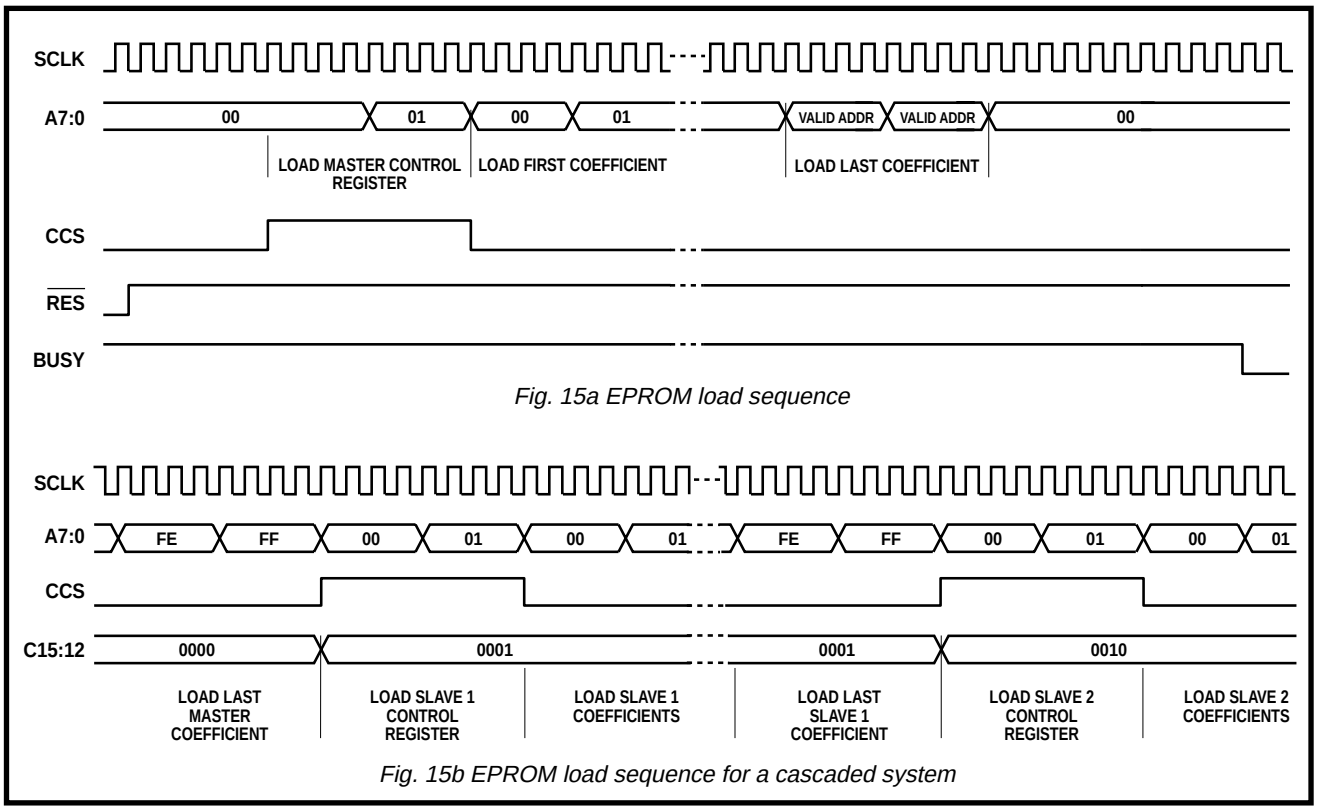


Fig. 15a EPROM load sequence

Fig. 15b EPROM load sequence for a cascaded system

Figure. 15 EPROM load sequence timing diagrams

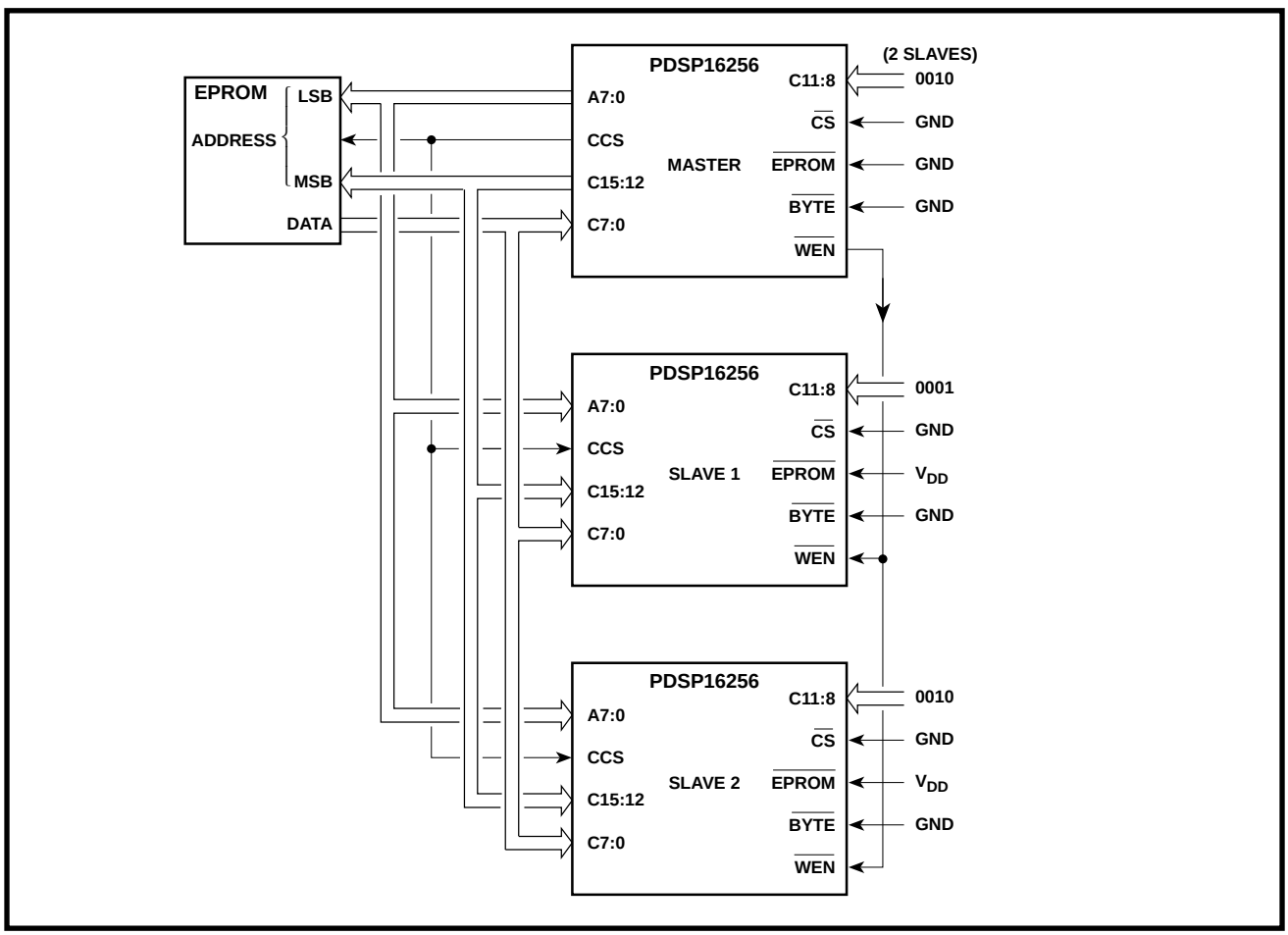


Figure. 16 Three device auto EPROM load

When the filter length is less than the maximum, the PDSP16256 will only transfer the correct number of coefficients, and one or more significant address bits will remain low. Sufficient coefficients are always loaded to allow for a possible Bank Swap to occur, and the EPROM allocation must allow for this even if the feature is not to be used. Table 5 shows the number of coefficients loaded for each of the modes.

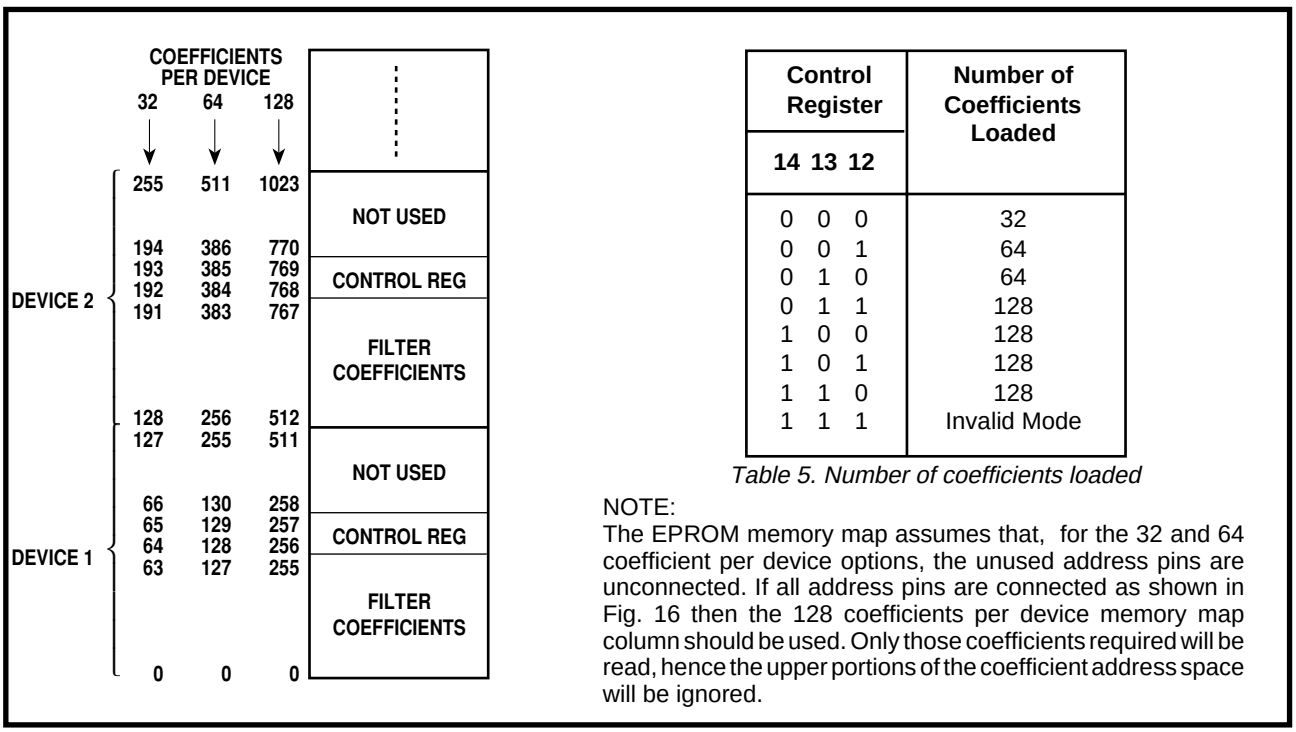
If several devices are cascaded, only one device assumes the role of the Master by having its $\overline{\text{EPROM}}$ pin grounded. It produces a $\overline{\text{WEN}}$ signal for the other devices, plus four higher order address outputs on C15:12, see Fig. 16. The extra address bits on C15:12 define separate areas of EPROM, containing coefficients for up to fifteen additional devices. The least significant block of memory must always be allocated to the Master device. The additional devices need not in practice be all part of the same cascaded chain, but can consist of several independent filters. They must, however, all havetheir $\overline{\text{BYTE}}$ pins tied low. FRUN can still be used to start these independent filters after all the devices have been loaded. In this case, however, each slave FEN pin should be driven by DFEN from the master device.

When one EPROM is supplying information for several devices, some means of selectively enabling each additional device must be provided. This is achieved by using the C11:8 pins on the slave devices as binary coded inputs to define one to fifteen extra devices.

These coded inputs always correspond to the block address used for the segment of EPROM allocated to that device. Code 'all zeros' must not be used since the Master device has implied use of the bottom segment. This is necessary since the C11:8 pins are alternatively used on the Master device to define the number of devices supported by the EPROM.

In addition to providing the most significant addresses to the EPROM, the C15:12 address outputs from the master device must also drive the C15:12 inputs on the slave devices. These C15:12 inputs are internally compared to the C11:8 inputs to decide if that device is currently to be loaded. This approach avoids the need for external decoders and makes the $\overline{\text{CS}}$ input redundant. This input, however, must be tied low on every device in an EPROM supported system.

The Control Coefficient pin (CCS) is used to define when the control register is to be loaded. It becomes an output on the Master device which provides an EPROM address bit next in significance above A7:0, and also drives the CCS inputs on the slave devices. This output is high for the first two EPROM transfers in order to access the control information, and then remains low whilst the coefficients are loaded. This control information is thus not stored adjacent to the coefficients within the EPROM, and in fact the EPROM must provide twice the storage necessary to contain the coefficients alone. All but two of the bytes in the additional half are redundant. See Fig.17 for the EPROM memory map.



Control Register 14 13 12	Number of Coefficients Loaded
0 0 0	32
0 0 1	64
0 1 0	64
0 1 1	128
1 0 0	128
1 0 1	128
1 1 0	128
1 1 1	Invalid Mode

Table 5. Number of coefficients loaded

NOTE:
The EPROM memory map assumes that, for the 32 and 64 coefficient per device options, the unused address pins are unconnected. If all address pins are connected as shown in Fig. 16 then the 128 coefficients per device memory map column should be used. Only those coefficients required will be read, hence the upper portions of the coefficient address space will be ignored.

Figure. 17 EPROM Memory Map

Using a Remote Master

When a remote master is used to load coefficients, $\overline{\text{EPROM}}$ must be tied high and a conventional peripheral interface is then provided. It is not possible, however, to read coefficients already stored. The master supplies an address and data bus, and writes to the PDSP16256 occur under the control of synchronous $\overline{\text{CS}}$ and $\overline{\text{WEN}}$ inputs. The Coefficient Control Register pin (CCS) must be driven by a master address line higher in significance than A7:0. Both the $\overline{\text{WEN}}$ and $\overline{\text{CS}}$ signals must be low for the load operation to occur. When loading the control register the $\overline{\text{CS}}$ signal must be held low for a further 2 cycles, see Fig. 20. Since the internal write operation is actually performed with the system clock, it is necessary for the clock to be present during the transfer.

The $\overline{\text{BYTE}}$ input defines whether coefficients are loaded as a single 16 bit word or two 8-bit bytes. The latter saves on connections to the remote master. Address bits A7:0 are used in byte mode. 16-bit word mode uses bits A6:0, A7 being redundant. When writing in byte mode the least significant byte (A0 = 0) must be written first followed by the most significant byte (A0 = 1).
In byte mode the internal comparison between C15:12 and C11:8 is made, regardless of the state of $\overline{\text{EPROM}}$. For this reason pins C15:8 should all be tied low when a remote master is used with byte transfers. This ensures that the internal comparison gives equality and allows the load operation to occur.

The address and coefficient buses plus the $\overline{\text{WEN}}$ and $\overline{\text{CS}}$ signals must all meet the specified set up and hold times with respect to the system clock, see Fig 20 and Switching Characteristics. This synchronous interface is optimum for the majority of high end applications, when individual coefficients must be updated at sample clock rates. However, if the coefficients are to be loaded under software control from a general purpose microprocessor, the processor's $\overline{\text{WRITE STROBE}}$ will probably be asynchronous with the SCLK clock used by the PDSP16256. In this case external synchronising logic is needed, as shown in Fig.18.

Fig. 19 shows the recommended loading sequence and filter operation initiation. The simplest technique is to reset the device prior to loading a set of coefficients. Coefficients may be loaded once BUSY returns low or 22 cycles after $\overline{\text{RES}}$ is taken high.

When loading a device from a remote master the control register must be loaded first followed by the filter coefficients. Fig. 19 shows the required loading sequence, two examples are given one for byte mode the other for word mode. A gap of at least one cycle must be left after loading the control register before loading the first coefficient.

Filter operations are started by presenting the first data word at the same time as raising signal FEN; FRUN should always be low.

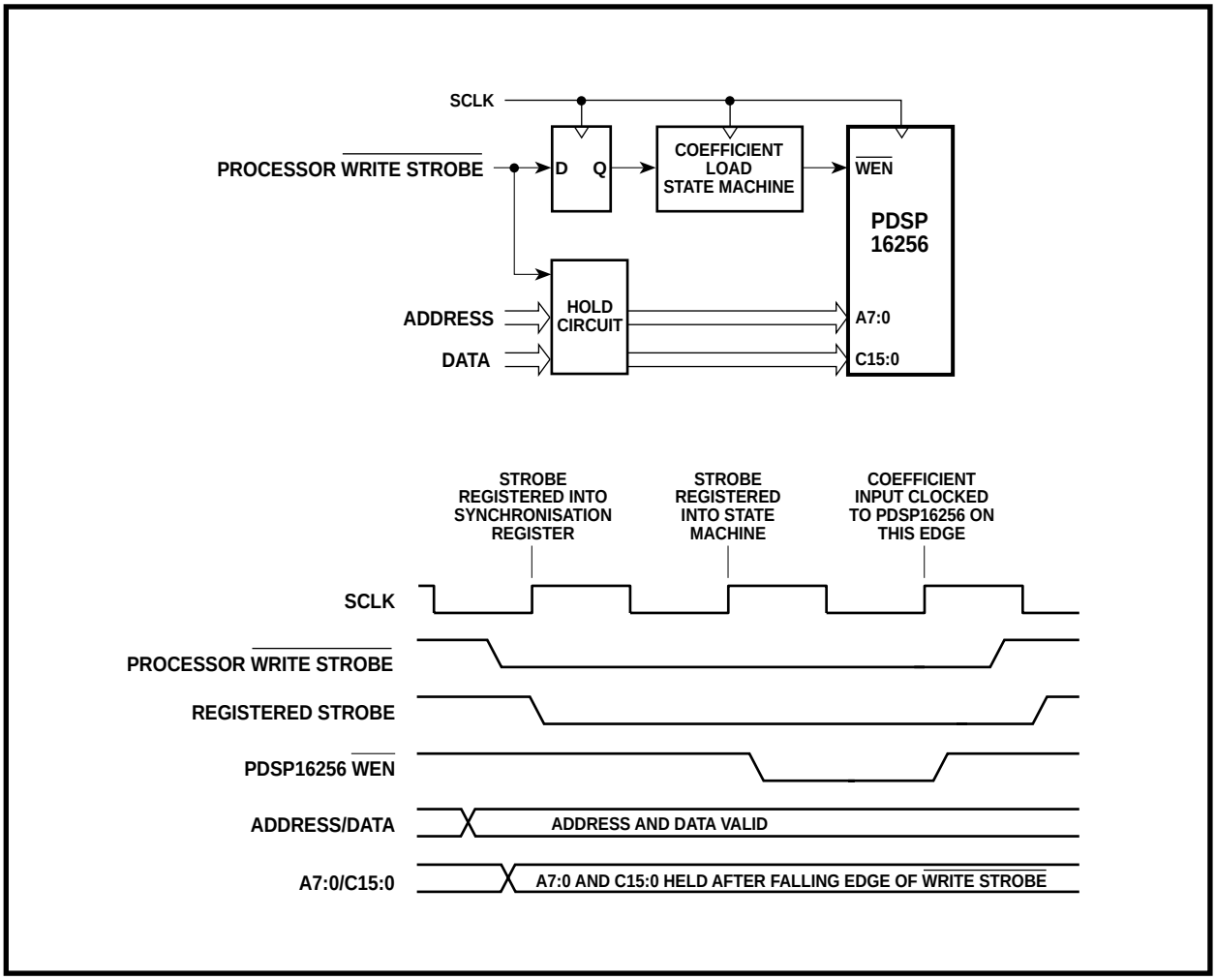


Figure. 18 Remote Master synchronisation

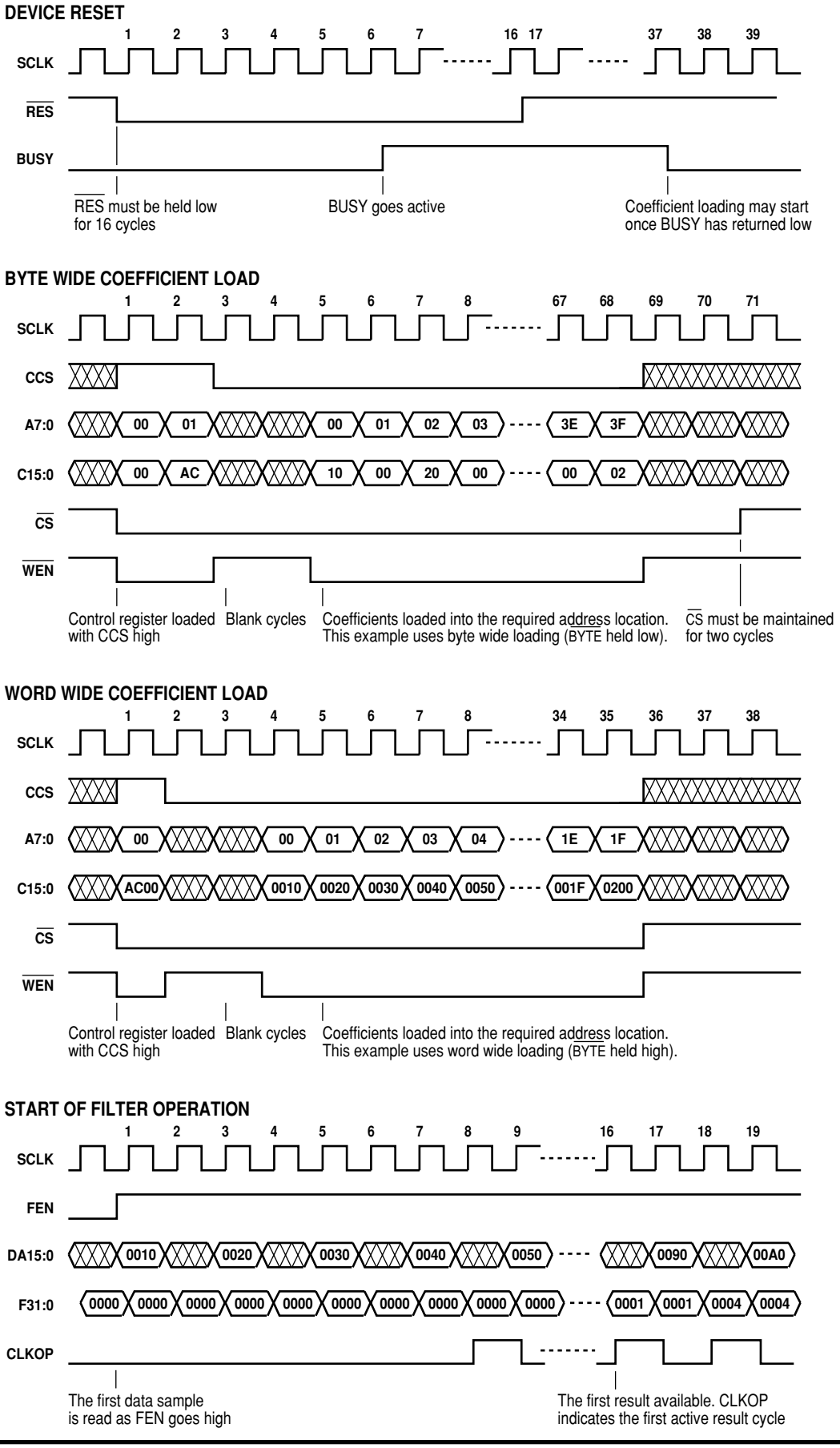


Figure. 19 Device startup timing diagrams

Control Register

The internal operation of the PDSP16256 is controlled by the status of a 16-bit control register. In the dual filter modes both networks are controlled by the same register. The significance of the various bits are shown in Table 6. Tables 7 and 8 define the control register bit interdependence for the filter and bank swapping modes.

The control register is double buffered. This allows the writing of a new control word without affecting the current operation of the device. To activate the new control register after it has been written to the device the bank swap signal must be toggled. After a reset the active control register is loaded directly and bank swap need not be used.

Bits	Decode	Function
15	0	Dual filter mode
15	1	Single filter mode
14:13	00	Sample rate is the system clock
14:13	01	Sample rate is half the system clock
14:13	10	Sample rate is quarter the system clock
14:13	11	Sample rate is eighth the system clock
12	0	Output rate equals the input rate
12	1	Decimate-by-two
11:10	00	Intermediate device
11:10	01	Interface device
11:10	10	Termination device
11:10	11	Single device
9:8	00	These bits MUST be at logical zero
7	0	Bank swap is controlled by input pin
7	1	Bank swap is controlled by Bit 6
6	0	Lower bank if bit 7 is set
6	1	Upper bank if bit 7 is set
5		This bit must be at logical zero
4	0	Two independent filters
4	1	Two filters in cascade
3:0		These bits MUST be at logical zero

Table 6 Control register bit allocation

Control Register Bits		Function
15	4	
0	0	Two independent filters
0	1	Two filters in cascade
1	X	Single Filter

Table 7 Control register filter mode bits

Control Register Bits			Function
7	6	5	
0	X	0	Control by input pin
1	0	0	Lower bank selected
1	1	0	Upper bank selected
X	X	1	Swap on every sample clock

Table 8 Control register bank swap bits

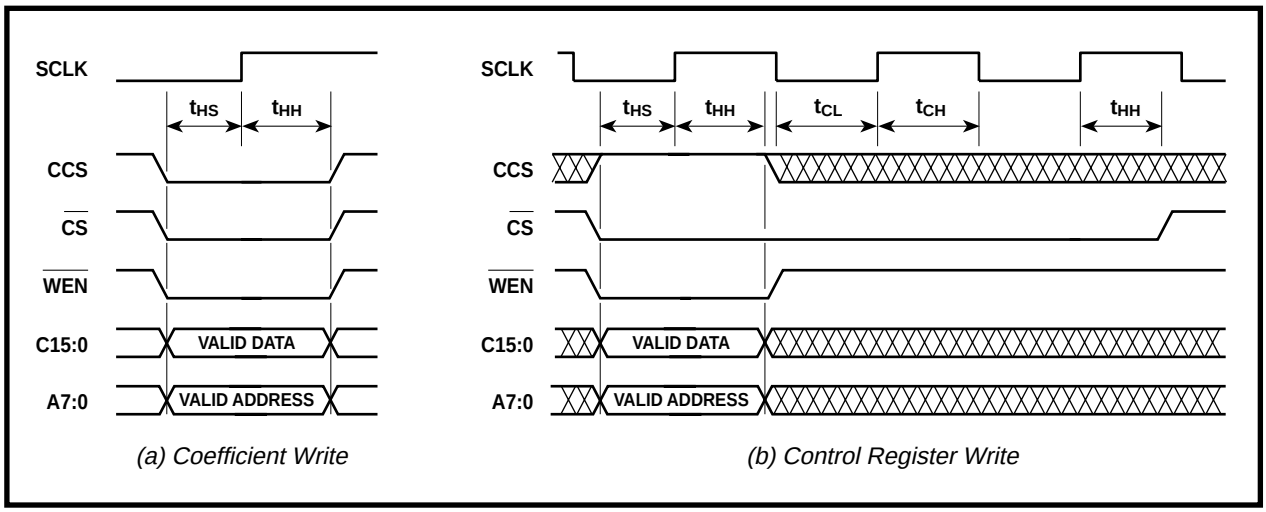


Figure. 20 Remote Master setup and hold timings

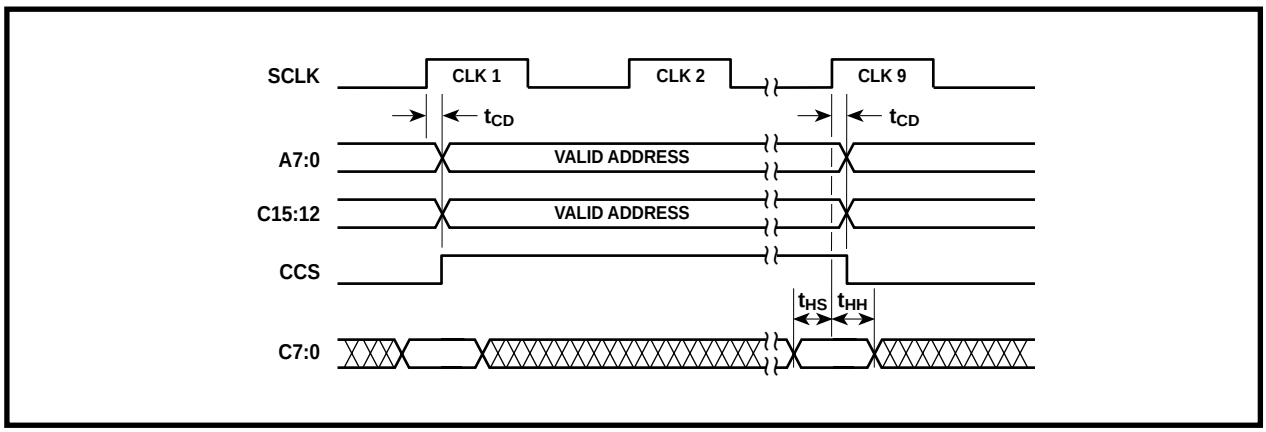


Figure. 21 EPROM load timings

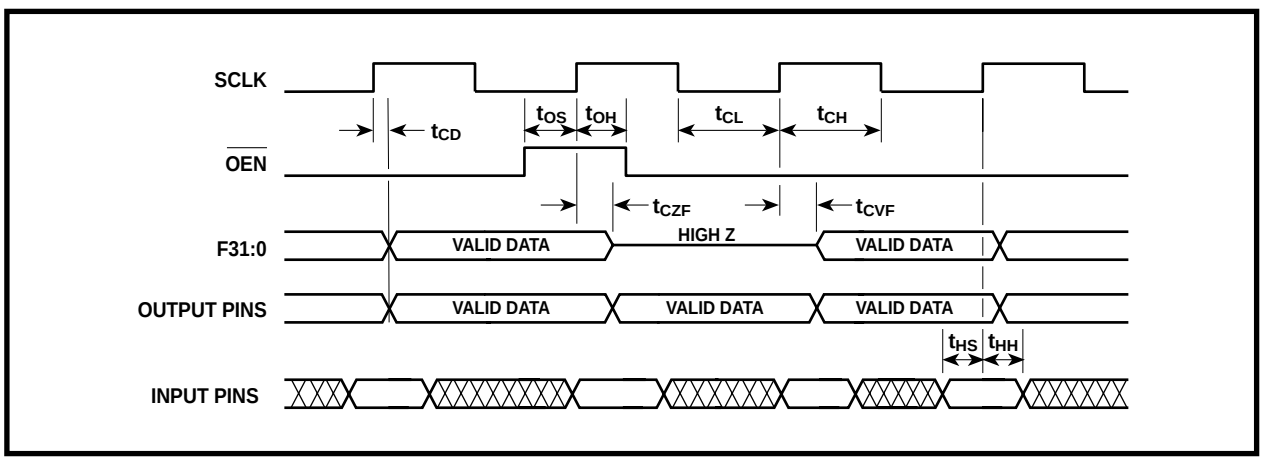


Figure. 22 Operating timings

Electrical Characteristics

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated:

Commercial: T_{AMB} = 0°C to+70°C, V_{DD} = +5V±5%, GND = 0V
IndustriaL: T_{AMB} = -40°C to +85°C, V_{DD} = +5V±10%, GND = 0V
Military: T_{AMB} = -55°C to +125°C, V_{DD} = +5V±10%, GND = 0V

Static Characteristics Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2·4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0·4	V	I_{OH} = 4mA
Input high voltage (CMOS)	V_{IH}	3·5		-	V	SCLK input only
Input low voltage (CMOS)	V_{IL}	-		1·0	V	SCLK input only
Input high voltage (TTL)	V_{IH}	2·0		-	V	All other inputs
Input low voltage (TTL)	V_{IL}	-		0·8	V	All other inputs
Input leakage current	I_{IN}	210		110	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	250		150	µA	GND < V_{OUT} < V_{DD}
Output short circuit current	I_{OS}	10		300	mA	V_{DD} = 15·5V

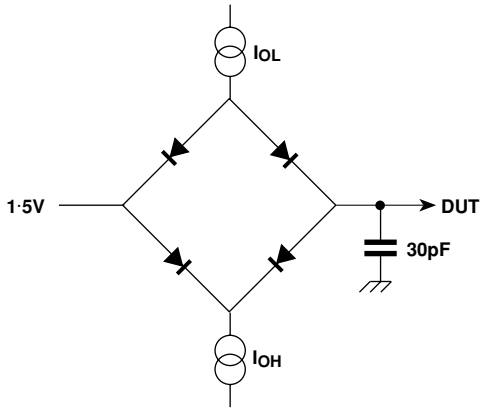
Switching Characteristics (see Figs. 20, 21 and 22)

Characteristic	Symbol	Commercial		Industrial		Military		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Input signal setup to clock rising edge	t_{HS}	8	-	8	-	8	-	ns	
Input signal hold after clock rising edge	t_{HH}	4	-	4	-	4	-	ns	
$\overline{OEN}$ set up to clock rising edge	t_{OS}	20	-	20	-	20	-	ns	
$\overline{OEN}$ hold after clock rising edge	t_{OH}	4	-	4	-	4	-	ns	
Clock rising edge to output signal valid	t_{CD}	5	26	5	28	5	28	ns	30pF
Clock frequency	f_{SCLK}	-	25	-	20	-	20	MHz	
Clock high time	t_{CH}	18	-	20	-	20	-	ns	
Clock low time	t_{CL}	11	-	12	-	12	-	ns	
Clock to data valid F bus from high impedance	t_{CVF}	-	30	-	30	-	30	ns	See Fig. 23
Clock to data high impedance F bus	t_{CZF}	-	30	-	30	-	30	ns	See Fig. 23
V_{DD} current	I_{DD}	-	400		380		380	mA	See Note 1

NOTE 1. V_{DD} = 15·5V, outputs unloaded, clock frequency = Max.

Test	Waveform measurement level
Delay from output high to output high impedance	V_H 0·5V
Delay from output low to output high impedance	V_L 0·5V
Delay from output high impedance to output low	1·5V 0·5V
Delay from output high impedance to output high	1·5V 0·5V

V_H is the voltage reached when the output is driven high
VL is the voltage reached when the output is driven low



Three state delay measurement load

Figure. 23 Three state delay measurement

Absolute Maximum Ratings (Note 1)

Supply voltage, V_{DD}	20·5V to 17·0V
Input voltage, V_{IN}	20·5V to V_{DD} 10·5V
Output voltage, V_{OUT}	20·5V to V_{DD} 10·5V
Clamp diode current per pin, I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature, T_S	265°C to1150°C
Maximum junction temperature, T_{JMAX}	
Commercial grade	1100°C
Industrial grade	1110°C
Military grade	1150°C
Package power dissipation	3000mW
Thermal resistance, Junction-to-Case, θ_{JC}	5°C/W

NOTES

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation should not be exceeded for more than 1 second, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.
5. The θ_{JC} data assumes that heat is extracted from the top of the package.
6. Maximum junction temperature, T_{JMAX}, is specified with power applied.

PDSP16256 MC AC1R and PDSP16256 MC GC1R (MIL-STD-883 PARTS)

Polyimide is used as an inter-layer dielectric as glassification. Polymeric material meeting the requirements of MIL-STD-883 test method 5011 is used for die attach.

Life tesst/burn-in connections are given in Tables 9 and 10 on the following pages.

Change Notification

The change notification requirements of MIL-PRF-38535 will be implemented on MIL-STD-883 grade devices. Known customers will be notified of any changes since the last buy when ordering further parts if significant changes have been made.

Rev.	A	B	C	D
Date	MAR 1993	SEPT 1995	JAN 1998	AUG 1998

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
A1	N/C	C8	15·0V/180k	H14	N/C	N12	15·0V
A2	0V/180k	C9	15·0V/180k	H15	N/C	N13	N/C
A3	0V/180k	C10	15·0V/180k	J1	0V	N14	N/C
A4	0V/180k	C11	15·0V/180k	J2	0V/180k	N15	N/C
A5	0V/180k	C12	15·0V/180k	J3	0V/180k	P1	15·0V/180k
A6	0V/180k	C13	0V	J13	N/C	P2	15·0V/180k
A7	15·0V	C14	N/C	J14	N/C	P3	15·0V
A8	0V/180k	C15	N/C	J15	0V	P4	15·0V
A9	0V	D1	N/C	K1	0V/180k	P5	0V
A10	15·0V/180k	D2	N/C	K2	0V/180k	P6	0V
A11	15·0V/180k	D3	N/C	K3	0V/180k	P7	15·0V
A12	15·0V/180k	D4	N/C	K13	N/C	P8	15·0V
A13	15·0V/180k	D13	N/C	K14	N/C	P9	15·0V
A14	15·0V/180k	D14	N/C	K15	N/C	P10	0V
A15	N/C	D15	N/C	L1	15·0V	P11	0V
B1	N/C	E1	N/C	L2	15·0V	P12	0V
B2	N/C	E2	N/C	L3	RESET	P13	N/C
B3	0V/180k	E3	N/C	L13	N/C	P14	0V
B4	0V/180k	E13	N/C	L14	N/C	P15	N/C
B5	0V/180k	E14	N/C	L15	N/C	R1	0V/180k
B6	0V/180k	E15	N/C	M1	CLOCK	R2	15·0V
B7	0V/180k	F1	N/C	M2	15·0V	R3	15·0V
B8	0V/180k	F2	N/C	M3	0V	R4	0V
B9	15·0V/180k	F3	N/C	M13	N/C	R5	0V
B10	15·0V/180k	F13	N/C	M14	N/C	R6	15·0V
B11	15·0V/180k	F14	N/C	M15	N/C	R7	15·0V
B12	15·0V/180k	F15	N/C	N1	0V	R8	15·0V
B13	15·0V/180k	G1	15·0V	N2	15·0V	R9	0V
B14	15·0V/180k	G2	N/C	N3	15·0V/180k	R10	15·0V
B15	N/C	G3	N/C	N4	15·0V	R11	0V
C1	N/C	G13	N/C	N5	15·0V	R12	0V
C2	N/C	G14	N/C	N6	0V	R13	0V
C3	N/C	G15	15·0V	N7	0V	R14	15·0V
C4	0V/180k	H1	15·0V/180k	N8	15·0V	R15	N/C
C5	0V/180k	H2	15·0V/180k	N9	15·0V		
C6	0V/180k	H3	15·0V/180k	N10	0V		
C7	0V/180k	H13	N/C	N11	0V		

Table 9 Life test/burn-in connections for PDSP16256 MC AC1R (PGA). NOTE: PDA is 5% and based on groups 1 and 7

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	N/C	44	15·0V	87	15·0V/180k	130	0V
2	N/C	45	0V	88	0V	131	N/C
3	N/C	46	15·0V	89	0V	132	0V/180k
4	N/C	47	N/C	90	15·0V	133	15·0V
5	15·0V	48	15·0V	91	0V	134	0V/180k
6	N/C	49	0V	92	15·0V	135	0V/180k
7	N/C	50	0V	93	15·0V	136	0V/180k
8	0V	51	0V	94	RESET	137	0V/180k
9	N/C	52	0V	95	CLOCK	138	0V/180k
10	N/C	53	0V	96	0V	139	0V/180k
11	N/C	54	0V	97	15·0V	140	0V
12	N/C	55	0V	98	15·0V	141	0V/180k
13	N/C	56	0V	99	15·0V	142	0V/180k
14	N/C	57	0V	100	0V/180k	143	15·0V
15	N/C	58	15·0V	101	0V/180k	144	0V/180k
16	0V	59	15·0V	102	0V/180k	145	0V/180k
17	N/C	60	15·0V	103	0V/180k	146	0V/180k
18	N/C	61	15·0V	104	0V/180k	147	0V/180k
19	N/C	62	15·0V	105	15·0V	148	0V/180k
20	15·0V	63	15·0V	106	15·0V/180k	149	0V/180k
21	N/C	64	15·0V	107	15·0V/180k	150	0V
22	N/C	65	15·0V	108	0V	151	0V/180k
23	N/C	66	15·0V	109	15·0V/180k	152	15·0V/180k
24	N/C	67	0V	110	N/C	153	15·0V/180k
25	15·0V	68	0V	111	N/C	154	15·0V/180k
26	N/C	69	0V	112	N/C	155	15·0V/180k
27	N/C	70	0V	113	0V	156	15·0V/180k
28	0V	71	0V	114	N/C	157	15·0V/180k
29	N/C	72	0V	115	N/C	158	15·0V/180k
30	N/C	73	0V	116	N/C	159	0V
31	N/C	74	15·0V	117	N/C	160	15·0V/180k
32	N/C	75	15·0V	118	N/C	161	15·0V/180k
33	N/C	76	15·0V	119	15·0V	162	15·0V/180k
34	N/C	77	15·0V	120	N/C	163	15·0V
35	N/C	78	15·0V	121	N/C	164	15·0V/180k
36	0V	79	15·0V	122	N/C	165	15·0V/180k
37	N/C	80	0V	123	N/C	166	15·0V/180k
38	N/C	81	15·0V	124	N/C	167	15·0V/180k
39	N/C	82	15·0V/180k	125	N/C	168	15·0V/180k
40	15·0V	83	15·0V/180k	126	N/C	169	0V
41	0V	84	15·0V	127	0V	170	15·0V/180k
42	N/C	85	0V	128	N/C	171	15·0V
43	N/C	86	0V/180k	129	15·0V	172	0V

Table 10 Life test/burn-in connections for PDSP16256 MC GC1R (QFP). NOTE: PDA is 5% and based on groups 1 and 7



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