# BCM® Bus Converter
## BCM384x120y800ACz



## Fixed Ratio DC-DC Converter

### Features

- Up to 800 W continuous output power
- 1177 W/in$^3$ power density
- 97.4% peak efficiency
- 4,242 Vdc isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 2361 through-hole ChiP package
  - 2.402" x 0.990" x 0.286"
    (61.00 mm x 25.14 mm x 7.26 mm)

### Typical Applications

- 380 DC Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

| Product Ratings | |
|---|---|
| $V_{PRI}$ = 384 V (260 – 410 V) | $P_{SEC}$= up to 800 W |
| $V_{SEC}$ = 12 V (8.1 – 12.8 V) (NO LOAD) | K = 1/32 |

### Product Description

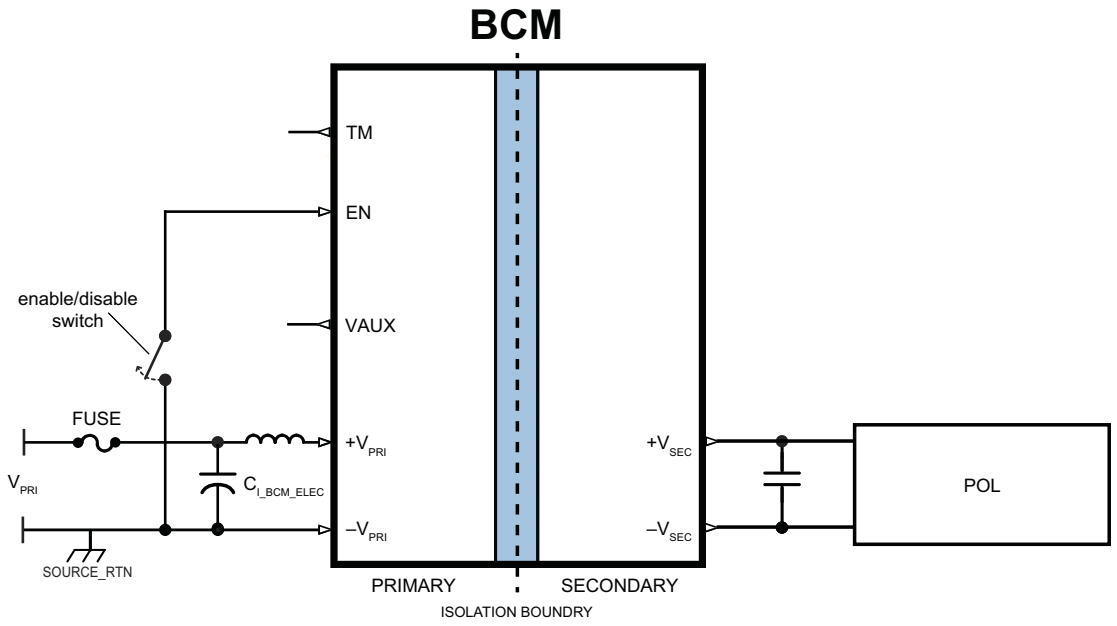
The VI Chip® Bus Converter (BCM®) is a high efficiency Sine Amplitude Converter™ (SAC™), operating from a 260 to 410 VDC primary bus to deliver an isolated, ratiometric output from 8.1 to 12.8 VDC.

The BCM384x120y800ACz offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the primary side of the BCM module. With a primary to secondary K factor of 1/32, that capacitance value can be reduced by a factor of 1024x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

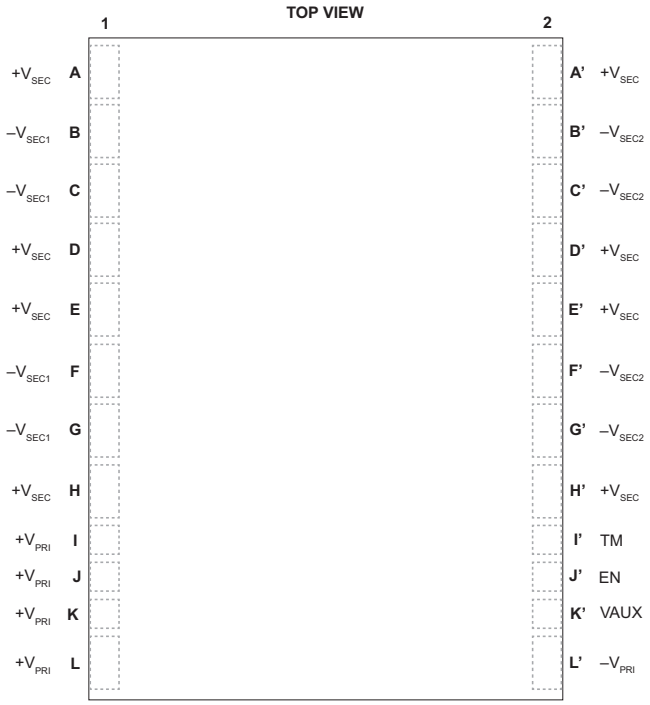
This product can operate in reverse direction, at full rated power, after being previously started in forward direction.

## Typical Application




BCM384x120y800ACz+ Point of Load

## Pin Configuration




**2361 ChiP Package**

## Pin Descriptions

| Pin Number | Signal Name | Type | Function |
|---|---|---|---|
| I1, J1, K1, L1 | $+V_{PRI}$ | PRIMARY POWER | Positive primary transformer power terminal |
| I'2 | TM | OUTPUT | Temperature Monitor; Primary side referenced signals |
| J'2 | EN | INPUT | Enables and disables power supply; Primary side referenced signals |
| K'2 | VAUX | OUTPUT | Auxilary Voltage Source; Primary side referenced signals |
| L'1 | $-V_{PRI}$ | PRIMARY POWER RETURN | Negative Primary transformer power terminal |
| A1, D1, E1, H1, A'2, D'2, E'2, H'2 | $+V_{SEC}$ | SECONDARY POWER | Positive secondary transformer power terminal |
| B1, C1, F1, G1, B'2, C'2, F'2, G'2 | $-V_{SEC*}$ | SECONDARY POWER RETURN | Negative secondary transformer power terminal |

*For proper operation an external low impedance connection must be made between listed $-V_{SEC1}$ and $-V_{SEC2}$ terminals.

## Part Ordering Information

| Device | Input Voltage Range | Package Type | Output Voltage x 10 | Temperature Grade | Output Power | Revision | Package Size | Version |
|---|---|---|---|---|---|---|---|---|
| BCM | 384 | x | 120 | y | 800 | A | C | z |
| BCM = BCM | 384 = 260 to 410 V | P = ChiP Through Hole | 120 = 12 V | T = -40 to 125°C<br>M = -55 to 125°C | 800 = 800 W | A | C = 2361 | 0 = Analog<br>R = Reversible |

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

## Standard Models

| Part Number | $V_{IN}$ | Package Type | $V_{OUT}$ | Temperature | Power | Package Size |
|---|---|---|---|---|---|---|
| BCM384**P**120**T**800AC0 | 260 to 410 V | ChiP Through Hole | 12 V<br>8.1 to 12.8 V | -40°C to 125°C | 800 W | 2361 |
| BCM384**P**120**M**800AC0 | 260 to 410 V | ChiP Through Hole | 12 V<br>8.1 to 12.8 V | -55°C to 125°C | 800 W | 2361 |
| BCM384**P**120**T**800ACR | 260 to 410 V | ChiP Through Hole | 12 V<br>8.1 to 12.8 V | -40°C to 125°C | 800 W | 2361 |
| BCM384**P**120**M**800ACR | 260 to 410 V | ChiP Through Hole | 12 V<br>8.1 to 12.8 V | -55°C to 125°C | 800 W | 2361 |

## Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|---|---|---|---|---|
| $+V_{PRI_DC}$ to $-V_{PRI_DC}$ | | -1 | 480 | V |
| $V_{PRI_DC}$ or $V_{SEC_DC}$ slew rate (operational) | | | 1 | V/µs |
| $+V_{SEC_DC}$ to $-V_{SEC_DC}$ | | -1 | 15 | V |
| TM to $-V_{PRI_DC}$ | | -0.3 | 4.6 | V |
| EN to $-V_{PRI_DC}$ | | | 5.5 | V |
| VAUX to $-V_{PRI_DC}$ | | | 4.6 | V |

## Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain PRIMARY to SECONDARY Specification (Forward Direction)** | | | | | | |
| Primary Input Voltage range, continuous | $V_{PRI_DC}$ | | **260** | | **410** | V |
| $V_{PRI}$ µController | $V_{\mu C_ACTIVE}$ | $V_{PRI_DC}$ voltage where µC is initialized, (ie VAUX = Low, powertrain inactive) | | | 130 | V |
| PRI to SEC Input Quiescent Current | $I_{PRI_Q}$ | Disabled, EN Low, $V_{PRI_DC}$ = 384 V | | 2 | | mA |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 4 | |
| PRI to SEC No Load Power Dissipation | $P_{PRI_NL}$ | $V_{PRI_DC}$ = 384 V, $T_{INTERNAL}$ = 25°C | | 9.3 | 13 | W |
| | | $V_{PRI_DC}$ = 384 V | **5** | | **20** | |
| | | $V_{PRI_DC}$ = 260 V to 410 V, $T_{INTERNAL}$ = 25 °C | | | 16 | |
| | | $V_{PRI_DC}$ = 260 V to 410 V | | | **22** | |
| PRI to SEC Inrush Current Peak | $I_{PRI_INR_PK}$ | $V_{PRI_DC}$ = 410 V, $C_{SEC_EXT}$ = 1000 µF, $R_{LOAD_SEC}$ = 50% of full load current | | 10 | | A |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 15 | |
| DC Primary Input Current | $I_{PRI_IN_DC}$ | At $I_{SEC_OUT_DC}$ = 68 A, $T_{INTERNAL}$ ≤ 100°C | | | 2.2 | A |
| Transformation Ratio | K | Primary to secondary, K = $V_{SEC_DC}$ / $V_{PRI_DC}$, at no load | | 1/32 | | V/V |
| Secondary Output Power (continuous) | $P_{SEC_OUT_DC}$ | Specified at $V_{PRI_DC}$ = 410 V | | | 800 | W |
| Secondary Output Power (pulsed) | $P_{SEC_OUT_PULSE}$ | Specified at $V_{PRI_DC}$ = 410 V; 10 ms pulse, 25% Duty cycle, $P_{SEC_AVG}$ = 50% rated $P_{SEC_OUT_DC}$ | | | 1100 | W |
| Secondary Output Current (continuous) | $I_{SEC_OUT_DC}$ | | | | 68 | A |
| Secondary Output Current (pulsed) | $I_{SEC_OUT_PULSE}$ | 10 ms pulse, 25% Duty cycle, $I_{SEC_OUT_AVG}$ = 50% rated $I_{SEC_OUT_DC}$ | | | 91 | A |
| PRI to SEC Efficiency (ambient) | $\eta_{AMB}$ | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 68 A | 96.2 | 97.2 | | % |
| | | $V_{PRI_DC}$ = 260 V to 410 V, $I_{SEC_OUT_DC}$ = 68 A | 95.7 | | | |
| | | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 34 A | 96.3 | 97 | | |
| PRI to SEC Efficiency (hot) | $\eta_{HOT}$ | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 68 A | 96 | 97 | | % |
| PRI to SEC Efficiency (over load range) | $\eta_{20\%}$ | 14 A < $I_{SEC_OUT_DC}$ < 68 A | 90 | | | % |
| PRI to SEC Output Resistance | $R_{SEC_COLD}$ | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 68 A, $T_{INTERNAL}$ = -40°C | 1.0 | 1.65 | 2.2 | mΩ |
| | $R_{SEC_AMB}$ | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 68 A | 1.6 | 2.3 | 2.9 | |
| | $R_{SEC_HOT}$ | $V_{PRI_DC}$ = 384 V, $I_{SEC_OUT_DC}$ = 384 A, $T_{INTERNAL}$ = 100°C | 2.3 | 2.9 | 3.4 | |
| Switching Frequency | $F_{SW}$ | Frequency of the Output Voltage Ripple = 2x FSW | **0.97** | 1.03 | **1.09** | MHz |
| Secondary Output Voltage Ripple | $V_{SEC_OUT_PP}$ | $C_{SEC_EXT}$ = 0 µF, $I_{SEC_OUT_DC}$ = 68 A, $V_{PRI_DC}$ = 384 V, 20 MHz BW | | 210 | | mV |
| | | $T_{INTERNAL}$ ≤ 100°C | | | 300 | |
| Primary Input Leads Inductance (Parasitic) | $L_{PRI_IN_LEADS}$ | Frequency 2.5 MHz (double switching frequency), Simulated lead model | | 7 | | nH |
| Secondary Output Leads Inductance (Parasitic) | $L_{SEC_OUT_LEADS}$ | Frequency 2.5 MHz (double switching frequency), Simulated lead model | | 0.64 | | nH |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain PRIMARY to SECONDARY Specification (Forward Direction) Cont.** | | | | | | |
| Effective Primary Capacitance (Internal) | $C_{PRI_INT}$ | Effective Value at 384 $V_{PRI_DC}$ | | 0.25 | | µF |
| Effective Secondary Capacitance (Internal) | $C_{SEC_INT}$ | Effective Value at 12 $V_{SEC_DC}$ | | 104 | | µF |
| Effective Secondary Output Capacitance (External) | $C_{SEC_OUT_EXT}$ | Excessive capacitance may drive module into SC protection | | | **1000** | µF |
| Effective Secondary Output Capacitance (External) | $C_{SEC_OUT_AEXT}$ | $C_{SEC_OUT_AEXT}$ Max = N * 0.5 * $C_{SEC_OUT_EXT\ MAX}$, where N = the number of units in parallel | | | | |
| **Protection PRIMARY to SECONDARY (Forward Direction)** | | | | | | |
| Auto Restart Time | $t_{AUTO_RESTART}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{PRI_DC}$ > $V_{PRI_UVLO+}$ | **292.5** | | **357.5** | ms |
| Primary Overvoltage Lockout Threshold | $V_{PRI_OVLO+}$ | | **420** | 434.5 | **450** | V |
| Primary Overvoltage Recovery Threshold | $V_{PRI_OVLO-}$ | | **410** | 424 | **440** | V |
| Primary Overvoltage Lockout Hysteresis | $V_{PRI_OVLO_HYST}$ | | | 10.5 | | V |
| Primary Overvoltage Lockout Response Time | $t_{PRI_OVLO}$ | | | 100 | | µs |
| Primary Undervoltage Lockout Threshold | $V_{PRI_UVLO-}$ | | **195** | 221 | **250** | V |
| Primary Undervoltage Recovery Threshold | $V_{PRI_UVLO+}$ | | **225** | 243 | **255** | V |
| Primary Undervoltage Lockout Hysteresis | $V_{PRI_UVLO_HYST}$ | | | 15 | | V |
| Primary Undervoltage Lockout Response Time | $t_{PRI_UVLO}$ | | | 100 | | µs |
| Primary Undervoltage Startup Delay | $t_{PRI_UVLO+_DELAY}$ | From $V_{PRI_DC}$ = $V_{PRI_UVLO+}$ to powertrain active, EN floating, (i.e One time Startup delay form application of $V_{PRI_DC}$ to $V_{SEC_DC}$) | | 20 | | ms |
| Primary Soft-Start Time | $t_{PRI_SOFT-START}$ | From powertrain active. Fast Current limit protection disabled during Soft-Start | | 1 | | ms |
| Secondary Output Overcurrent Trip Threshold | $I_{SEC_OUT_OCP}$ | | **75** | 85 | **110** | A |
| Secondary Output Overcurrent Response Time Constant | $t_{SEC_OUT_OCP}$ | Effective internal RC filter | | 3 | | ms |
| Secondary Output Short Circuit Protection Trip Threshold | $I_{SEC_OUT_SCP}$ | | **105** | | | A |
| Secondary Output Short Circuit Protection Response Time | $t_{SEC_OUT_SCP}$ | | | 1 | | µs |
| Overtemperature Shutdown Threshold | $t_{OTP+}$ | Temperature sensor located inside controller IC | **125** | | | °C |
| Overtemperature Recovery Threshold | $t_{OTP–}$ | | 105 | 110 | 115 | °C |
| Undertemperature Shutdown Threshold | $t_{UTP}$ | Temperature sensor located inside controller IC; Protection not available for M-Grade units. | | | -45 | °C |
| Undertemperature Restart Time | $t_{UTP_RESTART}$ | Startup into a persistent fault condition. Non-Latching fault detection given $V_{PRI_DC}$ > $V_{PRI_UVLO+}$ | | 3 | | s |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **General Powetrain SECONDARY to PRIMARY Specification (Reverse Direction)** | | | | | | |
| Secondary Input Voltage range, continuous | $V_{SEC_DC}$ | | **8.1** | | **12.8** | V |
| SEC to PRI No Load Power Dissipation | $P_{SEC_NL}$ | $V_{SEC_DC}$ = 12 V, $T_{INTERNAL}$ = 25°C | | 9.3 | 13 | W |
| | | $V_{SEC_DC}$ = 12 V | **5** | | **20** | |
| | | $V_{SEC_DC}$ = 8.1 V to 12.8 V, $T_{INTERNAL}$ = 25°C | | | 16 | |
| | | $V_{SEC_DC}$ = 8.1 V to 12.8 V | | | **22** | |
| DC Secondary Input Current | $I_{SEC_IN_DC}$ | At $I_{PRI_DC}$ = 2.1 A, $T_{INTERNAL}$ ≤ 100°C | | | **70** | A |
| Primary Ouptut Power (continuous) | $P_{PRI_OUT_DC}$ | Specified at $V_{SEC_DC}$ = 12.8 V | | | **800** | W |
| Primary Output Power (pulsed) | $P_{PRI_OUT_PULSE}$ | Specified at $V_{SEC_DC}$ = 12.8 V; 10 ms pulse, 25% Duty cycle, $P_{PRI_AVG}$ = 50% rated $P_{PRI_OUT_DC}$ | | | **1100** | W |
| Primary Output Current (continuous) | $I_{PRI_OUT_DC}$ | | | | **2.1** | A |
| Primary Output Current (pulsed) | $I_{PRI_OUT_PULSE}$ | 10 ms pulse, 25% Duty cycle, $I_{PRI_OUT_AVG}$ = 50% rated $I_{PRI_OUT_DC}$ | | | **2.9** | A |
| SEC to PRI Efficiency (ambient) | $\eta_{AMB}$ | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 2.1 A | 96.2 | 97.2 | | % |
| | | $V_{SEC_DC}$ = 8.1 V to 12.8 V, $I_{PRI_OUT_DC}$= 2.1 A | 95.6 | | | |
| | | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 1.05 A | 96.3 | 97 | | |
| SEC to PRI Efficiency (hot) | $\eta_{HOT}$ | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 2.1 A | 96 | 97 | | % |
| SEC to PRI Efficiency (over load range) | $\eta_{20\%}$ | 0.42 A < $I_{PRI_OUT_DC}$ < 2.1 A | **90** | | | % |
| SEC to PRI Output Resistance | $R_{PRI_COLD}$ | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 2.1 A, $T_{INTERNAL}$ = -40°C | 3000 | 3300 | 3600 | mΩ |
| | $R_{PRI_AMB}$ | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 2.1 A | 3600 | 3950 | 4300 | |
| | $R_{PRI_HOT}$ | $V_{SEC_DC}$ = 12 V, $I_{PRI_OUT_DC}$ = 2.1 A, $T_{INTERNAL}$ = 100°C | 4300 | 4600 | 4900 | |
| Primary Output Voltage Ripple | $V_{PRI_OUT_PP}$ | $C_{PRI_OUT_EXT}$ = 0 µF, $I_{PRI_OUT_DC}$ = 2.1 A, $V_{SEC_DC}$ = 12 V, 20 MHz BW | | 6700 | | mV |
| | | $T_{INTERNAL}$ ≤ 100°C | | | **9600** | |

## Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Protection SECONDARY to PRIMARY (Reverse Direction)** | | | | | | |
| Secondary Overvoltage Lockout Threshold | $V_{SEC_OVLO+}$ | Module latched shutdown with $V_{PRI_DC}$ < $V_{PRI_UVLO-_R}$ | **13.1** | 13.6 | **14.1** | V |
| Secondary Overvoltage Lockout Response Time | $t_{PRI_OVLO}$ | | | 100 | | µs |
| Secondary Undervoltage Lockout Threshold | $V_{SEC_UVLO-}$ | Module latched shutdown with $V_{PRI_DC}$ < $V_{PRI_UVLO-_R}$ | **3.4** | 3.75 | **4.1** | V |
| Secondary Undervoltage Lockout Response Time | $t_{SEC_UVLO}$ | | | 100 | | µs |
| Primary Undervoltage Lockout Threshold | $V_{PRI_UVLO-_R}$ | Applies only to reversilbe products in forward and in reverse direction; $I_{PRI_DC}$ ≤ 20 while $V_{PRI_UVLO-_R}$ < $V_{PRI_DC}$ < $V_{PRI_MIN}$ | **110** | 120 | **130** | V |
| Primary Undervoltage Recovery Threshold | $V_{PRI_UVLO+_R}$ | Applies only to reversilbe products in forward and in reverse direction; | **120** | 130 | **150** | V |
| Primary Undervoltage Lockout Hysteresis | $V_{PRI_UVLO_HYST_R}$ | Applies only to reversilbe products in forward and in reverse direction; | | 10 | | V |
| Primary Output Overcurrent Trip Threshold | $I_{PRI_OUT_OCP}$ | Module latched shutdown with $V_{PRI_DC}$ < $V_{PRI_UVLO-_R}$ | **2.3** | 2.7 | **3.4** | A |
| Primary Output Overcurrent Response Time Constant | $t_{PRI_OUT_OCP}$ | Effective internal RC filter | | 3 | | ms |
| Primary Short Circuit Protection Trip Threshold | $I_{PRI_SCP}$ | Module latched shutdown with $V_{PRI_DC}$ < $V_{PRI_UVLO-_R}$ | **3.3** | | | A |
| Primary Short Circuit Protection Response Time | $t_{PRI_SCP}$ | | | 1 | | µs |

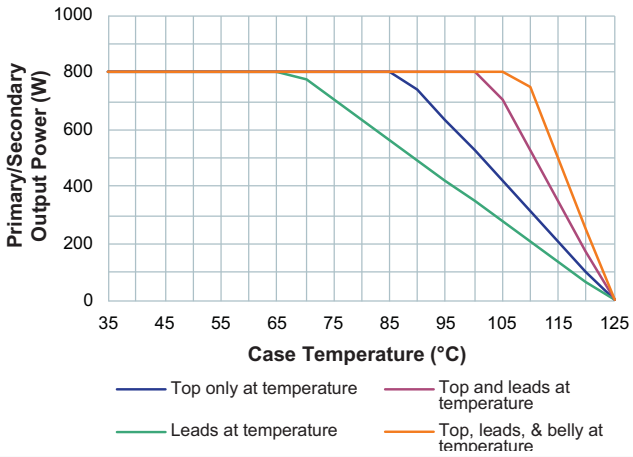



***Figure 1*** — *Specified thermal operating area*

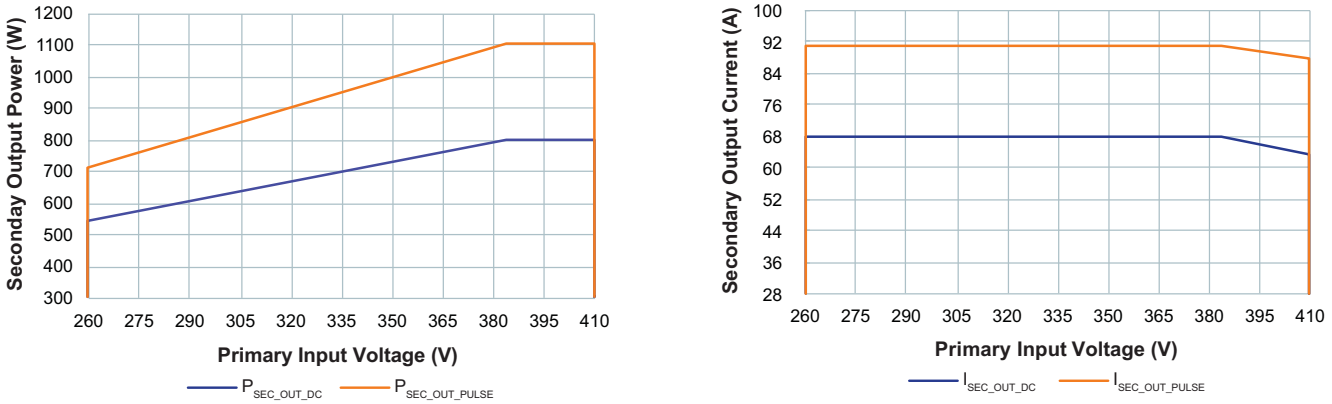



***Figure 2*** — *Specified electrical operating area using rated $R_{SEC_HOT}$*

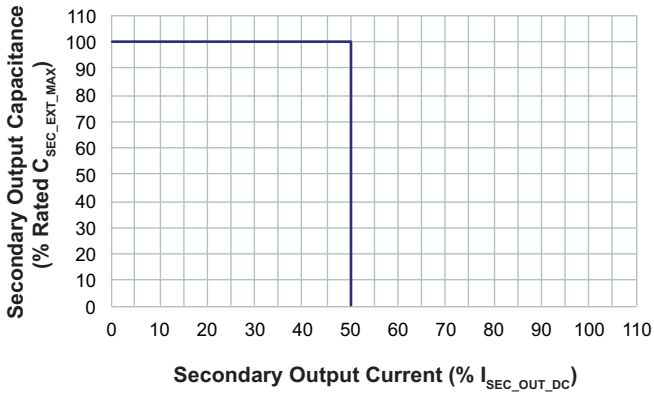



***Figure 3*** — *Specified Primary start-up into load current and external capacitance*

## Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Temperature Monitor | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| • The TM pin is a standard analog I/O configured as an output from an internal µC.<br>• The TM pin monitors the internal temperature of the controller IC within an accuracy of ±5°C.<br>• µC 250 kHz PWM output internally pulled high to 3.3 V. | | | | | | | | |
| **SIGNAL TYPE** | **STATE** | **ATTRIBUTE** | **SYMBOL** | **CONDITIONS / NOTES** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **DIGITAL OUTPUT** | Startup | Powertrain active to TM time | $t_{TM}$ | | | **100** | | µs |
| | Regular Operation | TM Duty Cycle | $TM_{PWM}$ | | **18.18** | | **68.18** | % |
| | | TM Current | $I_{TM}$ | | | | **4** | mA |
| | | **Recommended External filtering** | | | | | | |
| | | TM Capacitance (External) | $C_{TM_EXT}$ | Recommended External filtering | | 0.01 | | µF |
| | | TM Resistance (External) | $R_{TM_EXT}$ | Recommended External filtering | | 1 | | kΩ |
| | | **Specifications using recommended filter** | | | | | | |
| | | TM Gain | $A_{TM}$ | | | 10 | | mV / °C |
| | | TM Voltage Reference | $V_{TM_AMB}$ | | | 1.27 | | V |
| | | TM Voltage Ripple | $V_{TM_PP}$ | $R_{TM_EXT}$ = 1 K Ohm, $C_{TM_EXT}$ = 0.01 uF, $V_{PRI_DC}$ = 384 V, $I_{SEC_DC}$ = 68 A | | 28 | | mV |
| | | | | $T_{INTERNAL}$ ≤ 100°C | | | 40 | |

| Enable / Disable Control | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| • The EN pin is a standard analog I/O configured as an input to an internal µC.<br>• It is internally pulled high to 3.3 V.<br>• When held low the BCM internal bias will be disabled and the powertrain will be inactive.<br>• In an array of BCMs, EN pins should be interconnected to synchronize startup and permit startup into full load conditions. | | | | | | | | |
| **SIGNAL TYPE** | **STATE** | **ATTRIBUTE** | **SYMBOL** | **CONDITIONS / NOTES** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **ANALOG INPUT** | Startup | EN to Powertrain active time | $t_{EN_START}$ | $V_{PRI_DC}$ > $V_{PRI_UVLO+}$, EN held low both conditions satisfied for T > $t_{PRI_UVLO+_DELAY}$ | | **250** | | µs |
| | Regular Operation | EN Voltage Threshold | $V_{EN_TH}$ | | **2.3** | | | V |
| | | EN Resistance (Internal) | $R_{EN_INT}$ | Internal pull up resistor | | 1.5 | | kΩ |
| | | EN Disable Threshold | $V_{EN_DISABLE_TH}$ | | | | **1** | V |

## Signal Characteristics (Cont.)

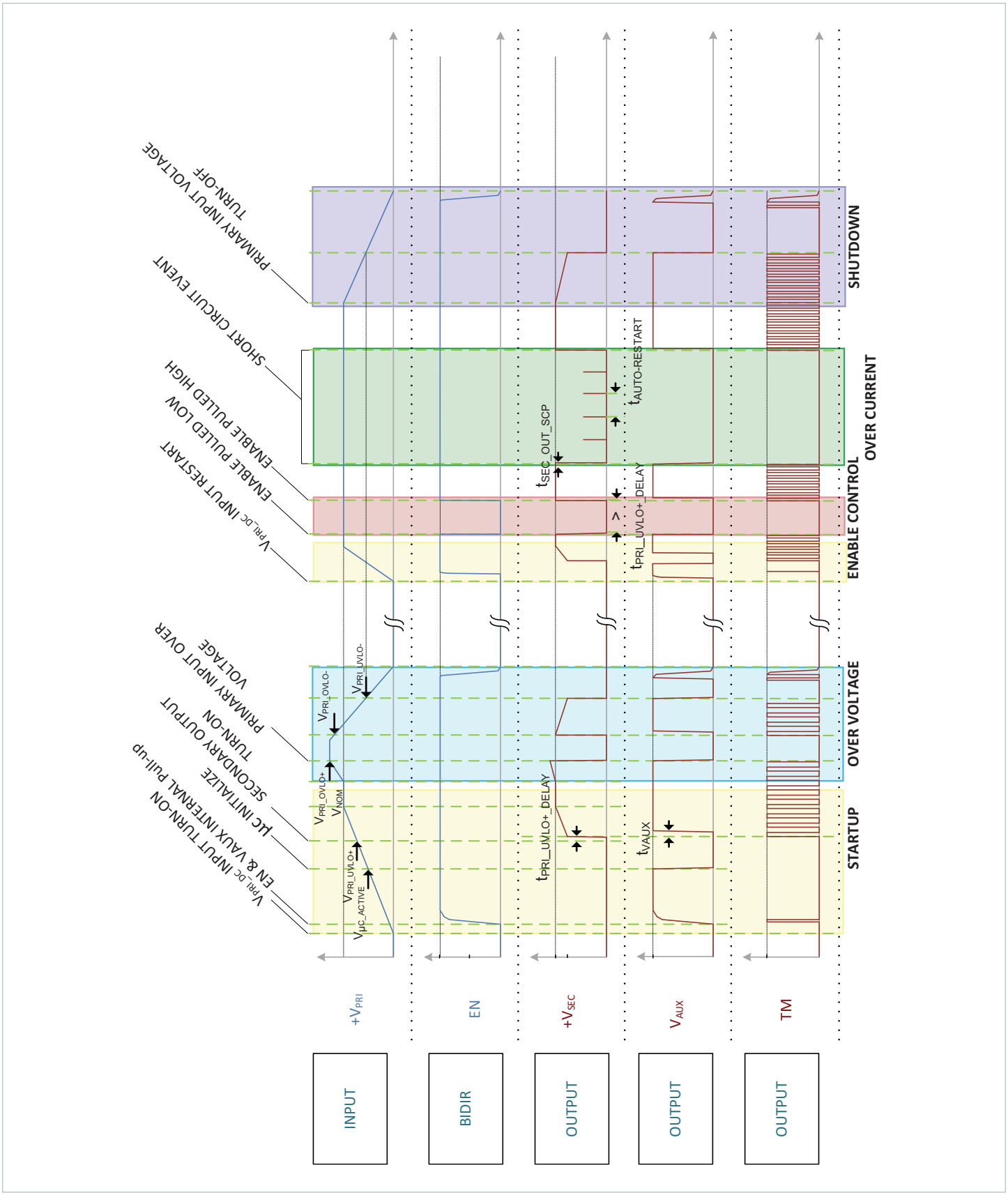
Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

**Auxiliary Voltage Source**

- The VAUX pin is a standard analog I/O configured as an output from an internal µC.
- VAUX is internally connected to µC output as internally pulled high to a 3.3 V regulator with 2% tolerance, a 1% resistor of 1.5 kΩ.
- VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2 ms delay from the start of powertrain activating, signaling the end of softstart.
- VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected.

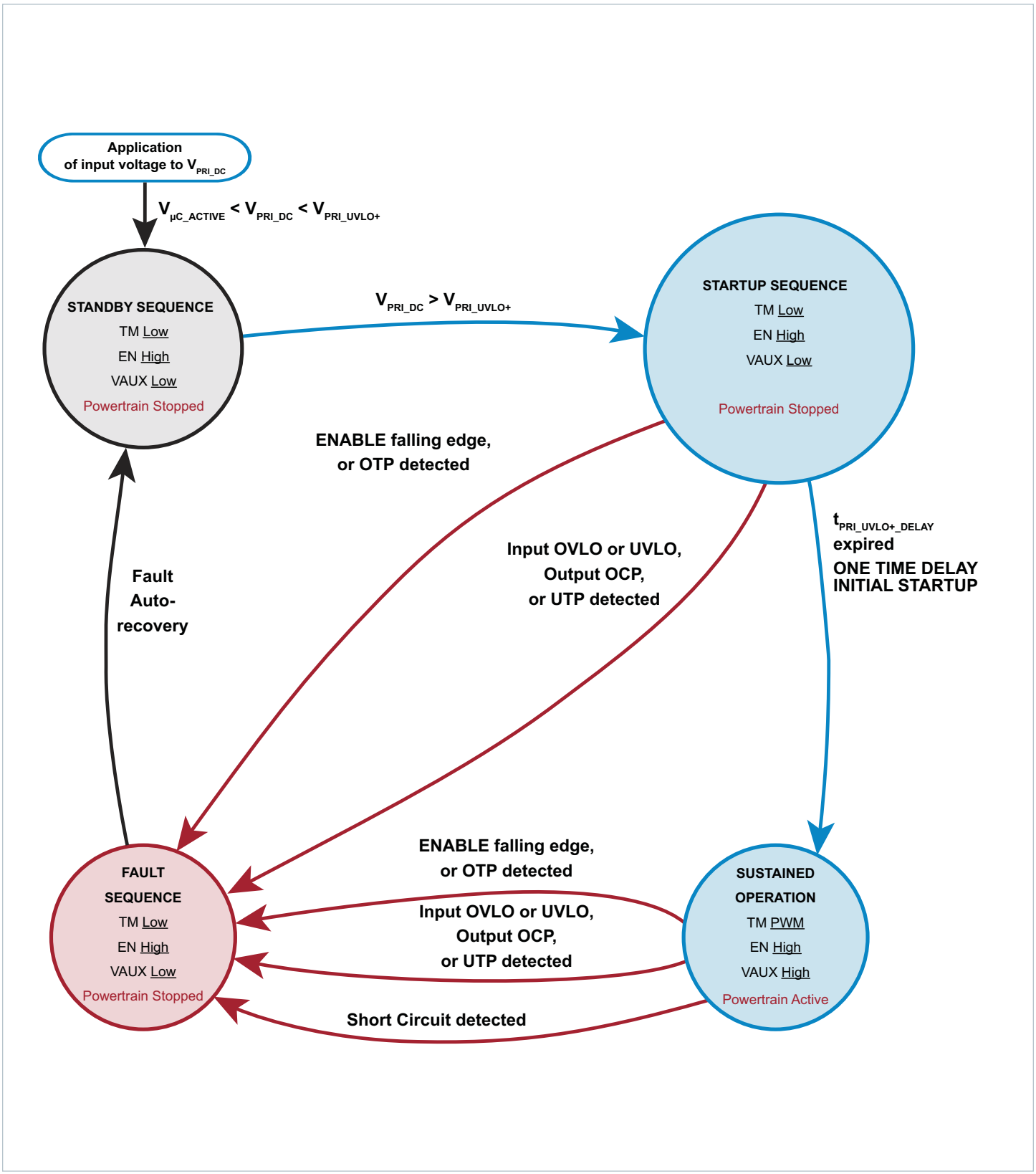
| SIGNAL TYPE | STATE | ATTRIBUTE | SYMBOL | CONDITIONS / NOTES | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| ANALOG OUTPUT | Startup | Powertrain active to VAUX time | $t_{VAUX}$ | Powertrain active to VAUX High | | **2** | | ms |
| | Regular Operation | VAUX Voltage | $V_{VAUX}$ | | **2.8** | | **3.3** | V |
| | | VAUX Available Current | $I_{VAUX}$ | | | | **4** | mA |
| | | VAUX Voltage Ripple | $V_{VAUX_PP}$ | | | 50 | | mV |
| | | | | $T_{INTERNAL}$ ≤ 100°C | | | **100** | |
| | | VAUX Capacitance (External) | $C_{VAUX_EXT}$ | | | | 0.01 | µF |
| | | VAUX Resistance (External) | $R_{VAUX_EXT}$ | $V_{PRI_DC} < V_{µC_ACTIVE}$ | 1.5 | | | kΩ |
| | Fault | VAUX Fault Response Time | $t_{VAUX_FR}$ | From fault to $V_{VAUX}$ = 2.8 V, $C_{VAUX}$ = 0 pF | | 10 | | µs |

## BCM Module Timing diagram



## High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



## Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected data form primary sourced units processing power in forward direction.See associated figures for general trend data.

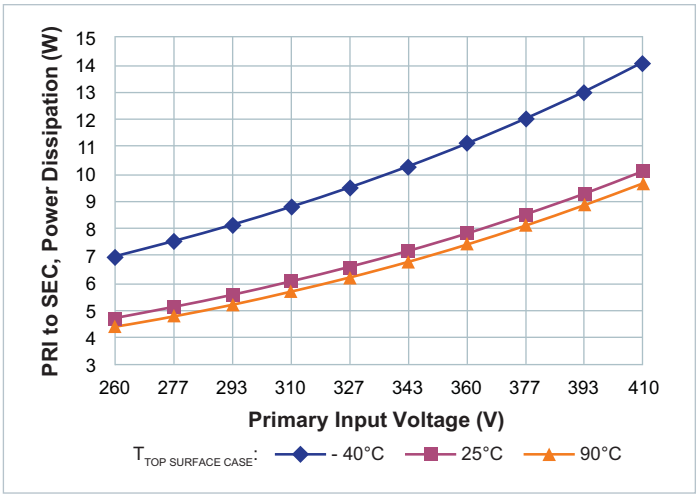



***Figure 4*** — *No load power dissipation vs. $V_{PRI_DC}$*

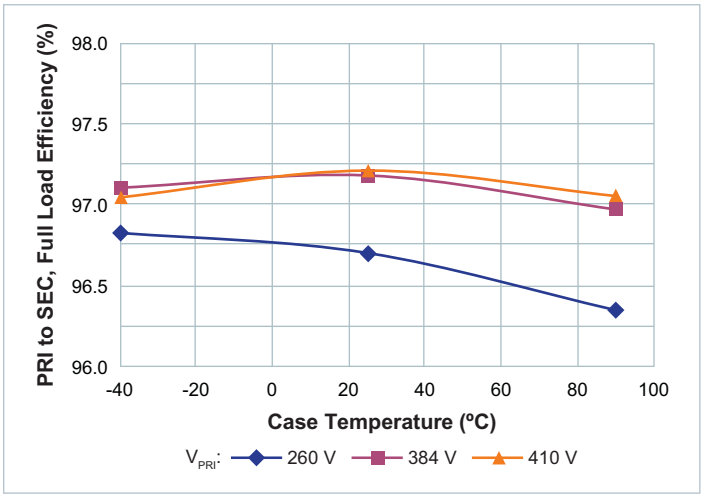



***Figure 5*** — *Full load efficiency vs. temperature; $V_{PRI_DC}$*

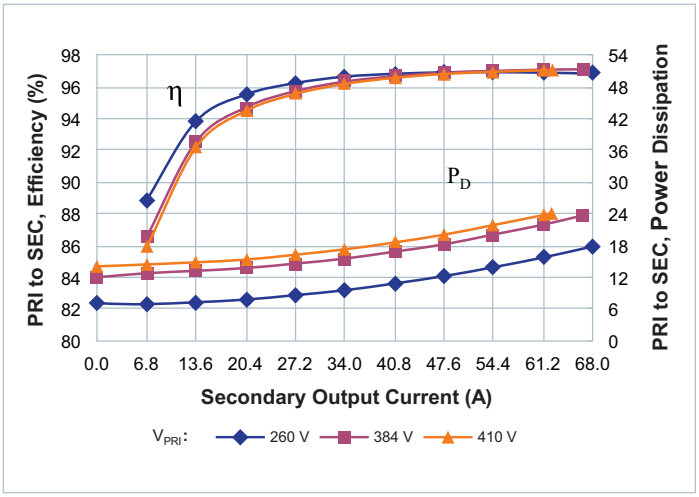



***Figure 6*** — *Efficiency and power dissipation at $T_{CASE}$ = -40°C*

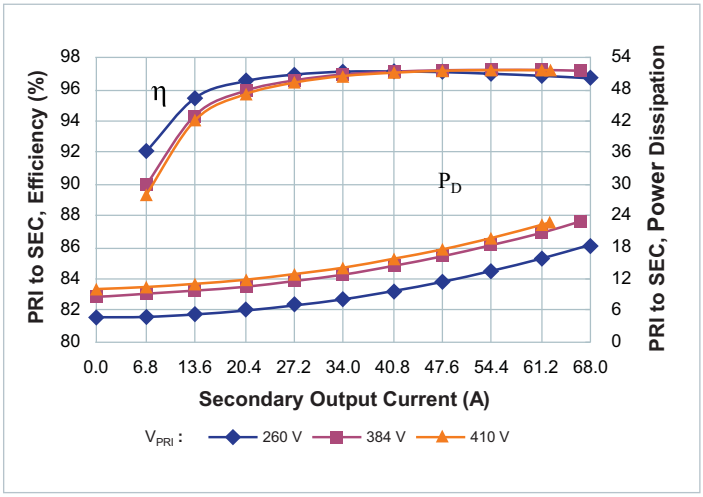



***Figure 7*** — *Efficiency and power dissipation at $T_{CASE}$ = 25°C*

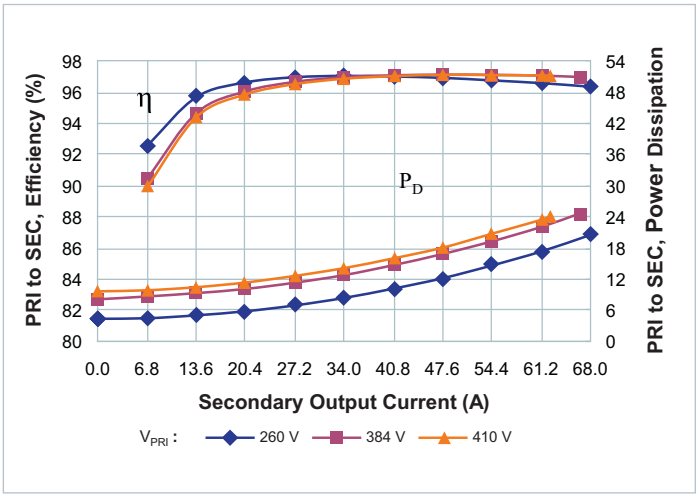



***Figure 8*** — *Efficiency and power dissipation at $T_{CASE}$ = 90°C*

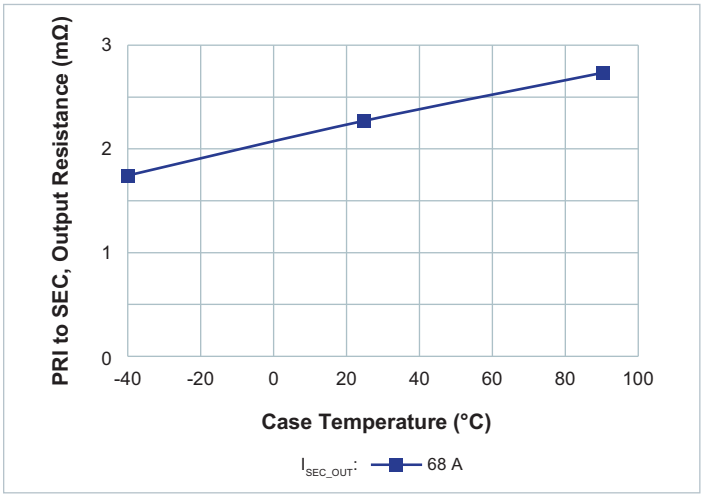



***Figure 9*** — *$R_{SEC}$ vs. temperature; Nominal $V_{PRI_DC}$ $I_{SEC_DC}$ = 66.67 A at $T_{CASE}$ = 90°C*

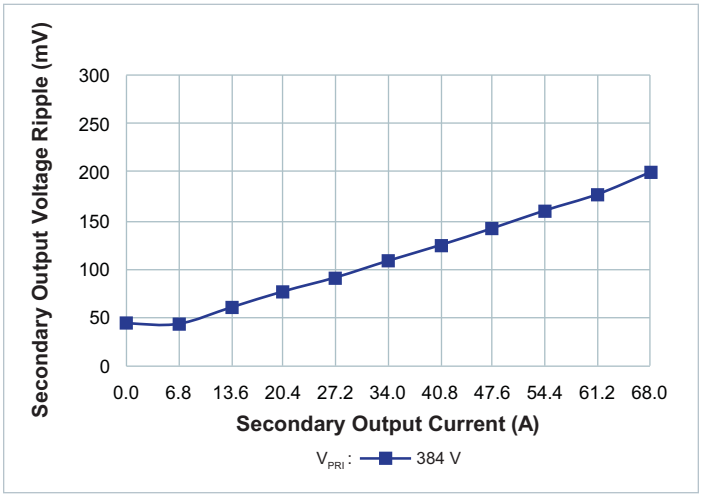



***Figure 10*** — *$V_{SEC_OUT_PP}$ vs. $I_{SEC_DC}$ ; No external $C_{SEC_OUT_EXT}$. Board mounted module, scope setting : 20 MHz analog BW*

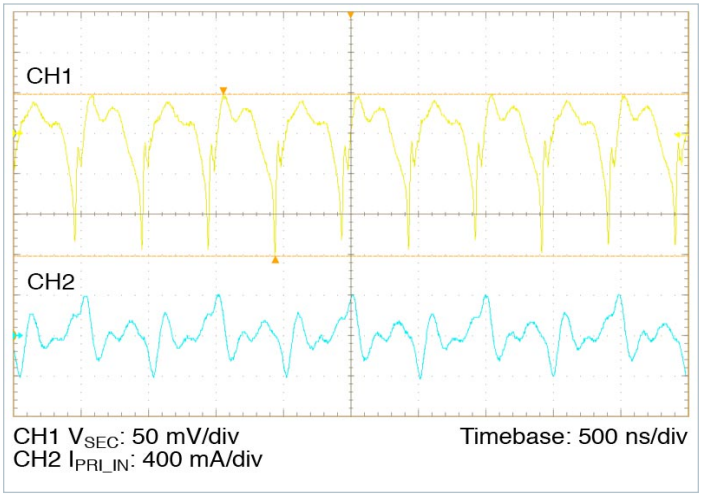



***Figure 11*** — *Full load ripple, 270 µF $C_{PRI_IN_EXT}$; No external $C_{SEC_OUT_EXT}$. Board mounted module, scope setting : 20 MHz analog BW*

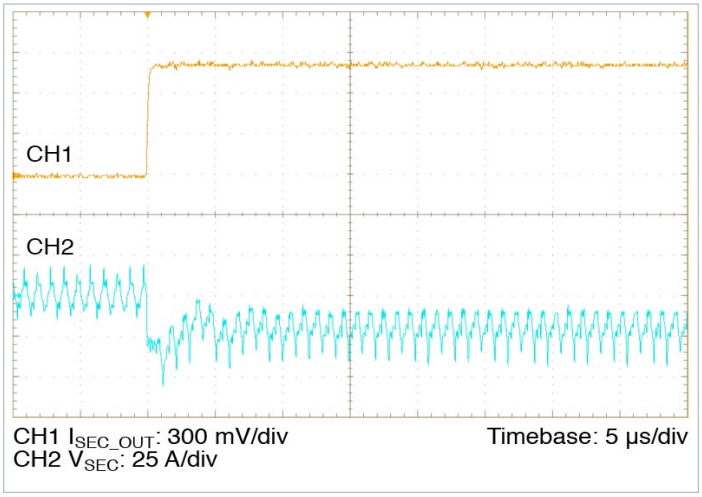



***Figure 12*** — *0 A– 68 A transient response: $C_{PRI_IN_EXT}$ = 270 µF, no external $C_{SEC_OUT_EXT}$*

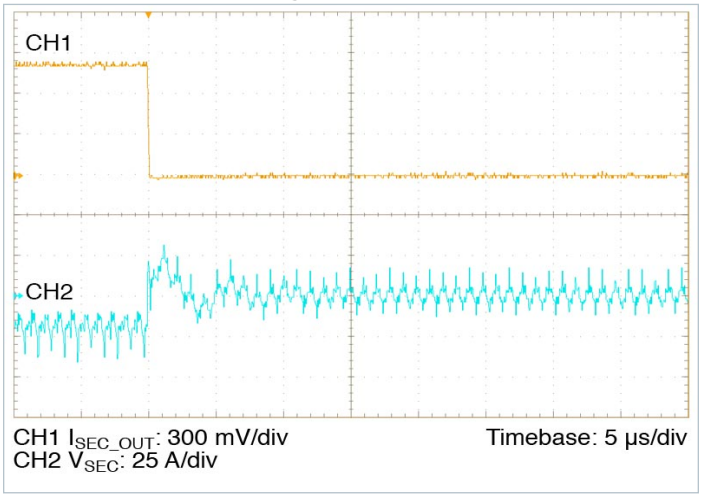



***Figure 13*** — *68 A – 0 A transient response: $C_{PRI_IN_EXT}$ = 270 µF, no external $C_{SEC_OUT_EXT}$*

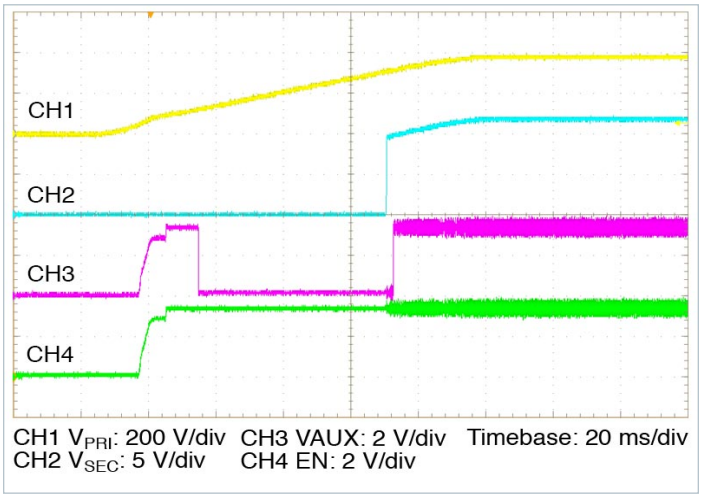



***Figure 14*** — *Start up from application of $V_{PRI_DC}$= 384 V, 50% $I_{OUT}$, 100% $C_{SEC_OUT_EXT}$*

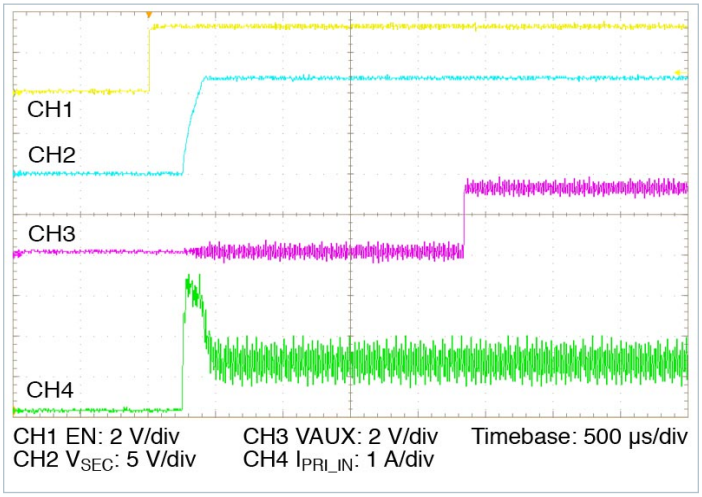



***Figure 15*** — *Start up from application of EN with pre-applied $V_{PRI_DC}$ = 384 V, 50% $I_{SEC_DC}$, 100% $C_{SEC_OUT_EXT}$*

## General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Mechanical** | | | | | | |
| Length | L | | 60.87 / [2.396] | 61.00 / [2.402] | 61.13 / [2.407] | mm/[in] |
| Width | W | | 24.76 / [0.975] | 25.14 / [0.990] | 25.52 / [1.005] | mm/[in] |
| Height | H | | 7.21 / [0.284] | 7.26 / [0.286] | 7.31 / [0.288] | mm/[in] |
| Volume | Vol | Without Heatsink | | 11.13 / [0.679] | | $cm^3$/[$in^3$] |
| Weight | W | | | 41 / [1.45] | | g/[oz] |
| Lead finish | | Nickel | 0.51 | | 2.03 | µm |
| | | Palladium | 0.02 | | 0.15 | |
| | | Gold | 0.003 | | 0.051 | |
| **Thermal** | | | | | | |
| Operating Temperature | $T_{INTERNAL}$ | BCM384T120P800AC0 (T-Grade)<br>BCM384T120P800ACR (T-Grade) | -40 | | 125 | °C |
| | | BCM384M120P800AC0 (M-Grade)<br>BCM384M120P800ACR (M-Grade) | -55 | | 125 | °C |
| Thermal Resistance Top Side | $\Phi_{INT-TOP}$ | Estimated thermal resistance to maximum temperature internal component from isothermal top | | 1.35 | | °C/W |
| Thermal Resistance Leads | $\Phi_{INT-LEADS}$ | Estimated thermal resistance to maximum temperature internal component from isothermal leads | | 2 | | °C/W |
| Thermal Resistance Bottom Side | $\Phi_{INT-BOTTOM}$ | Estimated thermal resistance to maximum temperature internal component from isothermal bottom | | 1.91 | | °C/W |
| Thermal Capacity | | | | 34 | | Ws/°C |
| **Assembly** | | | | | | |
| Storage temperature | | BCM384T120P800AC0 (T-Grade)<br>BCM384T120P800ACR (T-Grade) | -55 | | 125 | °C |
| | | BCM384M120P800AC0 (M-Grade)<br>BCM384M120P800ACR (M-Grade) | -65 | | 125 | °C |
| ESD Withstand | $ESD_{HBM}$ | Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV) | | | | |
| | $ESD_{CDM}$ | Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V) | | | | |

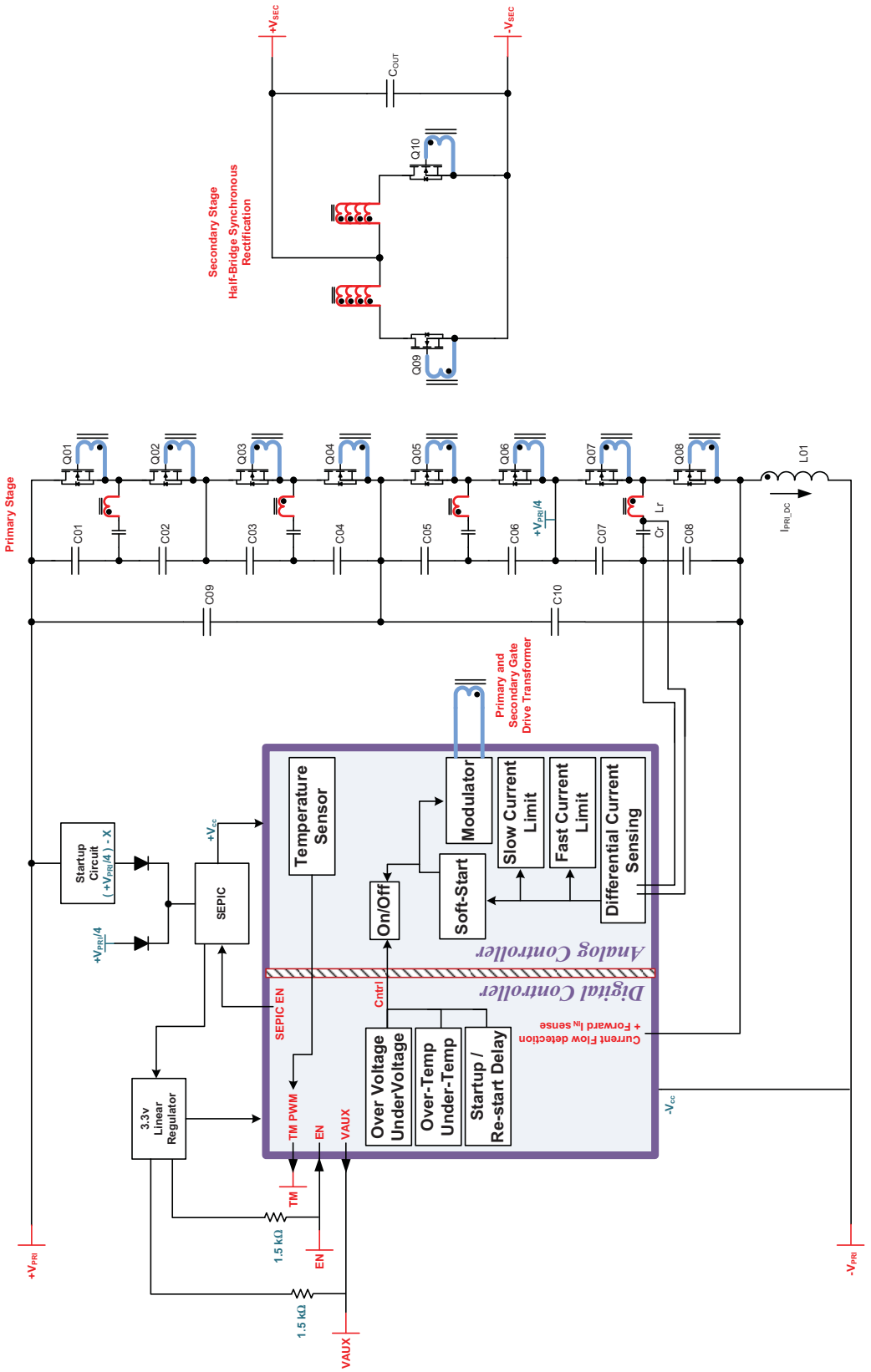
## General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

| | | | | | | |
|---|---|---|---|---|---|---|
| **Soldering[1]** | | | | | | |
| Peak Temperature Top Case | | | | | 135 | °C |
| **Safety** | | | | | | |
| Isolation voltage / Dielectric test | $V_{HIPOT}$ | PRIMARY to SECONDARY | **4,242** | | | $V_{DC}$ |
| | | PRIMARY to CASE | **2,121** | | | |
| | | SECONDARY to CASE | **2,121** | | | |
| Isolation Capacitance | $C_{PRI_SEC}$ | Unpowered Unit | **620** | 780 | **940** | pF |
| Insulation Resistance | $R_{PRI_SEC}$ | At 500 Vdc | **10** | | | MΩ |
| MTBF | | MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer | | 5.61 | | MHrs |
| | | Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled | | 1.73 | | MHrs |
| Agency Approvals / Standards | | cTUVus "EN 60950-1" | | | | |
| | | cURus "UL 60950-1" | | | | |
| | | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | | |

[1] Product is not intended for reflow solder attach.

## BCM Module Block Diagram



## Sine Amplitude Converter™ Point of Load Conversion

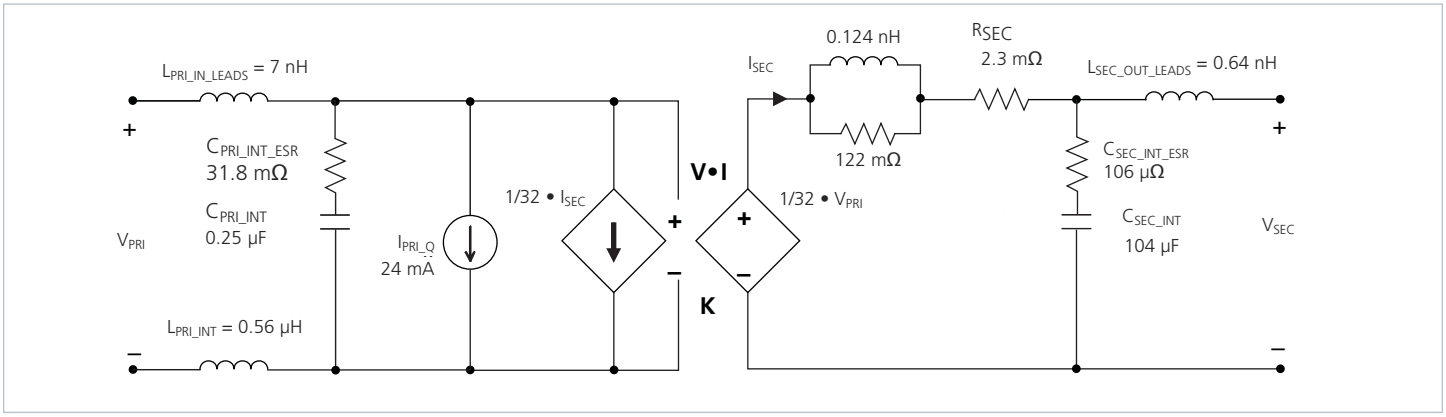



***Figure 16*** — *BCM module AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from Primary to secondary and vice versa. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the BCM module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM384x120y800ACz SAC can be simplified into the preceeding model.

At no load:

$$V_{SEC} = V_{PRI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{SEC}}{V_{PRI}} \qquad (2)$$

In the presence of load, $V_{OUT}$ is represented by:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \qquad (3)$$

and $I_{OUT}$ is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI_Q}}{K} \qquad (4)$$

$R_{OUT}$ represents the impedance of the SAC, and is a function of the $R_{DSON}$ of the input and output MOSFETs and the winding resistance of the power transformer. $I_Q$ represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{SEC} = 0\ \Omega$ and $I_{PRI_Q} = 0$ A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with $V_{IN}$.

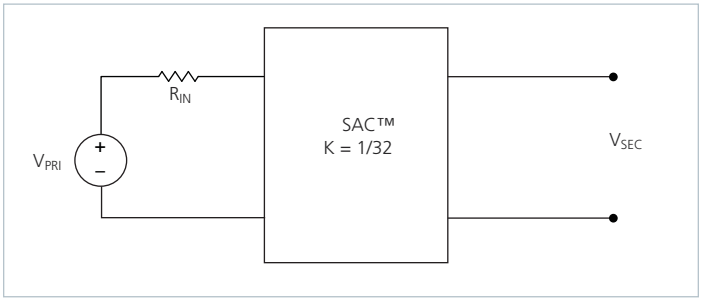



***Figure 17*** — *K = 1/32 Sine Amplitude Converter with series input resistor*

The relationship between $V_{PRI}$ and $V_{SEC}$ becomes:

$$V_{SEC} = (V_{PRI} - I_{PRI} \bullet R_{IN}) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) ($I_{PRI_Q}$ is assumed = 0 A) into Eq. (5) yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{IN} \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where $R_{SEC}$ is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the primary side of the SAC is effectively scaled by $K^2$ with respect to the secondary.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 1 mΩ, with K = 1/32 .

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the primary input to the SAC. A switch in series with $V_{PRI}$ is added to the circuit. This is depicted in Figure 18.

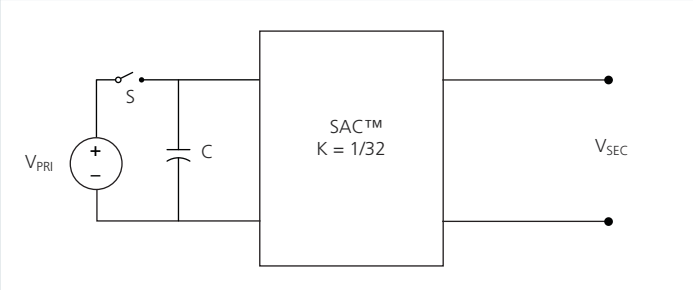



***Figure 18*** — *Sine Amplitude Converter with input capacitor*

A change in $V_{PRI}$ with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{PRI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to $V_{PRI}$, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{SEC} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{SEC} = \frac{C}{K^2} \bullet \frac{dI_{SEC}}{dt} \qquad (9)$$

The equation in terms of the output has yielded a $K^2$ scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary output when expressed in terms of the input. With a K= 1/32 as shown in Figure 18, C=1 µF would appear as C=1024 µF when viewed from the secondary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation ($P_{PRI_NL}$): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($R_{SEC}$): refers to the power loss across the BCM® module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI_NL} + P_{R_{SEC}} \qquad (10)$$

Therefore,

$$P_{SEC_OUT} = P_{PRI_IN} - P_{DISSIPATED} = P_{RI_IN} - P_{PRI_NL} - P_{R_{SEC}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC_OUT}}{P_{IN}} = \frac{P_{PRI_IN} - P_{PRI_NL} - P_{R_{SEC}}}{P_{IN}} \qquad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{PRI_NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left( \frac{P_{PRI_NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}} \right)$$

## Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the BCM module's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 1 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce input and/or output voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

  The module primary/secondary voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the output of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500 kHz the module appears as an impedance of $R_{SEC}$ between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. (13).

$$C_{SEC_EXT} = \frac{C_{PRI_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

## Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 19 shows the "thermal circuit" for a VI Chip® BCM module 2361 in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is $PD_{TOTAL}$ and the three surface temperatures are represented as $T_{CASE_TOP}$, $T_{CASE_BOTTOM}$, and $T_{LEADS}$. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

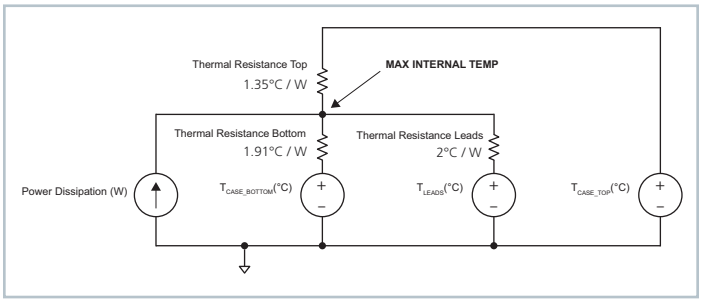



***Figure 19*** — *Top case, Bottom case and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE_TOP}$

$T_{INT} - PD_2 \bullet 1.24 = T_{CASE_BOTTOM}$

$T_{INT} - PD_3 \bullet 7 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_2 + PD_3$

Where $T_{INT}$ represents the internal temperature and $PD_1$, $PD_2$, and $PD_3$ represent the heat flow through the top side, bottom side, and leads respectively.

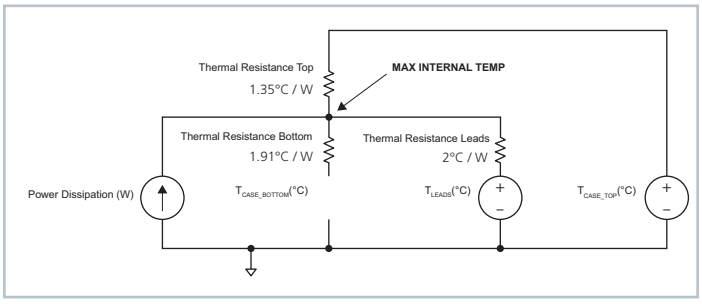



***Figure 20*** — *Top case and leads thermal model*

Figure 20 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE_TOP}$

$T_{INT} - PD_3 \bullet 7 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_3$

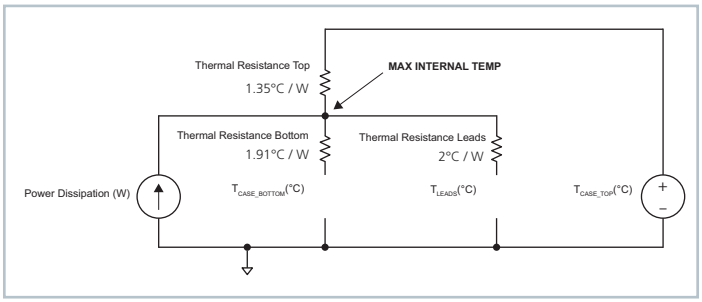



***Figure 21*** — *Top case thermal model*

Figure 21 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE_TOP}$

$PD_{TOTAL} = PD_1$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

## Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of BCMs in order to prevent circulating currents.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

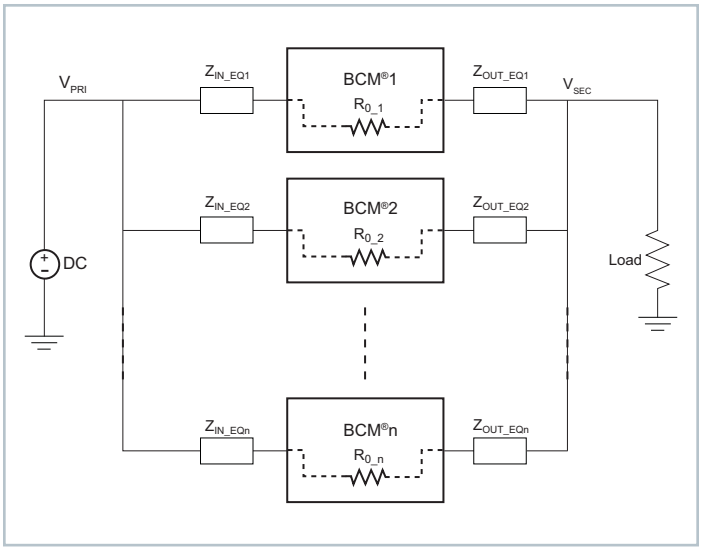



***Figure 22*** — *BCM module array*

## Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting $I^2t$
- Recommend fuse: ≤ 5 A Bussmann PC-Tron

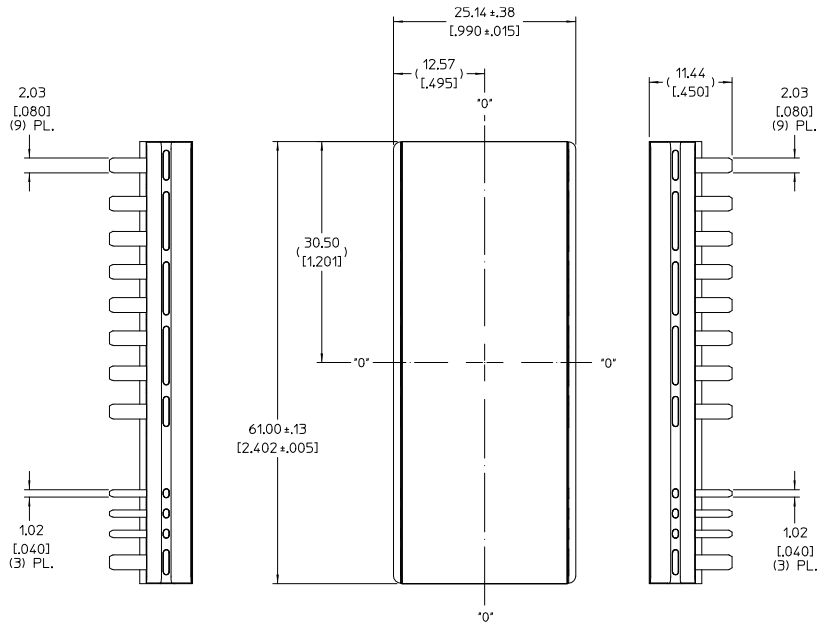
## Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{PRI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

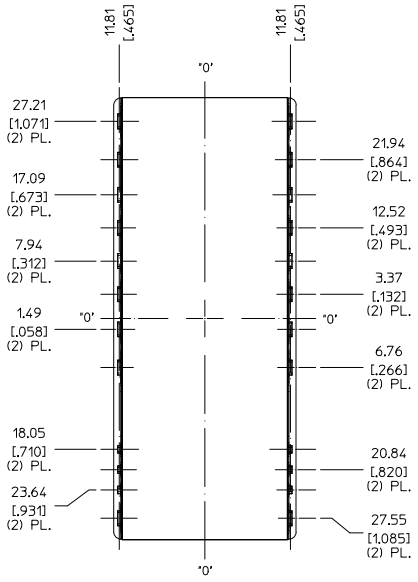
Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input.

The BCM384T120P800ACR and BCM384M120P800ACR are both qualified for continuous operation in reverse power condition. A primary voltage of $V_{PRI_DC} > V_{PRI_UVLO+_R}$ must be applied first allowing primary reference controller and power train to start. Continuous operation in reverse is then possible after a successful startup.

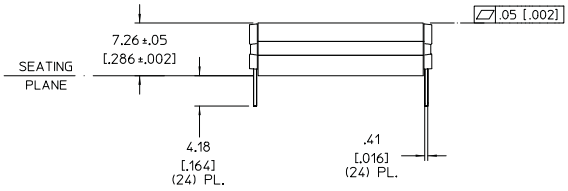
## BCM Module Through Hole Package Mechanical Drawing and Recommended Land Pattern




*TOP VEIW (COMPONENT SIDE)*

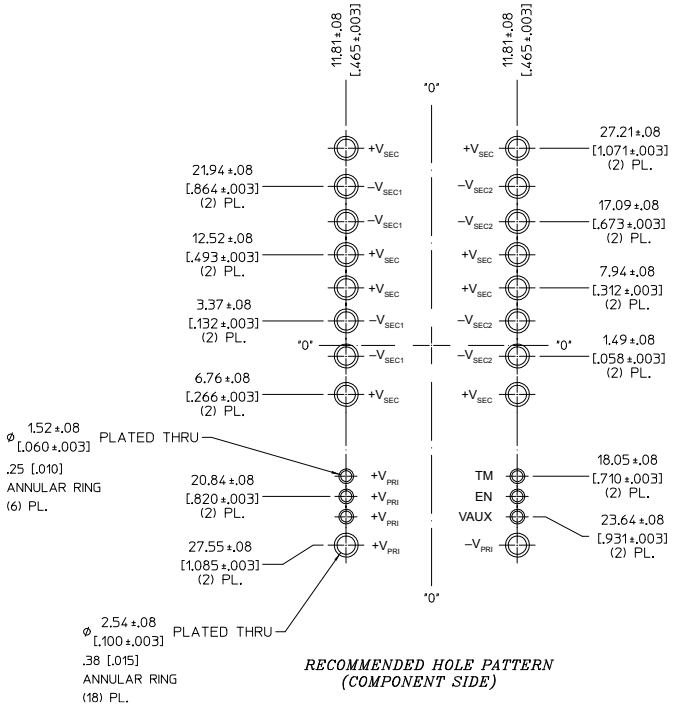



*BOTTOM VIEW*




NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.




*RECOMMENDED HOLE PATTERN (COMPONENT SIDE)*

## Revision History

| Revision | Date | Description | Page Number(s) |
|---|---|---|---|
| 1.1 | 05/15 | Previous version of part #BCM384x120y800AC0 | n/a |
| 1.2 | 07/21/15 | Multiple updates. Additional new products.<br>Analog HV BCM qualified for continuous reversible operations. | all |

**Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.**

Information furnished by Vicor is believed to be accurate and reliable. However, no responsibility is assumed by Vicor for its use. Vicor makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication. Vicor reserves the right to make changes to any products, specifications, and product descriptions at any time without notice. Information published by Vicor has been checked and is believed to be accurate at the time it was printed; however, Vicor assumes no responsibility for inaccuracies. Testing and other quality controls are used to the extent Vicor deems necessary to support Vicor's product warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.
**Specifications are subject to change without notice.**

## Vicor's Standard Terms and Conditions

All sales are subject to Vicor's Standard Terms and Conditions of Sale, which are available on Vicor's webpage or upon request.

## Product Warranty

In Vicor's standard terms and conditions of sale, Vicor warrants that its products are free from non-conformity to its Standard Specifications (the "Express Limited Warranty"). This warranty is extended only to the original Buyer for the period expiring two (2) years after the date of shipment and is not transferable.
UNLESS OTHERWISE EXPRESSLY STATED IN A WRITTEN SALES AGREEMENT SIGNED BY A DULY AUTHORIZED VICOR SIGNATORY, VICOR DISCLAIMS ALL REPRESENTATIONS, LIABILITIES, AND WARRANTIES OF ANY KIND (WHETHER ARISING BY IMPLICATION OR BY OPERATION OF LAW) WITH RESPECT TO THE PRODUCTS, INCLUDING, WITHOUT LIMITATION, ANY WARRANTIES OR REPRESENTATIONS AS TO MERCHANTABILITY, FITNESS FOR PARTICULAR PURPOSE, INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT, OR ANY OTHER MATTER.

This warranty does not extend to products subjected to misuse, accident, or improper application, maintenance, or storage. Vicor shall not be liable for collateral or consequential damage. Vicor disclaims any and all liability arising out of the application or use of any product or circuit and assumes no liability for applications assistance or buyer product design. Buyers are responsible for their products and applications using Vicor products and components. Prior to using or distributing any products that include Vicor components, buyers should provide adequate design, testing and operating safeguards.

Vicor will repair or replace defective products in accordance with its own best judgment. For service under this warranty, the buyer must contact Vicor to obtain a Return Material Authorization (RMA) number and shipping instructions. Products returned without prior authorization will be returned to the buyer. The buyer will pay all charges incurred in returning the product to the factory. Vicor will pay all reshipment charges if the product was defective within the terms of this warranty.

## Life Support Policy

VICOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF VICOR CORPORATION. As used herein, life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness. Per Vicor Terms and Conditions of Sale, the user of Vicor products and components in life support applications assumes all risks of such use and indemnifies Vicor against all liability and damages.

## Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and pending patent applications) relating to the products described in this data sheet. No license, whether express, implied, or arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Numbers:
6,911,848; 6,930,893; 6,934,166; 7,145,786; 7,782,639; 8,427,269 and for use under 6,975,098 and 6,984,965.

**Vicor Corporation**
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

**email**
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com