❑ MN103SB9 Series

Type	MN103SB9N	MN103SFB9R
Internal ROM type	Mask ROM	FLASH
ROM (byte)	512K	1024K
RAM (byte)	32K	
Package (Lead-free)	TQFP128-P-1414A	
Minimum Instruction Execution Time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)	

■ Interrupts

RESET. IRQ × 9. NMI. Timer × 28. I^2C × 3. SIF × 10. DMA × 12. WDT. A/D. Time base timer × 2. System error

■ Timer Counter

8-bit timer × 10

Reload-down count. Cascade connection possible (usable as a 16-bit to 32-bit timer)

16-bit timer × 6

Up-down count. Input capture. PWM output. Compare/capture register 2 channnels

Time base timer × 1

Watchdog timer × 1

■ Serial interface

UART/Synchronous/Multi-master I^2C interface selective × 3

UART/Synchronous interface selective × 2

■ DMA controller

Number of channels: 4 channels

Unit of transfer: 8/16/32 bits

Maximum transfer cycles: 65535

Starting factor: External interrupt. Timer. Serial transmission/reception. A/D conversion finish. I^2C transmission/reception. External transmission request. Software

Transfer method: 2-bus cycle transfer

Adressing modes: Fixed. Increment. Decrement

Transfer mode: Word transfer. Burst transfer. Intermittent transfer

■ Extended Calculation

Multiply and accumulate arithmetic. Multiplication. Saturated arithmetic

■ I/O Pins

I/O 104 : Common use

■ A/D converter

10-bit × 12 channels

■ ROM Correction

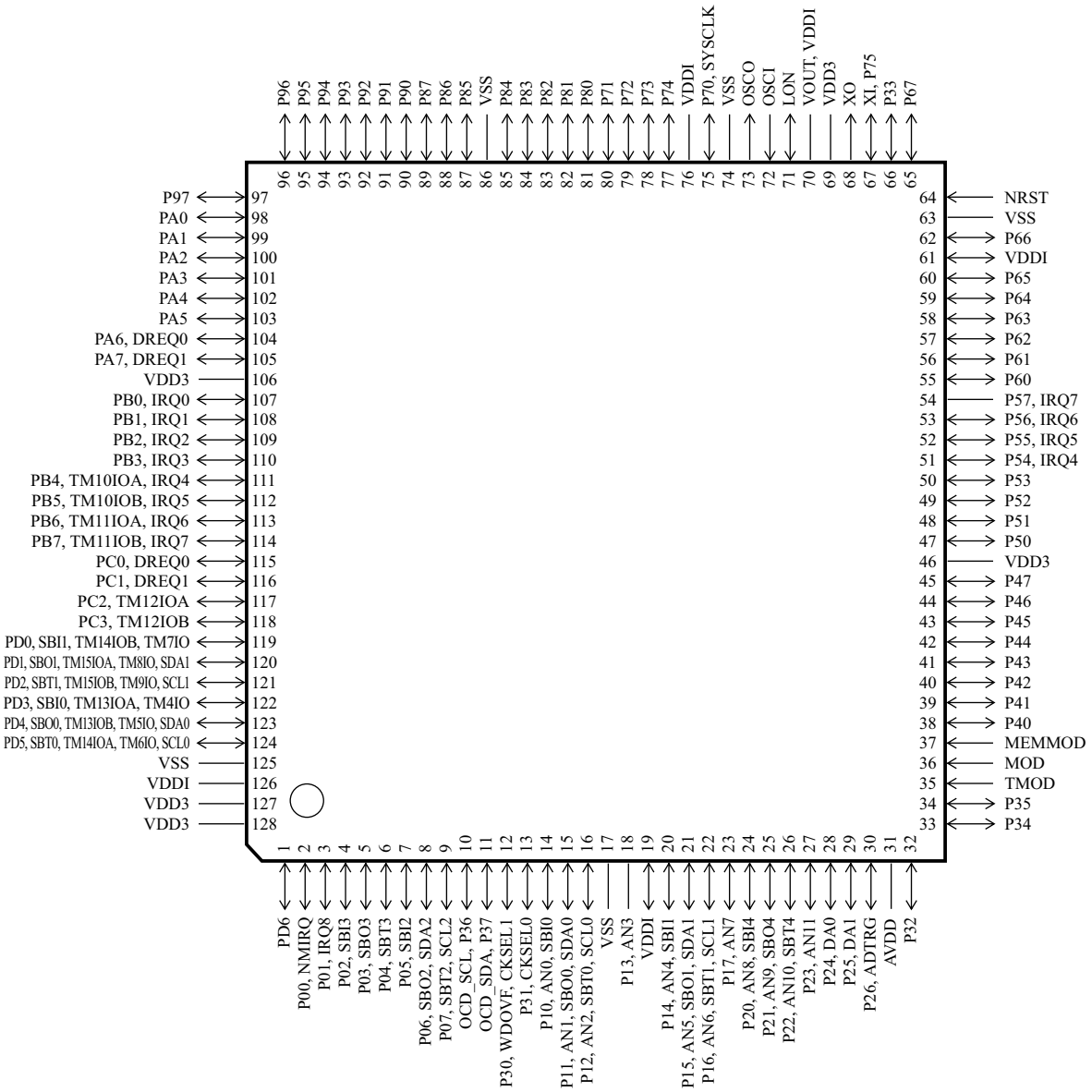
8 channels

■ Electrical Charactreistics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
Non-linear error		AVDD = 3.3 V. VSS = 0 V			±4	LSB
Differential non-linearity error					±4	LSB

■ Pin Assignment

TQFP128-P-1414A



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