F75204

USB Charger Controller

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Release Date: Dec., 2011
Version: V0.15P

F75204 Datasheet Revision History

Version	Date	Page	Revision History
Data Brief	2011/09	-	Data Brief with Application Circuit
V0.11P	2011/09	-	Typo Correction
V0.12P	2011/09	-	Add new Function Description
V0.13P	2011/09	-	Update Application Circuit &
V0.14P	2011/10	-	Release Version. Update function description. Add AC / DC Spec.
V0.15P	2011/12		Add new Function Description

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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Fintek for any damages resulting from such improper use or sales.

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1 General Description

The F75204 is the combination of Hi-Speed USB data switches and a USB Dedicated Charger identification circuit. The F75204 support most of the USB Battery Charging Specification worldwide, including BC 1.2, Apple® charging spec (for i-Pad & i-Phones) and specs for Samsung Galaxy Tab. The F75204 also equipped with a control output to control peripheral power components.

A digital input CB is able to control the mode configuration of F75204. In transmission mode, the F75204 acts like a USB bridge which connects the route between the USB Host and the USB Device, and allows device using CDP mode to charge the handheld devices; in the charger mode the F75204 can automatic detect the device and provide correct acknowledge signal to the device that is going to be charged, even if the computer system has been shut down.

By setting the USB Data pins (D+/D-) to the required voltage levels, the charging device recognize the voltage levels, and starts to draw the current to charge. The F75204 are equipped with a control output (CEN or CEN#) allows users to control the peripheral power management device which controls the charging current.

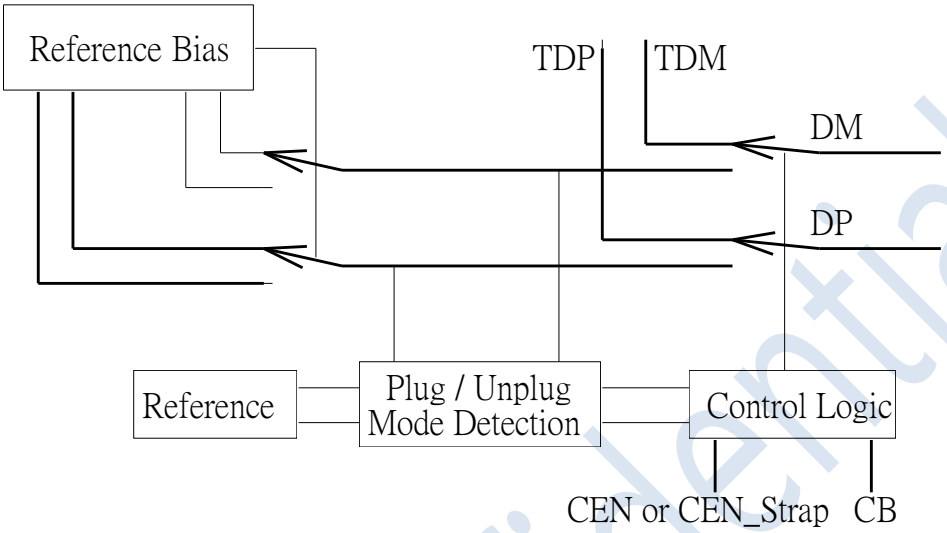
The F75204 Series enhanced ESD protection up to ±8kV on the DP and DM. The F75204 is available in a MSOP-8 Package and is allow working over the 0°C to +70°C temperature range.

2 Feature List

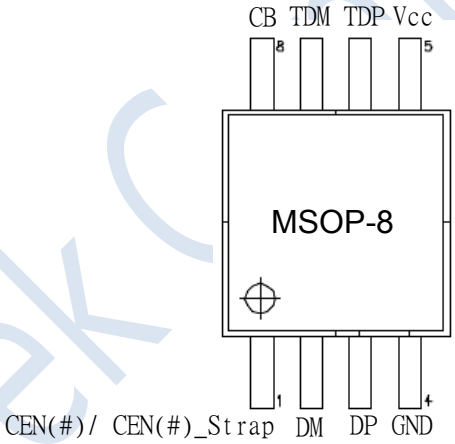
- 4.5V~5.5V Single Supply Operation.
- Automatic USB charger Identification Circuit.
- Automatic Power Switch Control (CEN or CEN#)
- Support Apple® Devices fast charging.
- Support BC1.2 & YD/T 1591-2009 Charging Spec.
- Support Samsung Galaxy Devices Charging.
- Support BC1.2 **CDP** in S0 state.
- Fintek **Advance CDP** Feature.
- Support **Full / Low speed USB device** wake up in from S3 state.
- ±8kV High ESD Protection On DP/DM.
- Available in MSOP-8 Package.

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3 Block Diagram



4 Pin Configuration



Pin Configuration of F75204

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5 Pin Description

IN - input pin with schmitt trigger.
OUT - Open-drain output pin
P -Power.

4.1. Pin Description

F75204	Pin Name	Type	Description
1	CEN(#)	Out	Open drain output. Power Switch Control Output. This pin can be used as the enable signal for the power switch, which controls the V_{BUS} of the USB charging port.
	CEN(#)_Strap	-	External pull high: CEN External pull down: CEN#
2	DM	Analog	USB negative data-channel to external USB device
3	DP	Analog	USB positive data-channel to external USB device
4	GND	Ground	Ground
5	VCC	P	Power
6	TDP	Analog	USB positive data-channel to USB controller (HOST)
7	TDM	Analog	USB negative data-channel to USB controller (HOST)
8	CB	IN	Mode Selection Pin, CB = 1 Transmission Mode; CB = 0 Charger Mode.

6 Function Description

6.1 F75204 General Function Description

6.1.1 Mode Description & Selection

The F75204 USB charger controller can be configured to operate either as the bridge or USB devices identification circuit. Users can alternate between modes by a digital input mode control pin – CB. In the transmission Mode, as it shows below in Figure 6.1, the F75204 acts as a USB bridge which connect the D+/D- data line of the host to the USB device.

In Charger Mode, the F75204 supplies the voltage to the D+ and D- lines from the internal resistor-divider. If the device attached is BC 1.2-compliant, the F75204 will automatically shorts D+ and D- data line to allow correct charger detection.

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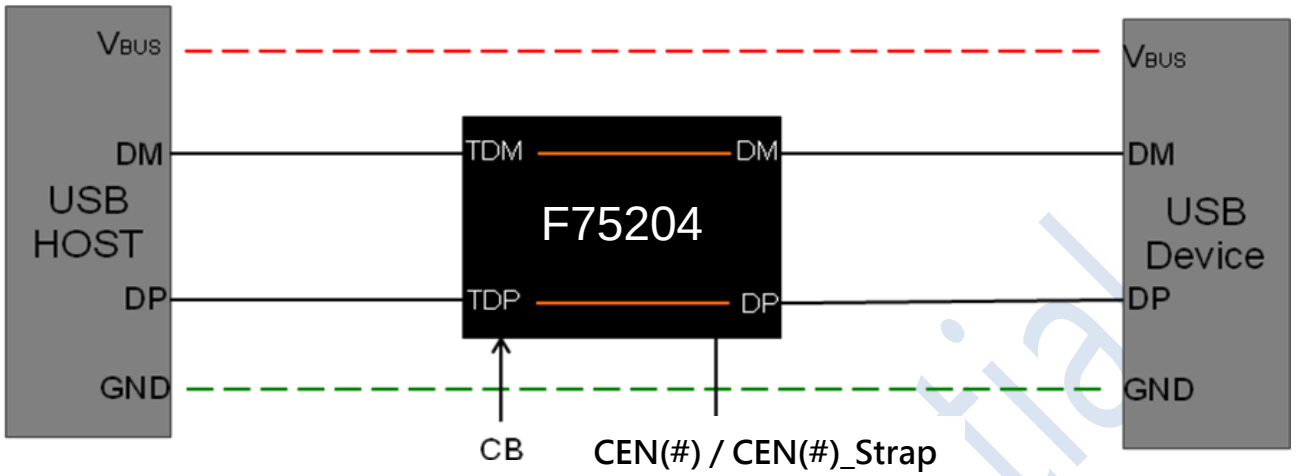


Figure 6.1 Pass-Through Mode

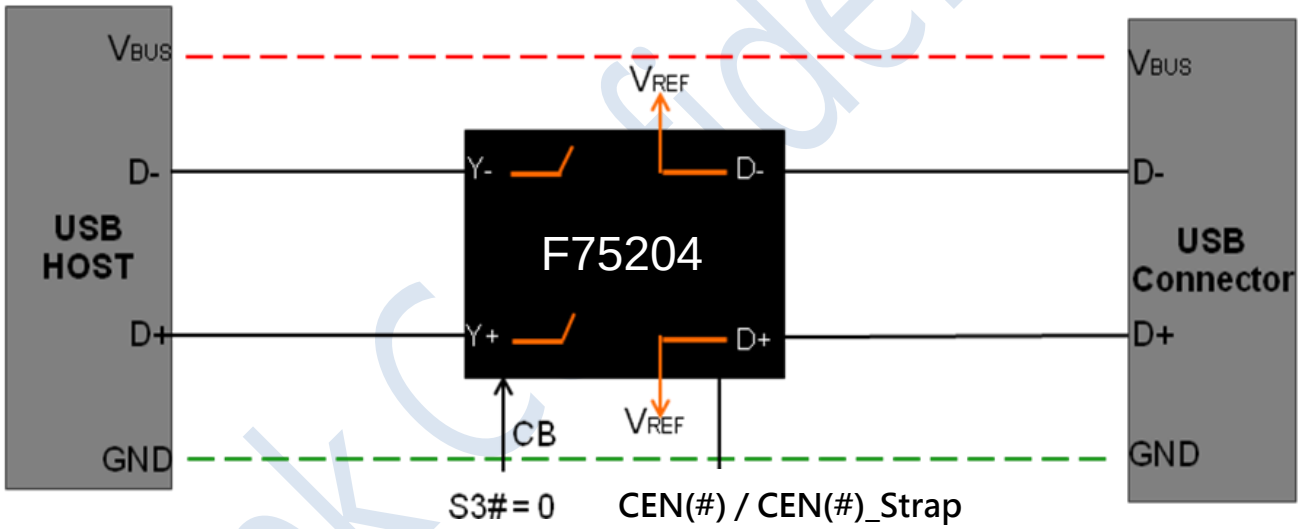


Figure 6.2 Charger Mode (Auto Detect Mode)

Table 6.1.2 Truth table of CB

CB	Configuration
0	Charger Mode
1	Pass-Through

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6.1.2 Advance CDP Function

The F75204 featured an Advance CDP function to provide an always USB connectivity for handheld devices. When non-CDP devices are connected to a CDP USB port, some might fail to make connection with the USB host on a standard CDP port. To solve this problem, the Advance CDP feature is able to switches the charging port automatically to SDP mode during handshaking, if the attached device is a non-CDP device. This function can ensure a correct data connection when non-CDP device is plugged in.

CDP is the abbreviation for Charging Downstream Port, which allows supported devices to do fast charging (Maximum 1.5A) & data communication at the same time. The advance CDP solution is able to disable CDP function while attached device is not support CDP function, and re-connect to the attached device.

6.1.3 Full / Low Speed USB Devices Wake up

Traditional USB host charger may cut off the data linking path then disable the keyboard / mouse wakeup function. To avoid the situation, the F75204 allows Full / Low speed USB devices to wake up the system. In order to make sure the wake up function work properly, the F75204 won't cut off the D+ / D- data path of USB if the device attached is an full / low speed USB keyboard / mouse. This feature allows most of keyboard / mouse to wake the system up normally.

6.1.4 External Chip Enable Signal – CEN (or CEN#)

The F75204 is equipped with a digital output signal pin – CEN (or CEN#), which allows users to control the external power switch. To reduce the complexity, Fintek made this F75204 to supports both active high / low types of power switch. Using an external strap resistor to deiced the character of this pin. Table 6.1.3.1 describes the configuration of strap resistor.

Table 6.1.3.1 CEN(#) Strapping

CEN Strap	Configuration	Remark
CEN	External Pull-High	High Active System
CEN#	External Pull-Down	Low Active System

In order to control the Power Switch, the CEN (or CEN#) should be connected to the enable pin of the Power Switch. The F75204 will assert a signal for 1 sec to cut off the Vbus power, when the logic input signal level of CB changes from 0 to 1 or 1 to 0. This function is able to emulate the re-plug of USB device and guarantee that the device has correct contact detection.

The F75204 use CEN(#) pin to reconnect the devices. In other word, when a non-CDP device is connected to the USB charging port, the F75204 will trigger CEN (CEN#) pulse, and make the device to reconnect with host in the SDP mode.

CEN: (External Pull-High on CEN(#)_Strap)

If the USB Vbus is controlled by an Active-High power switch, strap the F75204 to CEN configuration. Then F75204 CEN pin will assert a constant high signal to enable the Vbus Power Switch. Only when the logic level CB changes, then the CEN pull-down for 1 Sec to temporary shut down the Vbus.

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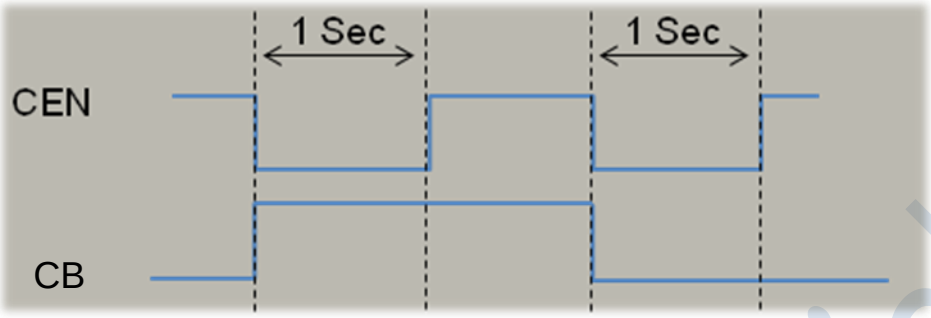


Figure 6.1.3.1 CEN Timing diagram

CEN#: (External Pull-Down on CEN(#)_Strap)

If the USB Vbus is controlled by an Active-Low power switch, strap the F75204 to CEN# configuration. Then F75204 CEN# output signal will keep low to enable the Vbus Power Switch. Only when the logic level CB changes, then the CEN# output signal will assert high 1 Sec to temporary shut down the Vbus.

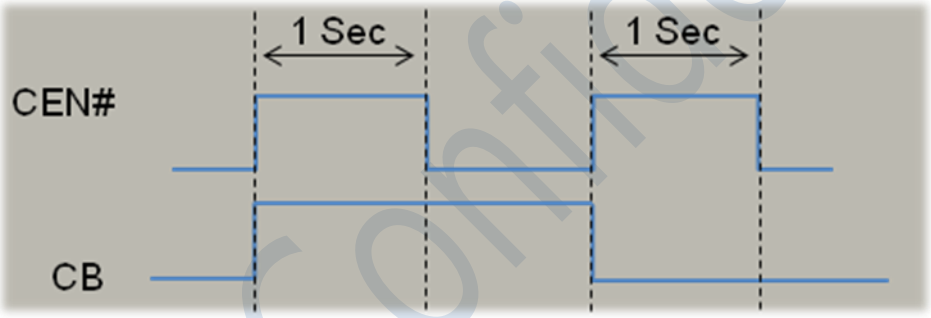


Figure 6.1.3.2 CEN# Timing diagram

※ Please Note that. The CEN(#) signal is designed to provide the correct contact detection after each mode transfer. Please note that all the mode transformation of USB port process must be finished during the work period of the CEN(#) pulse. If the mode transfer process is taking longer than 1 sec please consider to extent the CEN(#) pulse time.

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7 Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	SYMBOL	RATINGS	UNIT
Voltages Referenced to GND	VCC, TDP, TDM, CB, DP, DM, CEN	-0.3 to 6.0	V
Continuous Current into Any Terminal		±30	mA
※ Maximum junction temperature (plastic package)	T_j	+150	°C
※ Maximum storage temperature	T_{STO}	-65 ~ +150	°C
※ Maximum lead temperature (soldering 10s)		+260	°C

Note: **If ICs are stressed beyond the limits listed in the "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.**

Package thermal information

PARAMETER	SYMBOL	SOIC	UNIT
Thermal resistance junction-ambient	Rth_ja		°C/W

Recommended Operating Conditions

Supply Voltage, VCC ---------- 2.8V~5.5V
Ambient Temperature Range---------- 0°C to 70°C
Junction Temperature Range---------- -40°C to 125°C

DC and AC electrical characteristics (VCC=5V, TA = 25℃)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
POWER SUPPLY							
Operating Power Supply Range	Vcc	$V_{CB} > V_{IH}$		4.5		5.5	V
		V_{CB} = 0V		4.5		5.5	V
Supply Current (F75204)	I_{CC}	CB = Vcc	Vcc = 4.5V			35	uA
		CB = Vcc	Vcc = 5.5V			45	
		CB = 0V	Vcc =4.5V		150	200	
		CB = 0V	Vcc = 5.5V		200	250	
ANALOG SWITCH							
Analog Signal Range	V_{DP}, V_{DM}			0		Vcc	V
On Resistance TDP/ TDM Switch	R_{ONT}	V=0V to Vcc, I=10mA			4.0	7	Ω

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
On-Resistance Match Between Channels TDP/TDM Switch	ΔR_{ON}	Vcc=5.0V, I=10mA, V=400mV		0.1		Ω
On-Resistance Flatness TDP/TDM Switch	R_{FLAT}	Vcc=5.0V, I=10mA, V=0V to Vcc		0.1		Ω
On Resistance of DP/DM short	R_{SHORT}	CB=0, DP=1V, DM=20Kohm		50	70	Ω
Off Leakage Current	I_{SW}(Off)	Vcc=5.5V, V_{TDP} ,V_{TDM} =3.6V, 0.3V	-250		250	nA
On Leakage Current	I_{SW}(On)	Vcc=5.5V, V_{TDP} ,V_{TDM} =3.6V, 0.3V, V_{DP} ,V_{DM} =3.6V, 0.3V	-250		250	nA
Dynamic						
Turn On Time	t_{ON}	V_{TDP} or V_{TDM} =1.5V, R_L=300Ω, C_L=35pF, V_{IH}=Vcc, V_{IH}=0V		17	40	us
Turn Off Time	t_{OFF}	V_{TDP} or V_{TDM} =1.5V, R_L=300Ω, C_L=35pF, V_{IH}=Vcc, V_{IH}=0V		15	40	us
INTERNAL RESISTORS ※						
RP1/RP2 Ratio	RT_{RP}		0.854	0.863	0.872	
DP Output Impedance	R_{DP}		17.3		28.6	kΩ
RM1/RM2 Ratio	RT_{RM}		1.485	1.5	1.515	
DM Output Impedance	R_{DM}		22.5		37.5	kΩ
LOGIC Input						
CB Input Logic High	V_{IH}		2.0			V
CB Input Logic Low	V_{IL}				0.4	V
CB Input Leakage Current	I_{IN}	$0 \leqq V_{IN} \leqq V_{IL}$ and $V_{IH} \leqq V_{IN} \leqq V_{CC}$, Vcc=5.5V	-1		+1	uA
CEN(#)						
Vbus Toggle time	t_{VBT}	CB=0 to 1 & 1 to 0	0.5	1.2	2	S
CEN# Output Logic High Voltage		CB=0 to 1, I_{SOURCE} = 2mA	Vcc-0.4			V
CEN# Output Leakage Current		Vcc=5.5V, $V_{CEN\#}$=0V, CEN# deasserted			1	uA
ESD Protection						
ESD Protection level (DP and DM only)	V_{ESD}	Air gun contact discharge		±8		kV
ESD Protection level all other pins	V_{ESD}	Human Body Model		±2		kV

※ Design Guarantee

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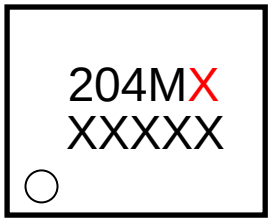
8 Ordering Information

Part Number	Package Type	Production Flow
F75204M	MSOP-8	Commercial, 0°C to +70°C

9 Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:

MSOP-8



1st Line: Device Name + **IC Version (X)**

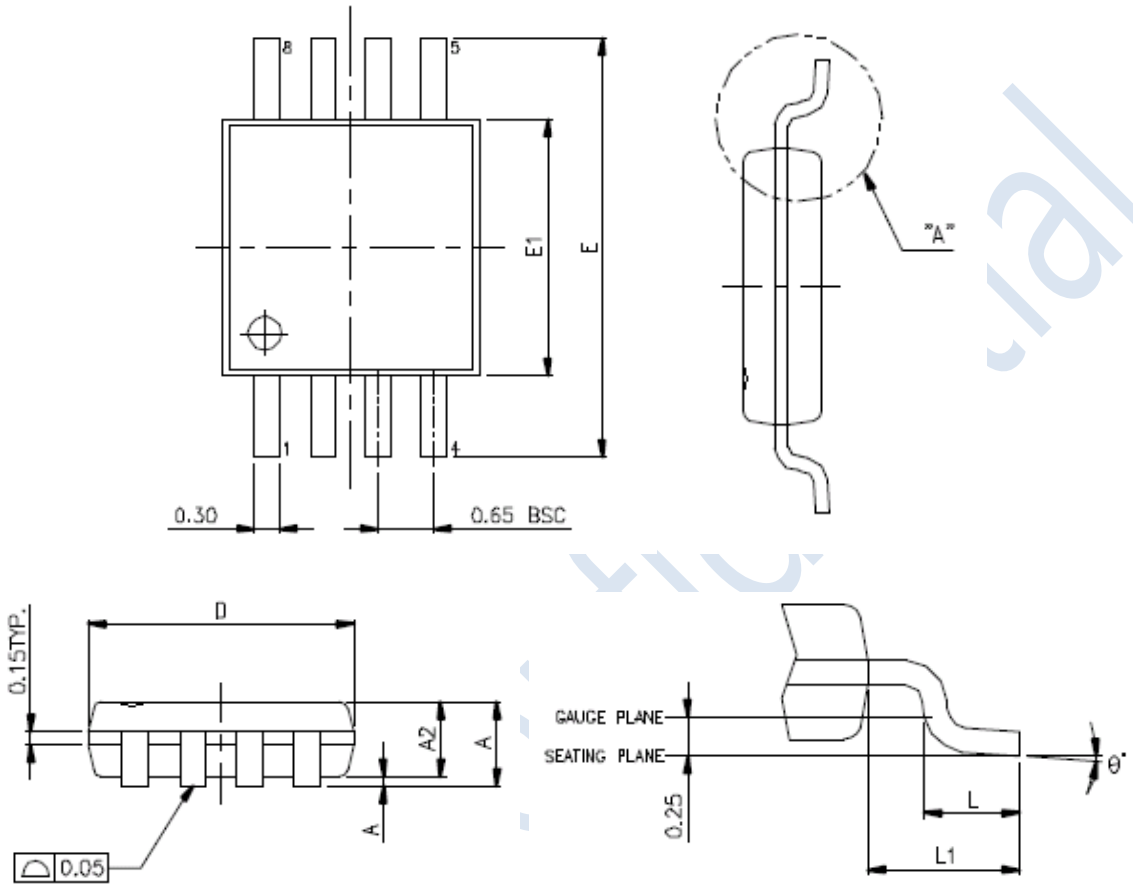
2nd Line: Assembly Code (X)+Date code(XXX)+Trace Code(X)

◯ : Pin 1 Identifier

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10 Package Spec.

MSOP-8 Package

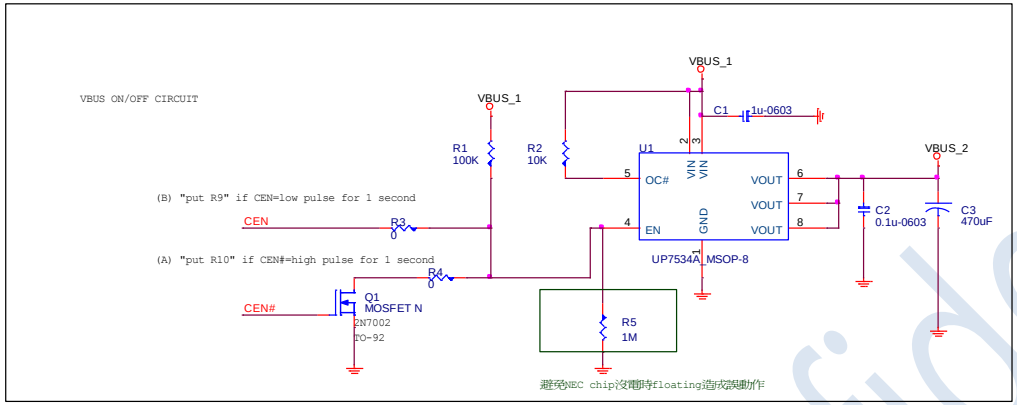


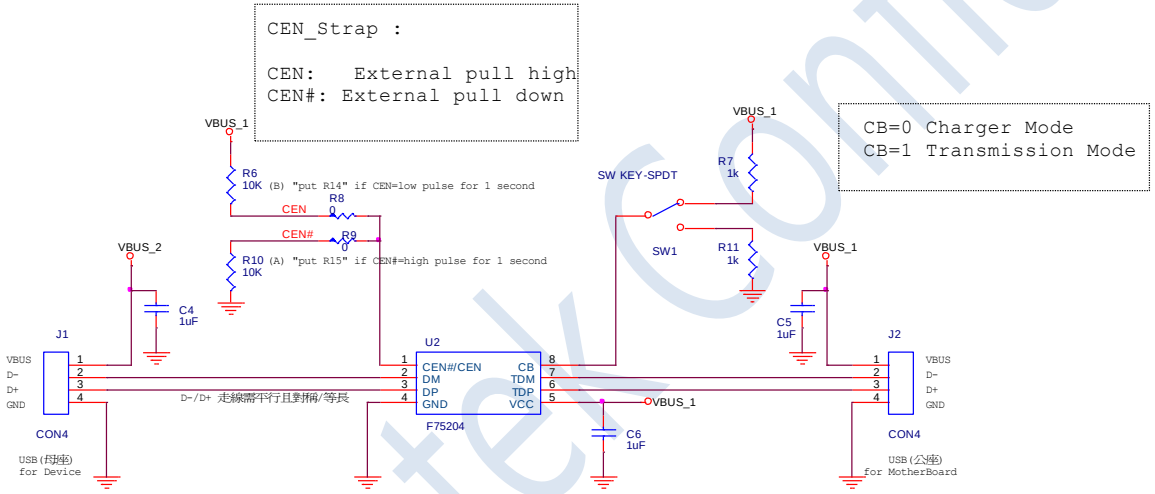
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

NOTES:
1.JEDEC OUTLINE : MO-187 AA
2.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION "0.22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "0.22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS "b" AND "E1" TO BE DETERMINED AT DATUM PLANE H .

10. Application Circuit





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Title	<F75204> Feature Integration Technology Inc.		
Size	Document Number		Rev
Custom	<Doc>		0.1
Date:	Friday, September 09, 2011	Sheet 1 of 2	