PEEL™ 22CV10AZ-25
CMOS Programmable Electrically Erasable Logic Device

Features

Ultra Low Power Operation
- V_{CC} = 5 Volts ±10%
- Icc = 10 µA (typical) at standby
- Icc = 2 mA (typical) at 1 MHz
- t_{PD} = 25ns.

CMOS Electrically Erasable Technology
- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

Development/Programmer Support
- Third party software and programmers
- Anachip PLACE Development Software

Architectural Flexibility
- 133 product terms x 44 input AND array

- Up to 22 inputs and 10 I/O pins
- 12 possible macrocell configurations
- Synchronous preset, asynchronous clear
- Independent output enables
- Programmable clock source and polarity
- 24-pin DIP/SOIC/TSSOP and 28-pin PLCC

Application Versatility
- Replaces random logic
- Pin and JEDEC compatible with 22V10
- Ideal for power-sensitive systems

General Description

The PEEL™22CV10AZ is a Programmable Electrically Erasable Logic (PEEL™) device that provides a low power alternative to ordinary PLDs. The PEEL™22CV10AZ is available in 24-pin DIP, SOIC, TSSOP and 28-pin PLCC packages (see Figure 19). A "zero-power" (100µA max. I_{CC}) standby mode makes the PEEL™22CV10AZ ideal for power sensitive applications such as handheld meters, portable communication equipment and lap- top computers/ peripherals. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves factory testability, thus ensuring the highest quality possible.

The PEEL™22CV10AZ is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e., 22CV10AZ+ & 22CV10AZ++). The additional macrocell configurations allow more logic to be put into every device, potentially reducing the design's component count and lowering the power requirements even further.

Development and programming support for the PEEL™22CV10AZ is provided by popular third-party programmers and development software. Anachip also offers free WinPLACE development software.

Figure 19 Pin Configuration

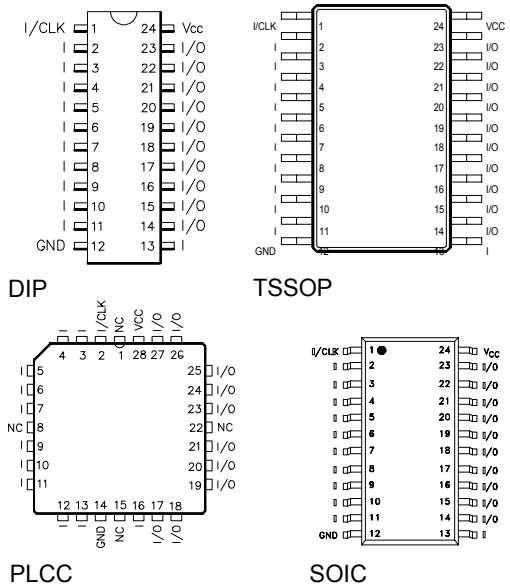
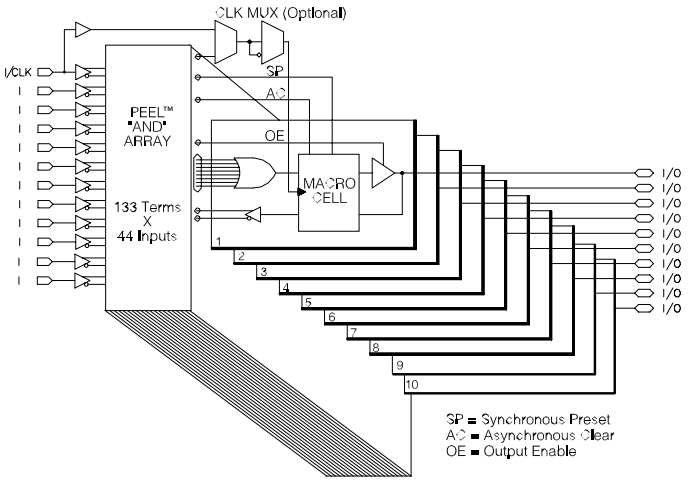


Figure 19 Block Diagram



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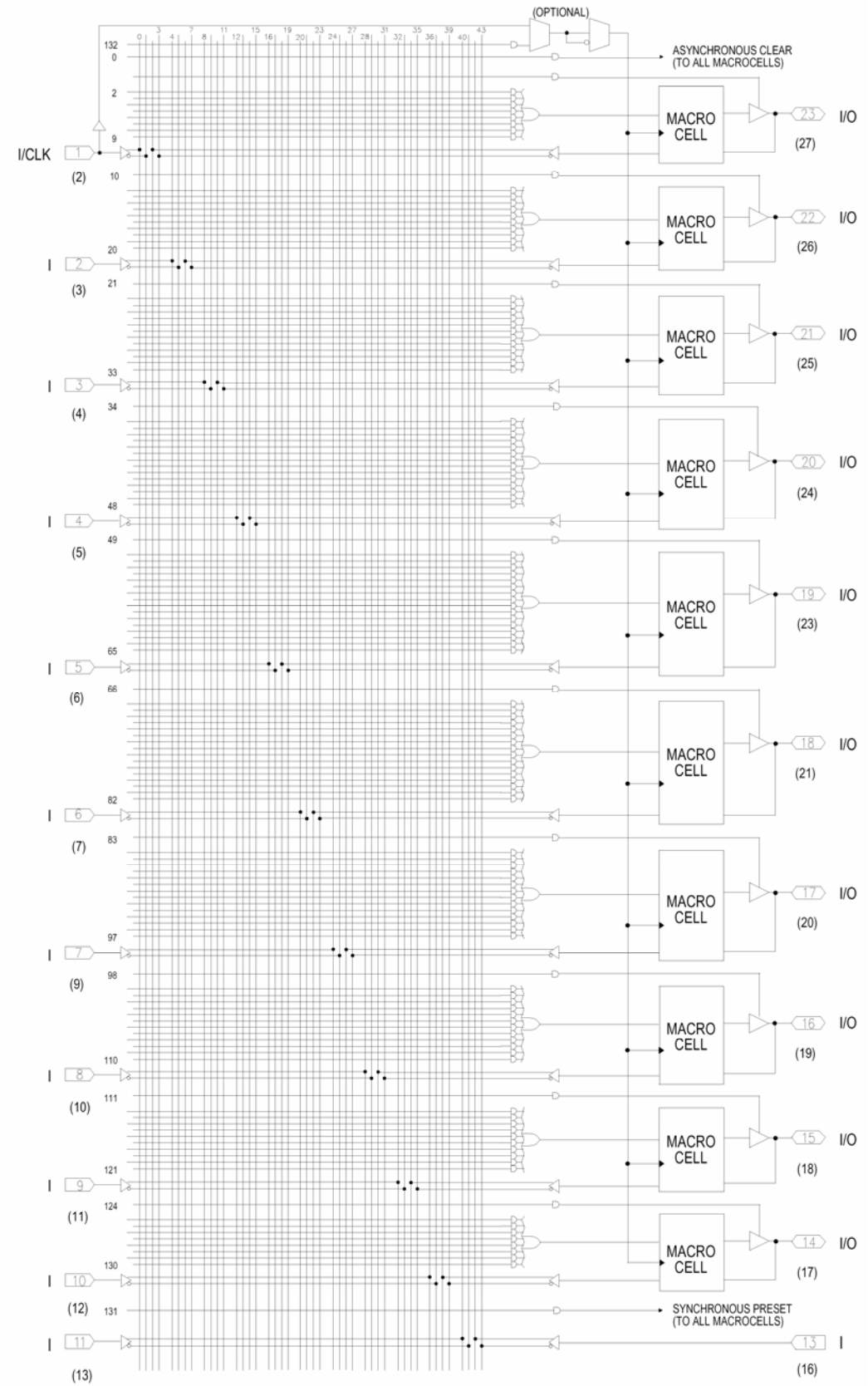


Figure 21 PEEL™22CV10AZ Logic Array Diagram

Function Description

The implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The architecture is illustrated in the block diagram of Figure 19. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creating logic functions (see Figure 21). At the core of the device is a programmable electrically-erasable AND array that drives a fixed OR array. With this structure, the PEEL™22CV10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the ten OR functions is an I/O macrocell that can be independently programmed to one of four different configurations in standard 22V10 mode, or any one of 12 configurations using the special "Plus" mode. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL™22CV10AZ (shown in Figure 21) is formed by input lines intersecting prod- uct terms. The input lines and product terms are used as follows:

44 Input Lines:

– 24 input lines carry the true and complement of the signals applied to the 12 input pins
– 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

133 Product Terms:

– 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) are used to form sum of product functions
– 10 output enable terms (one for each I/O)
– 1 global synchronous preset term
– 1 global asynchronous clear term
– 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and therefore will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL™22CV10AZ, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL™ device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

Variable Product Term Distribution

The PEEL™22CV10AZ provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Figure 21). This distribution allows optimum use of the device resources.

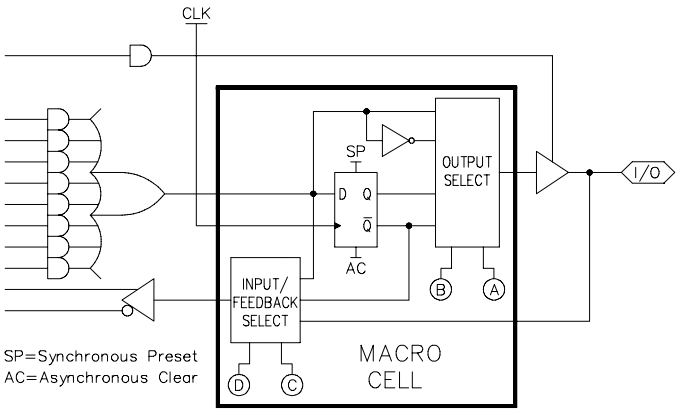
Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently lets you to tailor the configuration of the PEEL™22CV10AZ to the precise requirements of your design.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 20, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of the macrocell is determined by four EEPROM bits that control the multiplexers. These bits determine the output polarity, output type (registered or non-registered) and input-feedback path (bidirectional I/O, combinatorial feedback). Refer to Table 1. for details. Four of these macrocells duplicate the functionality of the industry-standard PAL22V10. (See Figure 21 and Table 1.)

Figure 20 Block Diagram of the PEEL™22CV10A I/O Macrocell



In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10), The macrocell provides eight additional configurations. Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 22. These structures are accessed by specifying the PEEL™22CV10A+ or PEEL™22CV10A++ option when assembling the equations.

Figure 21 Equivalent Circuits for the Four Configurations of the I/O Macrocell

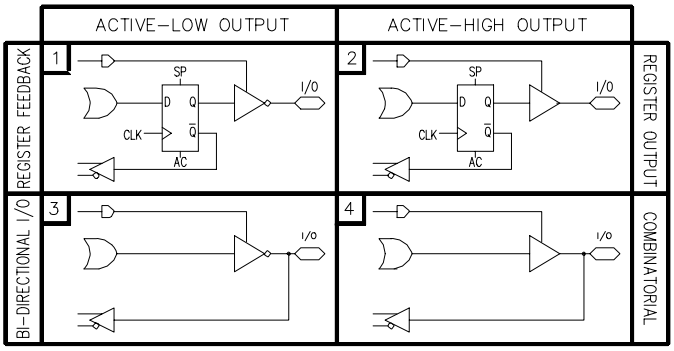


Table 1. PEEL™22CV10A Macrocell Configuration Bits

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4					Active High

When creating a PEEL™ device design, the desired macrocell configuration is generally specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register is set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear sets Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is switched into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/ O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 21), the $\overline{Q}$ output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial output (configurations 3 and 4 in Figure 21), the feedback term is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-direc- tional I/O (Refer also to Table 1.)

Programmable Clock Options

A unique feature of the PEEL™22CV10AZ is a programmable clock multiplexer that allows you to select true or complement forms of either the input pin or a product-term clock source. This feature can be accessed by specifying the PEEL™22CV10A++ option when assembling the equations.

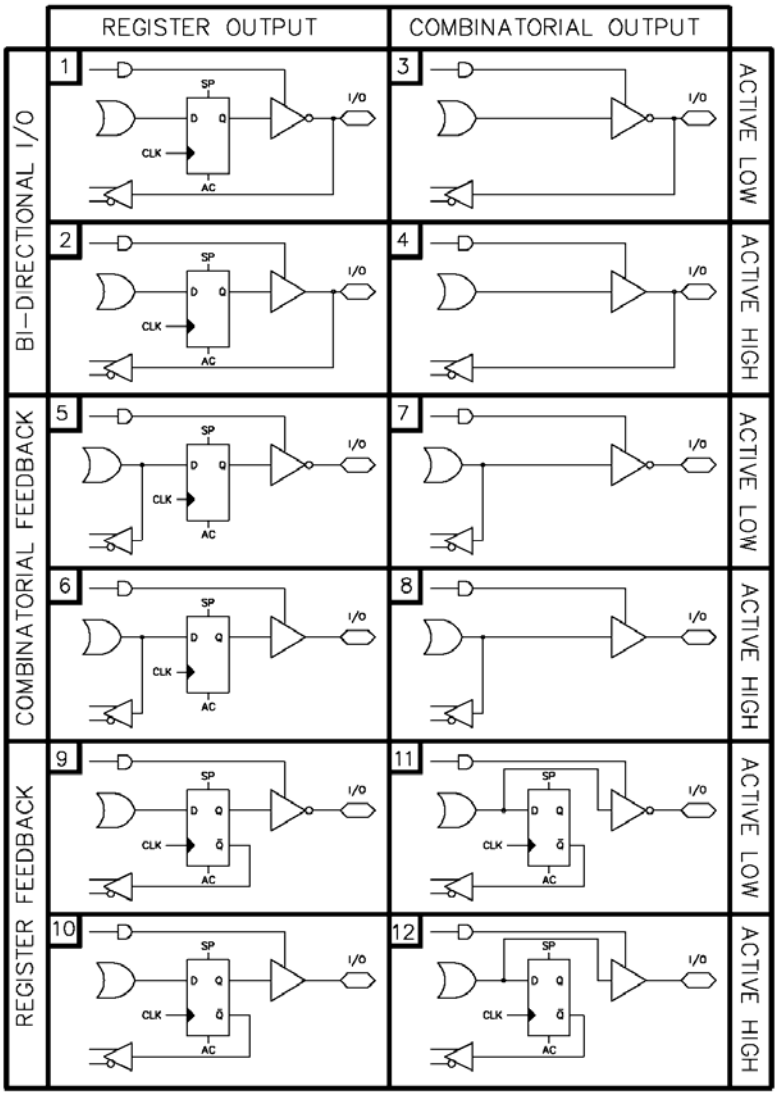


Figure 22 Equivalent Circuits for the Twelve Configurations of the PEEL™22CV10AZ+ I/O Macrocell

Table 1. I/O Macrocell Equivalent Circuits

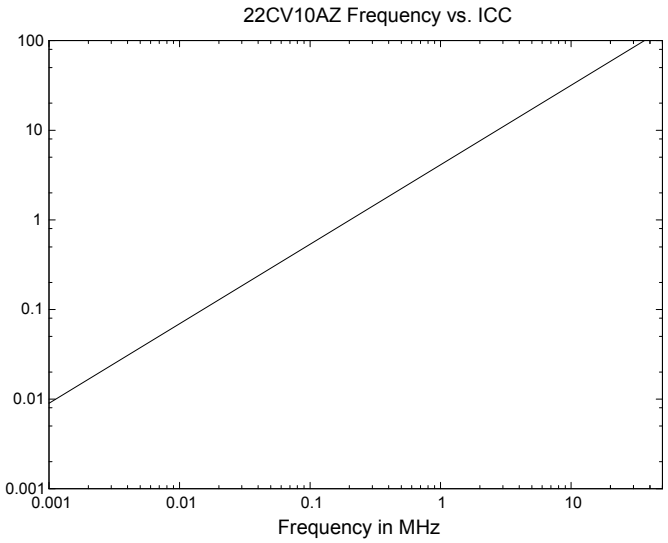
Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-directional I/O	Register	Active Low
2	1	0	1	0			Active High
3	0	1	0	0		Combinatorial	Active Low
4	1	1	0	0			Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1			Active High
7	0	1	1	1		Combinatorial	Active Low
8	1	1	1	1			Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0			Active High
11	0	1	1	0		Combinatorial	Active Low
12	1	1	1	0			Active High

Zero Power Feature

The CMOS PEEL™22CV10AZ features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately two t_{PDS}, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down.

As a result of the "Zero-Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate (see Figure 23).

Figure 23 Typical ICC vs. Input Clock Frequency for the 22CV10AZ.



Design Security

The PEEL™22CV10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL™ until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL™22CV10AZ if the PEEL™22CV10AZ+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

Programming Support

Anachip's JEDEC file translator allows easy conversion of existing 24 pin PLD designs to the PEEL™22CV10AZ, without the need for redesign. Anachip supports a broad range of popular third party design entry systems, including the Abel-to-PEEL Arrays fitter software. Anachip also offers (for free) its proprietary WinPLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers such as BP Microsystems, System General, Logical Devices, and numerous others.

This device has been designed and tested for the specified operating ranges. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to +7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to V_{CC} +0.6	V
I_O	Output Current	Per Pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Table 2. Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	°C
T_R	Clock Rise Time	See Note 3.		20	ns
T_F	Clock Fall Time	See Note 3.		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3.		250	ms

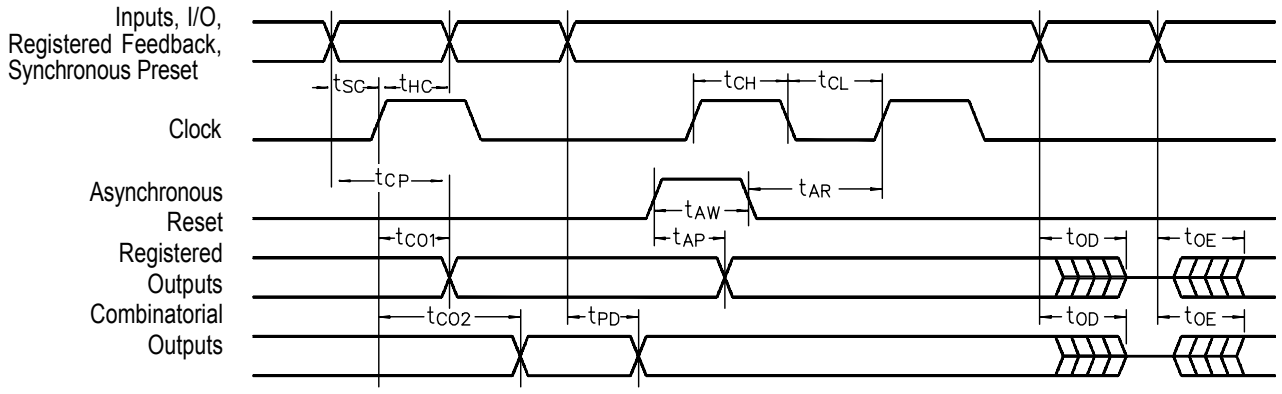
Table 3. D.C. Electrical Characteristics Over the operating range (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage – TTL	V_{CC} = Min, I_{OH} = -4.0 mA	2.4		V
V_{OHC}	Output HIGH Voltage – CMOS	V_{CC} = Min, I_{OH} = -10.0 µA	VCC-0.3		V
V_{OL}	Output LOW Voltage – TTL	V_{CC} = Min, I_{OL} = 16.0 mA		0.5	V
V_{OLC}	Output LOW Voltage – CMOS	V_{CC} = Min, I_{OL} = 10.0 µA		0.15	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.8	V
I_{IL}	Input and I/O Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}, I/O=High Z		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V, T_A = 25°C	-30	-135	mA
I_{CCS}	V_{CC} Current, Standby	V_{IN} = 0V or V_{CC}, All Outputs disabled[4]	10 (typ)	100	µA
I_{CC}[10]	V_{CC} Current, f=1MHz	V_{IN} = 0V or V_{CC}, All Outputs disabled[4]	2 (typ)	5	mA
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC}=5.0V @ f = 1MHz		6	pF
C_{OUT}[7]	Output Capacitance			12	pF

Table 10. Over the operating range [8]

Symbol	Parameter	-25		Unit
		Min	Max	
t_{PD}	Input[5] to non-registered output		25	ns
t_{OE}	Input[5] to output enable[6]		25	ns
t_{OD}	Input[5] to output disable[6]		25	ns
t_{CO1}	Clock to Output		15	ns
t_{CO2}	Clock to comb. Output delay via internal registered feedback		35	ns
t_{CF}	Clock to Feedback		9	ns
t_{SC}	Input[5] or feedback setup to clock	15		ns
t_{HC}	Input[5] hold after clock	0		ns
t_{CL}, t_{CH}	Clock low time, clock high time[8]	13		ns
t_{CP}	Min clock period Ext ($t_{SC} + t_{CO1}$)	30		ns
f_{MAX1}	Internal feedback ($1/t_{SC} + t_{CF}$)[11]	41.6		MHz
f_{MAX2}	External feedback ($1/t_{CP}$)[11]	33.3		MHz
f_{MAX3}	No feedback ($1/t_{CL}+t_{CH}$)[11]	38.4		MHz
t_{AW}	Asynchronous Reset Pulse Width	25		ns
t_{AP}	Input to Asynchronous Reset		25	ns
t_{AR}	Asynchronous Reset recovery time		25	ns
t_{RESET}	Power-on reset time for registers in clear state[12]		5	µs

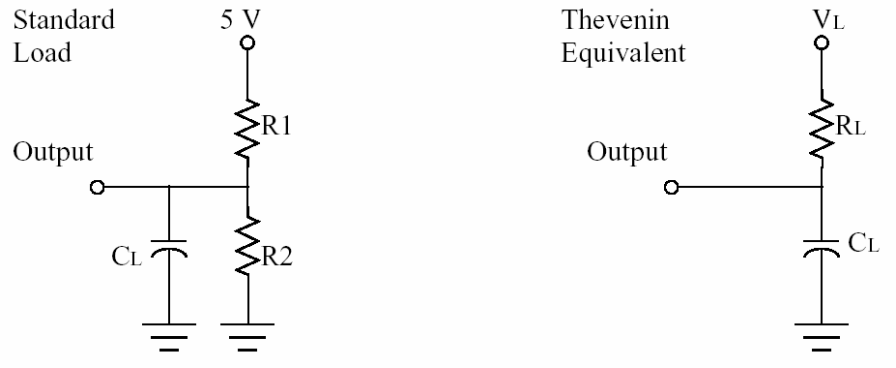
Switching Waveforms



Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. VI and VO are not specified for program/verify operation.
3. Test Points for Clock and VCC in tR and tF are referenced at the 10% and 90% levels.
4. I/O pins are 0V and VCC.
5. "Input" refers to an input pin signal.
6. tOE is measured from input transition to VREF±0.1V, TOD is measured from input transition to VOH-0.1V or VOL+0.1V; VREF=VL.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
9. Test one output at a time for a duration of less than 1 second.
10. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
11. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
12. All inputs at GND.

PEEL™ Device and Array Test Loads

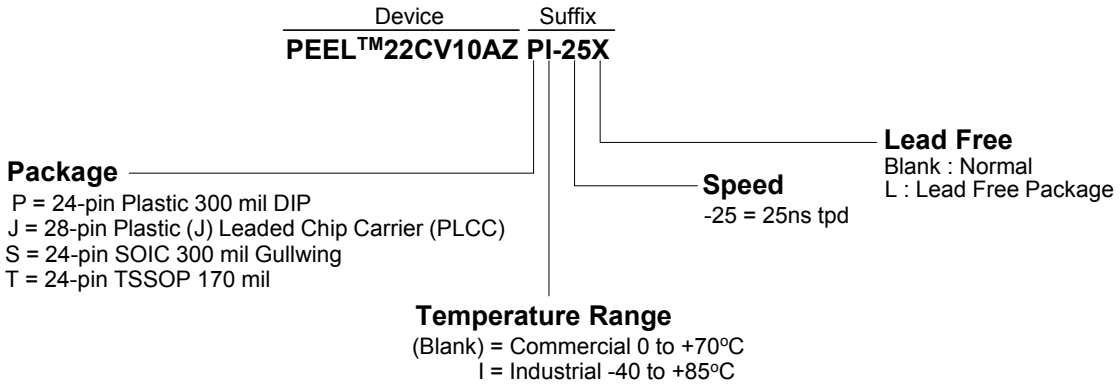


Technology	R1	R2	R_L	V_L	C_L
CMOS	480kΩ	480kΩ	228kΩ	2.375V	33pF
TTL	235Ω	159Ω	95Ω	2.02V	33pF

Ordering Information

Part Number	Speed	Temperature	Package
PEEL22CV10AZP-25 (L)	25ns	Commercial	24-pin Plastic DIP
PEEL22CV10AZJ-25 (L)	25ns	Commercial	28-pin PLCC
PEEL22CV10AZS-25 (L)	25ns	Commercial	24-pin SOIC
PEEL22CV10AZT-25 (L)	25ns	Commercial	24-pin TSSOP
PEEL22CV10AZPI-25 (L)	25ns	Industrial	24-pin Plastic DIP
PEEL22CV10AZJI-25 (L)	25ns	Industrial	28-pin PLCC
PEEL22CV10AZSI-25 (L)	25ns	Industrial	24-pin SOIC
PEEL22CV10AZTI-25 (L)	25ns	Industrial	24-pin TSSOP

Part Number



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