

N-channel TrenchMOS™ transistor

PHX23NQ10T

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching

SYMBOL



QUICK REFERENCE DATA

| |
|-------------------------------------|
| $V_{DSS} = 100\text{ V}$ |
| $I_D = 13\text{ A}$ |
| $R_{DS(ON)} \leq 70\text{ m}\Omega$ |

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full pack envelope using 'trench' technology.

Applications:-

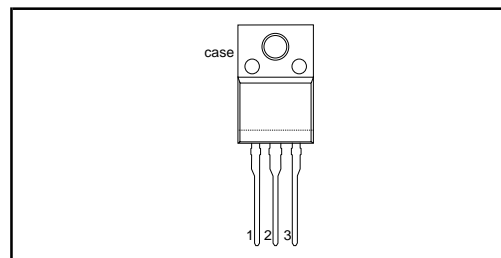
- d.c. to d.c. converters
- switched mode power supplies
- T.V. and computer monitor power supplies

The PHX23NQ10T is supplied in the SOT186A (FPAK) conventional leaded package.

PINNING

| PIN | DESCRIPTION |
|------|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| case | isolated |

SOT186A (FPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|---|------|----------|------------------|
| V_{DSS} | Drain-source voltage | $T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ | - | 100 | V |
| V_{DGR} | Drain-gate voltage | $T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 100 | V |
| V_{GS} | Gate-source voltage | | - | ± 20 | V |
| I_D | Continuous drain current | $T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$ $T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$ | - | 13 | A |
| I_{DM} | Pulsed drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 52 | A |
| P_D | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 27 | W |
| T_j, T_{stg} | Operating junction and storage temperature | | - 55 | 150 | $^\circ\text{C}$ |

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------|---------------------------------------|---|------|------|------|
| E_{AS} | Non-repetitive avalanche energy | Unclamped inductive load, $I_{AS} = 14$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25 °C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig:15 | - | 93 | mJ |
| I_{AS} | Peak non-repetitive avalanche current | | - | 23 | A |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|--|------------------------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | SOT186a package, in free air | - | - | 4.6 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | | - | 55 | - | K/W |

ELECTRICAL CHARACTERISTICS $T_j = 25$ °C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|--|----------------|-------------|-------------|--------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55$ °C | 100 89 | - - | - - | V V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 150$ °C $T_j = -55$ °C | 2 1.25 - | 3 - - | 4 - 6 | V V V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 13$ A $T_j = 150$ °C | - - | 49 115 | 70 163 | m Ω m Ω |
| I_{GSS} | Gate source leakage current | $V_{GS} = \pm 10$ V; $V_{DS} = 0$ V | - | 10 | 100 | nA |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 100$ V; $V_{GS} = 0$ V $T_j = 150$ °C | - | 0.05 | 10 500 | μ A μ A |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 23$ A; $V_{DD} = 80$ V; $V_{GS} = 10$ V | - | 22 | - | nC |
| Q_{gs} | Gate-source charge | | - | 5 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 10 | - | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD} = 50$ V; $R_D = 2.2$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load | - | 8 | - | ns |
| t_r | Turn-on rise time | | - | 39 | - | ns |
| $t_{d\ off}$ | Turn-off delay time | | - | 26 | - | ns |
| t_f | Turn-off fall time | | - | 24 | - | ns |
| L_d | Internal drain inductance | Measured from drain lead to centre of die | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz | - | 890 | 1187 | pF |
| C_{oss} | Output capacitance | | - | 139 | 167 | pF |
| C_{rss} | Feedback capacitance | | - | 83 | 109 | pF |

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

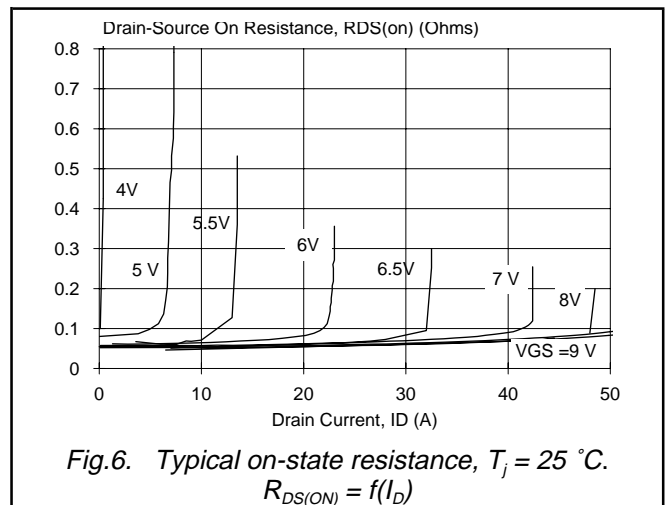
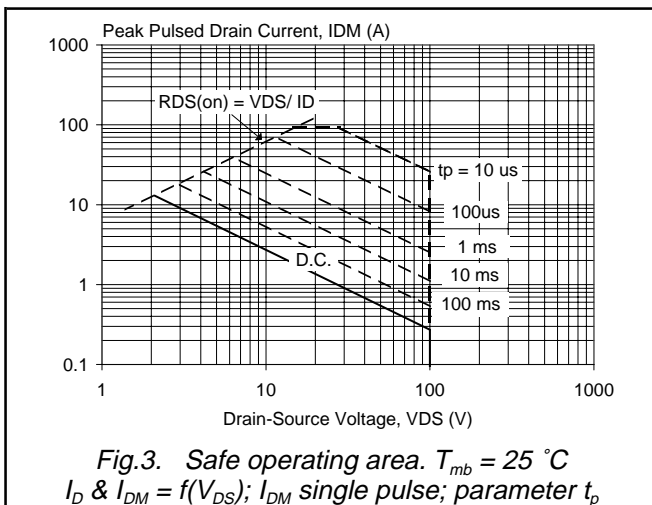
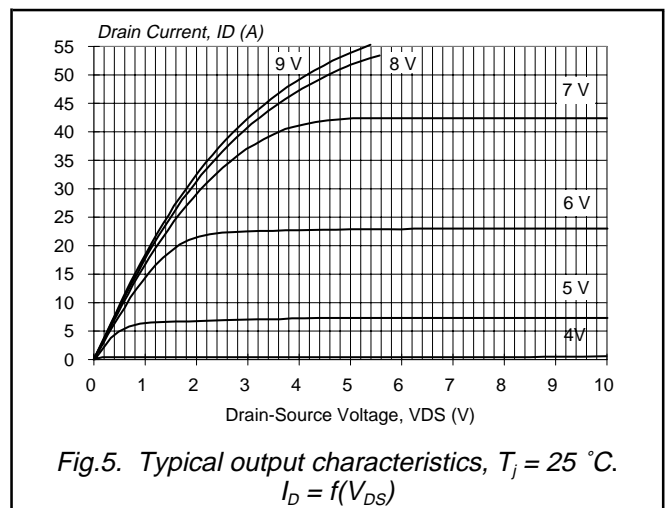
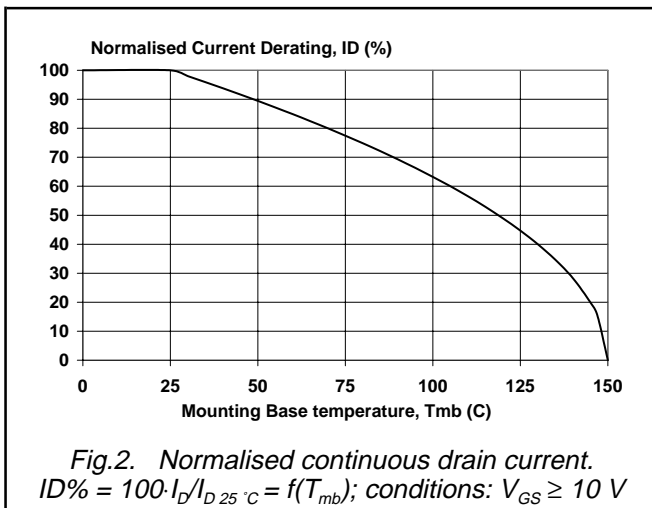
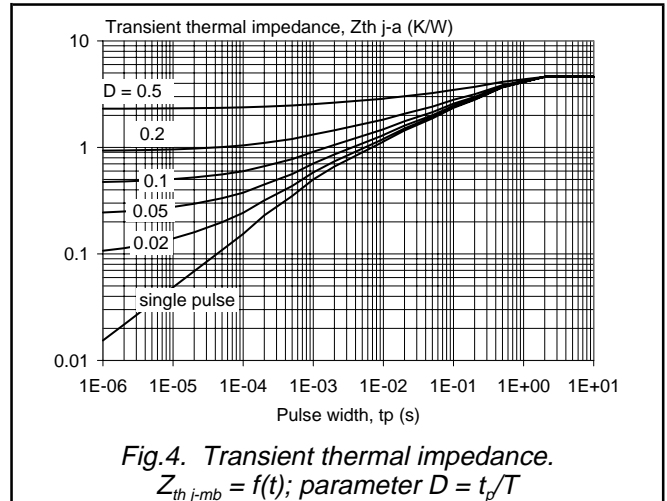
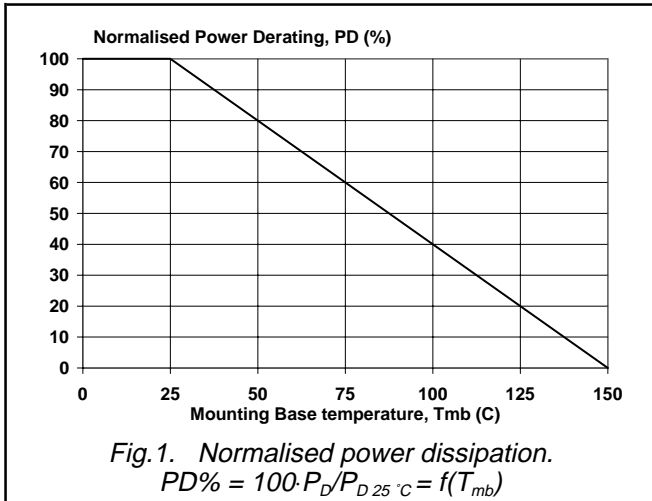
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|--|---|------|------|------|------|
| I_S | Continuous source current (body diode) | | - | - | 13 | A |
| I_{SM} | Pulsed source current (body diode) | | - | - | 92 | A |
| V_{SD} | Diode forward voltage | $I_F = 11\text{ A}; V_{GS} = 0\text{ V}$ | - | 0.9 | 1.2 | V |
| t_{rr} | Reverse recovery time | $I_F = 11\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 25\text{ V}$ | - | 64 | - | ns |
| Q_{rr} | Reverse recovery charge | | - | 120 | - | nC |

ISOLATION LIMITING VALUE & CHARACTERISTIC $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------|--|---|------|------|------|------|
| V_{isol} | R.M.S. isolation voltage from all three terminals to external heatsink | $f = 50\text{-}60\text{ Hz};$ sinusoidal waveform; R.H. $\leq 65\%$; clean and dustfree | - | | 2500 | V |
| C_{isol} | Capacitance from T2 to external heatsink | $f = 1\text{ MHz}$ | - | 10 | - | pF |

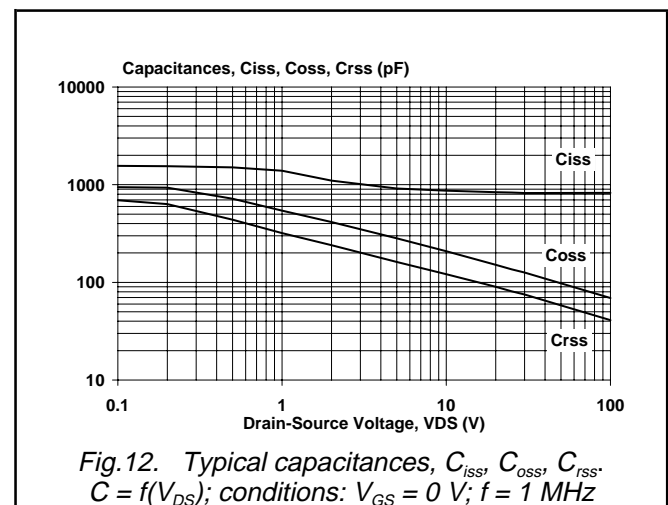
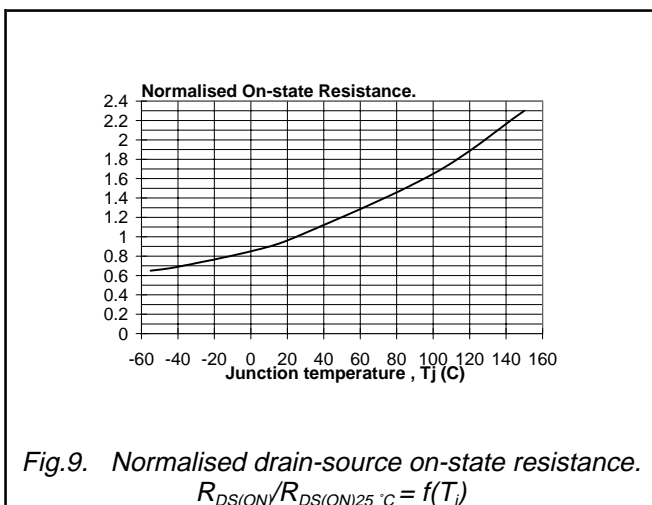
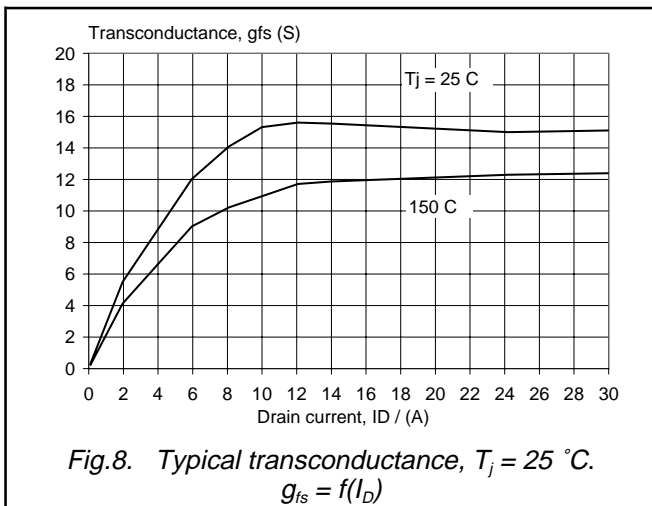
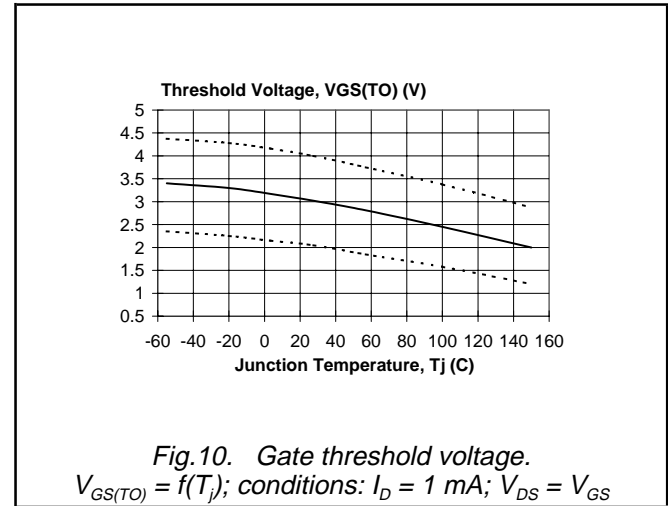
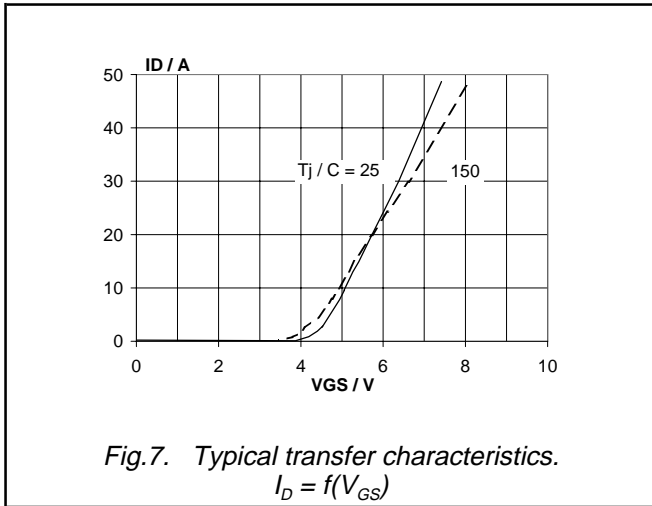
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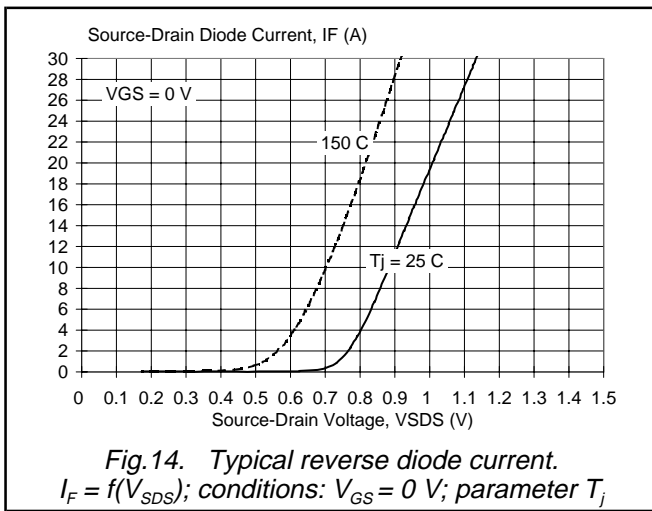
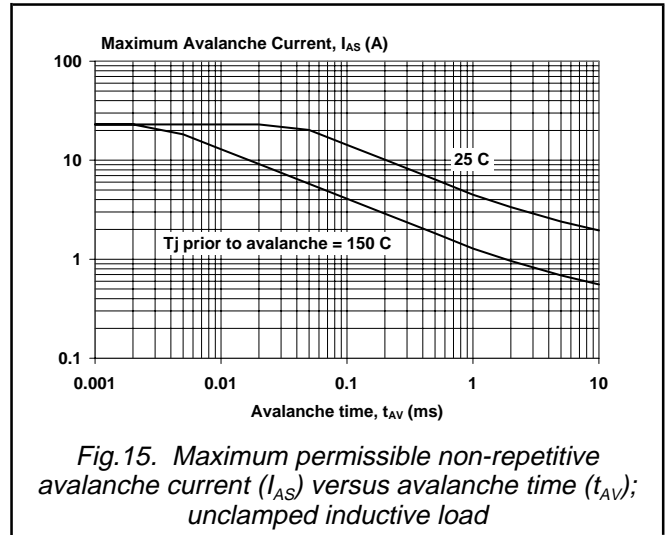
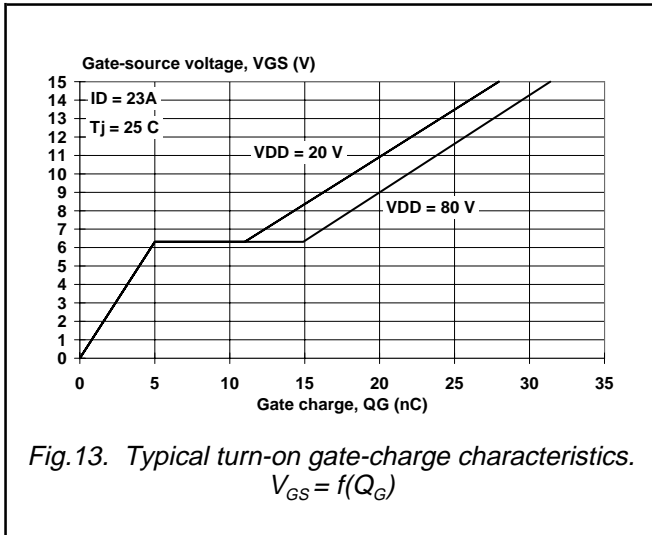
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MECHANICAL DATA

Dimensions in mm

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220

SOT186A

Net Mass: 2 g

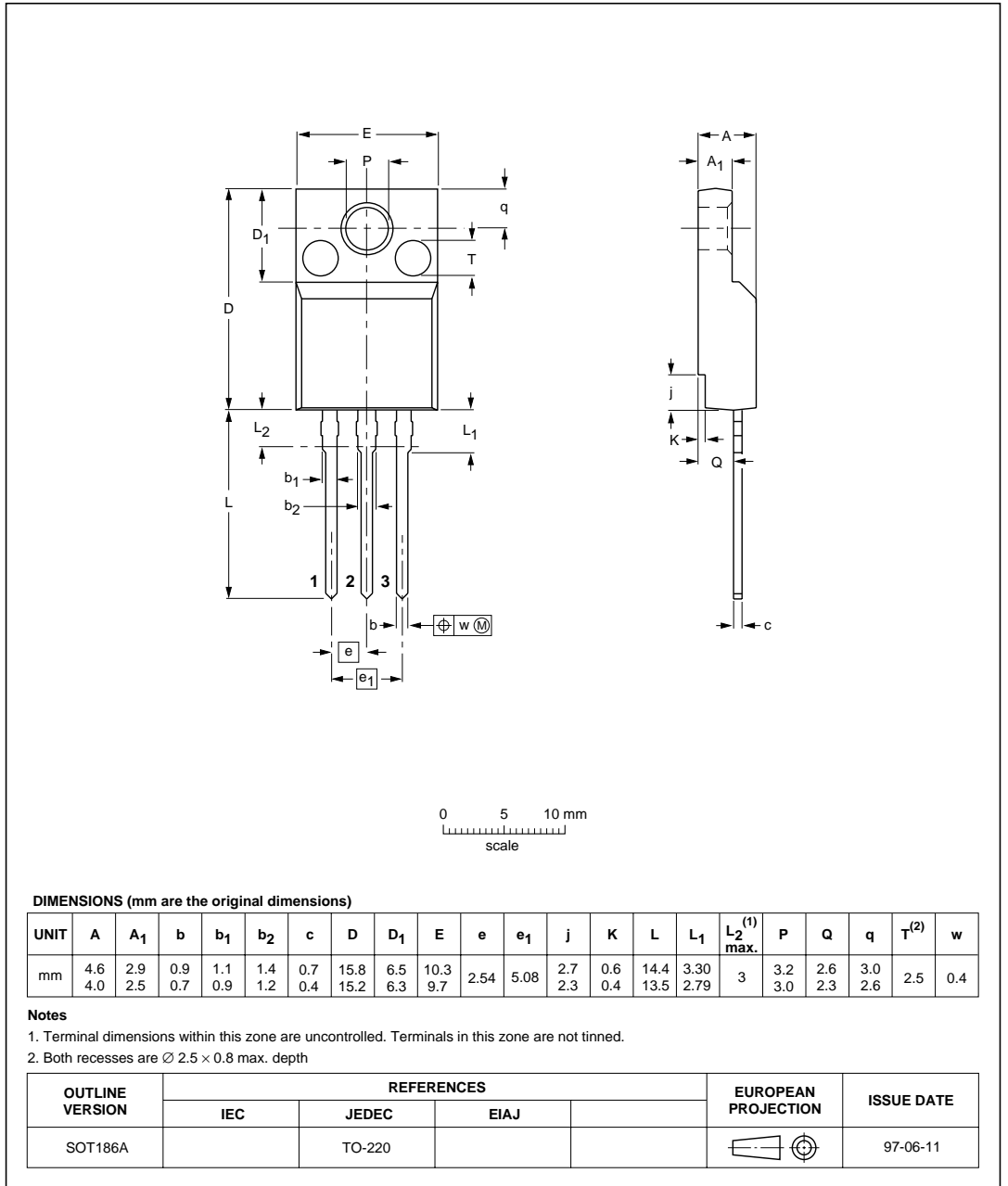


Fig. 16. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

- Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
- Refer to mounting instructions for F-pack envelopes.
- Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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