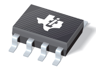


High Common-Mode Voltage Difference Amplifier

FEATURES

- **Common-Mode Voltage Range: ±275 V**
- **Minimum CMRR: 90 dB from –40°C to +125°C**
- **DC Specifications:**
  - **Maximum Offset Voltage: 1100 μV**
  - **Maximum Offset Voltage Drift: 15 μV/°C**
  - **Maximum Gain Error: 0.02%**
  - **Maximum Gain Error Drift: 10 ppm/°C**
  - **Maximum Gain Nonlinearity: 0.001% FSR**
- **AC Performance:**
  - **Bandwidth: 500 kHz**
  - **Typical Slew Rate: 5 V/μs**
- **Wide Supply Range: ±2.0 V to ±18 V**
  - **Maximum Quiescent Current: 900 μA**
  - **Output Swing on ±15-V Supplies: ±13.5 V**
- **Input Protection:**
  - **Common-Mode: ±500 V**
  - **Differential: ±500 V**

APPLICATIONS

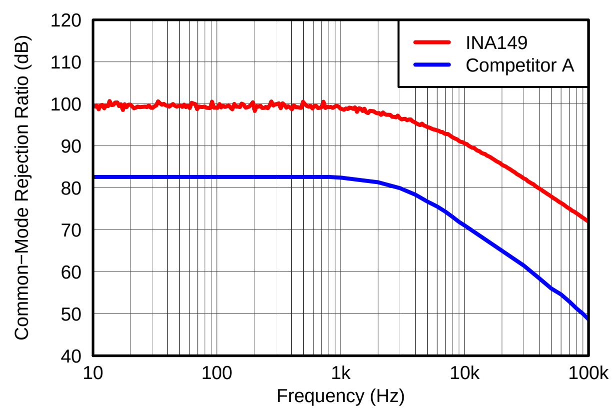
- **High-Voltage Current Sensing**
- **Battery Cell Voltage Monitoring**
- **Power-Supply Current Monitoring**
- **Motor Controls**
- **Replacement for Isolation Circuits**

DESCRIPTION

The INA149 is a precision unity-gain difference amplifier with a very high input common-mode voltage range. It is a single, monolithic device that consists of a precision op amp and an integrated thin-film resistor network. The INA149 can accurately measure small differential voltages in the presence of common-mode signals up to ±275 V. The INA149 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

In many applications, where galvanic isolation in not required, the INA149 can replace isolation amplifiers. This ability can eliminate costly isolated input side power supplies and the associated ripple, noise, and quiescent current. The excellent 0.0005% nonlinearity and 500-kHz bandwidth of the INA149 are superior to those of conventional isolation amplifiers.

The INA149 is pin-compatible with the INA117 and INA148 type high common-mode voltage amplifiers and offers improved performance over both devices. The INA149 is available in the SOIC-8 package with operation specified over the extended industrial temperature range of –40°C to +125°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA149	SOIC-8	D	INA149AID

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		INA149	UNIT
Supply voltage	(V+) – (V–)	40	V
Input voltage range	Continuous	300	V
Common-mode and differential, 10 s		500	V
Maximum Voltage on REF_A and REF_B		(V–) – 0.3 to (V+) + 0.3	V
Input current on any input pin(2)		10	mA
Output short-circuit current duration		Indefinite	
Operating temperature range		–55 to +150	°C
Storage temperature range		–65 to +150	°C
Junction temperature		+150	°C
ESD rating	Human body model (HBM)	1500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) REF_A and REF_B are diode clamped to the power-supply rails. Signals applied to these pins that can swing more than 0.3 V beyond the supply rails should be limited to 10 mA or less.

ELECTRICAL CHARACTERISTICS: V+ = +15 V and V– = –15 V

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_{CM} = REF_A = REF_B = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA149 MIN	TYP	MAX	UNIT
GAIN						
	Initial	V_{OUT} = ±10.0 V		1		V/V
	Gain error	V_{OUT} = ±10.0 V		±0.005	±0.02	%FSR
	Gain	vs temperature, T_A = –40°C to +125°C		±1.5	±10	ppm/°C
	Nonlinearity			±0.0005	±0.001	%FSR
OFFSET VOLTAGE						
	Initial offset			350	1100	μV
		vs temperature, T_A = –40°C to +125°C		3	15	μV/°C
		vs supply (PSRR), V_S = ±2 V to ±18 V	90	120		dB
INPUT						
	Impedance	Differential		800		kΩ
		Common-mode		200		kΩ
	Voltage range	Differential	–13.5		13.5	V
		Common-mode	–275		275	V
	Common-mode rejection (CMRR)	At dc, V_{CM} = ±275 V	90	100		dB
		vs temperature, T_A = –40°C to +125°C, at dc	90			dB
		At ac, 500 Hz, V_{CM} = 500 V_{PP}	90			dB
		At ac, 1 kHz, V_{CM} = 500 V_{PP}		90		dB
OUTPUT						
	Voltage range		–13.5		13.5	V
	Short-circuit current			±25		mA
	Capacitive load drive	No sustained oscillations		10		nF
OUTPUT NOISE VOLTAGE						
	0.01 Hz to 10 Hz			20		$μV_{PP}$
	10 kHz			550		$nV/\sqrt{Hz}$
DYNAMIC RESPONSE						
	Small-signal bandwidth			500		kHz
	Slew rate	V_{OUT} = ±10-V step	1.7	5		V/μs
	Full-power bandwidth	V_{OUT} = 20 V_{PP}		32		kHz
	Settling time	0.01%, V_{OUT} = 10-V step		7		μs
POWER SUPPLY						
	Voltage range		±2		±18	V
	Quiescent current	V_S = ±18 V, V_{OUT} = 0 V		810	900	μA
		vs temperature, T_A = –40°C to +125°C			1.1	mA
TEMPERATURE RANGE						
	Specified		–40		+125	°C
	Operating		–55		+150	°C
	Storage		–65		+150	°C

ELECTRICAL CHARACTERISTICS: V+ = 5 V and V– = 0 V

At T_A = +25°C, R_L = 2 kΩ connected to 2.5 V, and V_{CM}= REF_A = REF_B = 2.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA149 MIN	INA149 TYP	INA149 MAX	UNIT
GAIN						
	Initial	V_{OUT} = 1.5 V to 3.5 V		1		V/V
	Gain error	V_{OUT} = 1.5 V to 3.5 V		±0.005		%FSR
	Gain	vs temperature, T_A = –40°C to +125°C		±1.5		ppm/°C
	Nonlinearity			±0.0005		%FSR
OFFSET VOLTAGE						
	Initial offset			350		μV
		vs temperature, T_A = –40°C to +125°C		3		μV/°C
		vs supply (PSRR), V_S = 4 V to 5 V		120		dB
INPUT						
	Impedance	Differential		800		kΩ
		Common-mode		200		kΩ
	Voltage range	Differential	1.5		3.5	V
		Common-mode	–20		25	V
	Common-mode rejection	At dc, V_{CM} = –20 V to 25 V		100		dB
		vs temperature, T_A = –40°C to +125°C, at dc		100		dB
		At ac, 500 Hz, V_{CM} = 49 V_{PP}		100		dB
		At ac, 1 kHz, V_{CM} = 49 V_{PP}		90		dB
OUTPUT						
	Voltage range		1.5		3.5	V
	Short-circuit current			±15		mA
	Capacitive load drive	No sustained oscillations		10		nF
OUTPUT NOISE VOLTAGE						
	0.01 Hz to 10 Hz			20		$μV_{PP}$
	10 kHz			550		nV/√Hz
DYNAMIC RESPONSE						
	Small-signal bandwidth			500		kHz
	Slew rate	V_{OUT} = 2 V_{PP} step		5		V/μs
	Full-power bandwidth	V_{OUT} = 2 V_{PP}		32		kHz
	Settling time	0.01%, V_{OUT} = 2 V_{PP} step		7		μs
POWER SUPPLY						
	Voltage range			5		V
	Quiescent current	V_S = 5 V		810		μA
		vs temperature, T_A = –40°C to +125°C		1		mA

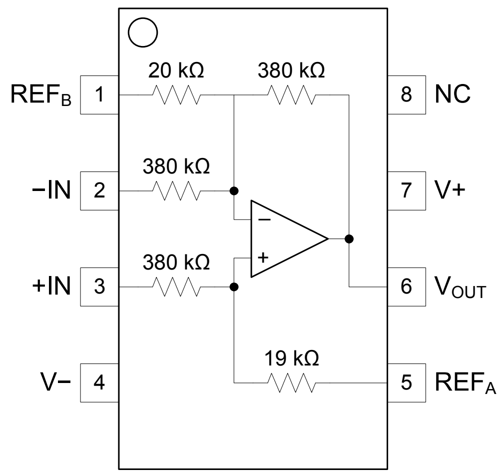
THERMAL INFORMATION

THERMAL METRIC(1)		INA149 D (SOIC) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	110	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57	
θ_{JB}	Junction-to-board thermal resistance	54	
ψ_{JT}	Junction-to-top characterization parameter	11	
ψ_{JB}	Junction-to-board characterization parameter	53	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATION

D PACKAGE
SOIC-8
(TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
–IN	2	Inverting input
+IN	3	Noninverting input
NC	8	No internal connection
REF_A	5	Reference input
REF_B	1	Reference input
V–	4	Negative power supply
V+	7	Positive power supply(1)
V_{OUT}	6	Output

(1) In this document, (V+) – (V–) is referred to as V_S.

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

CMRR vs FREQUENCY

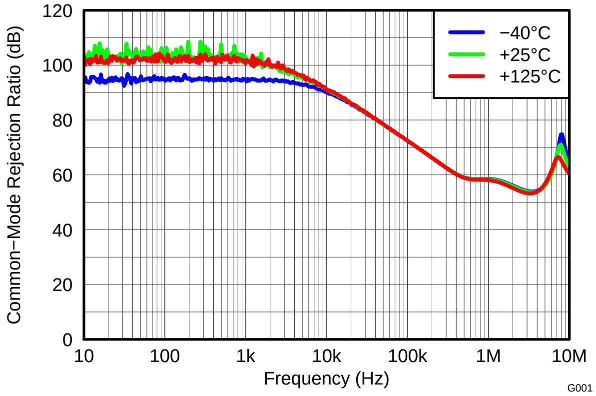


Figure 1.

COMMON-MODE REJECTION

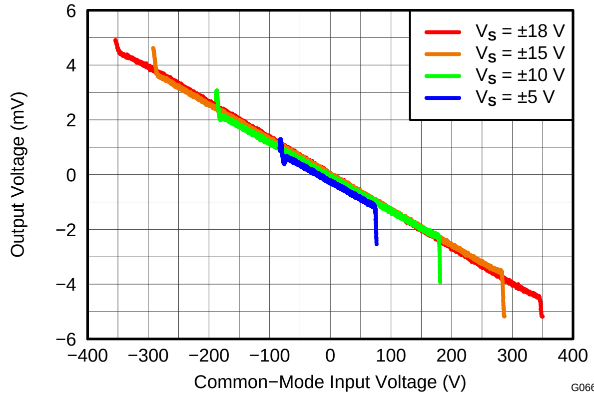


Figure 2.

COMMON-MODE OPERATING RANGE vs POWER-SUPPLY VOLTAGE

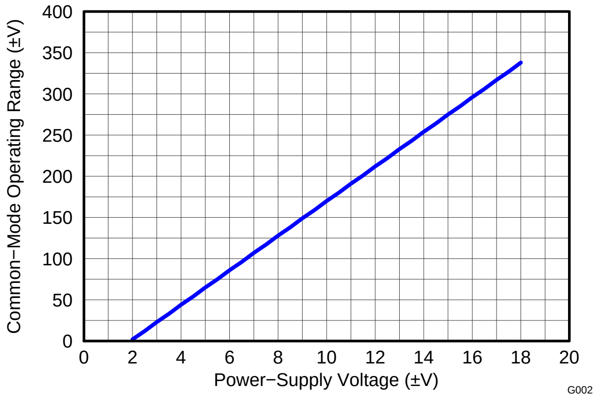


Figure 3.

TYPICAL GAIN ERROR FOR R_L = 10 kΩ (Curves Offset for Clarity)

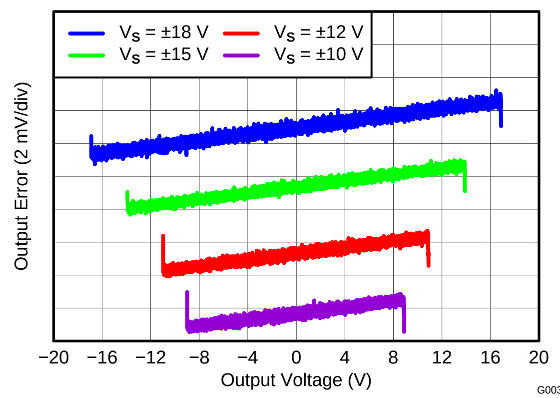


Figure 4.

TYPICAL GAIN ERROR FOR R_L = 2 kΩ (Curves Offset for Clarity)

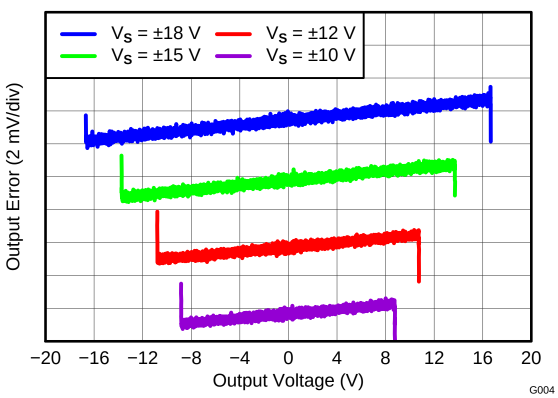


Figure 5.

TYPICAL GAIN ERROR FOR R_L = 1 kΩ (Curves Offset for Clarity)

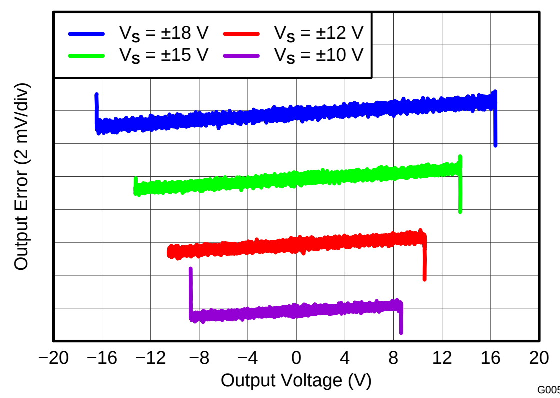


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

TYPICAL GAIN ERROR FOR LOW SUPPLY VOLTAGES (Curves Offset for Clarity)

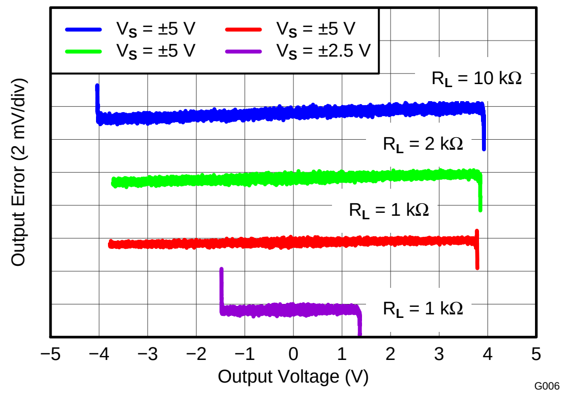


Figure 7.

GAIN NONLINEARITY

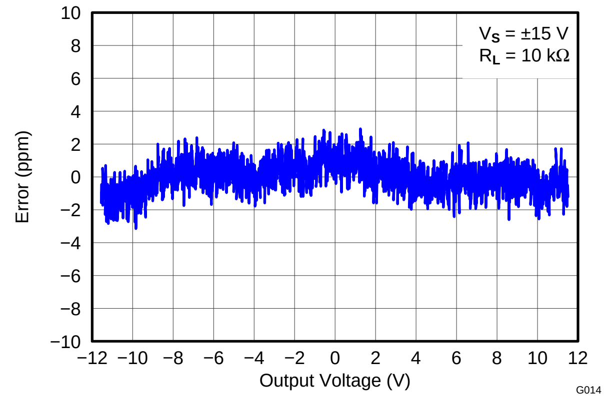


Figure 8.

GAIN NONLINEARITY

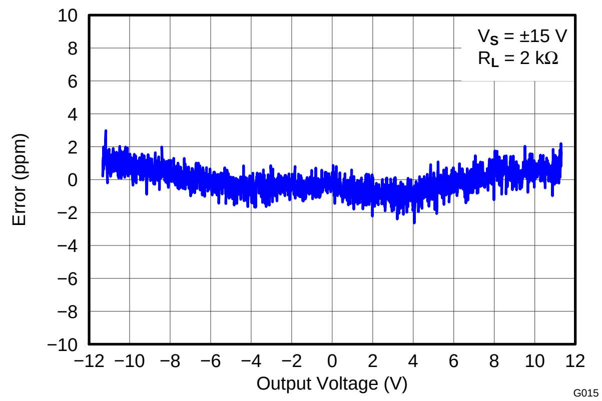


Figure 9.

GAIN NONLINEARITY

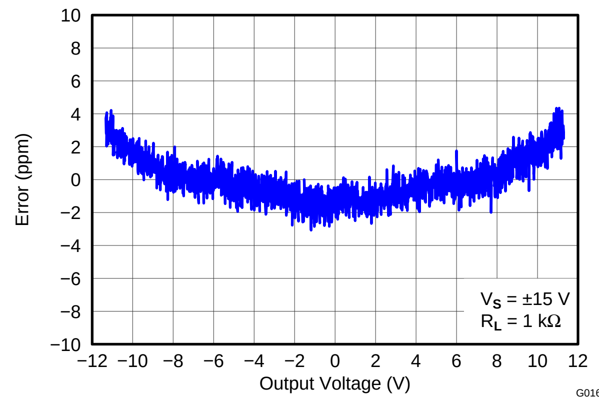


Figure 10.

GAIN NONLINEARITY

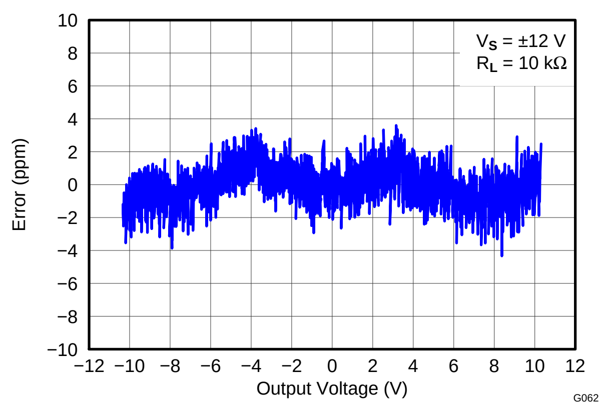


Figure 11.

OUTPUT VOLTAGE vs LOAD CURRENT

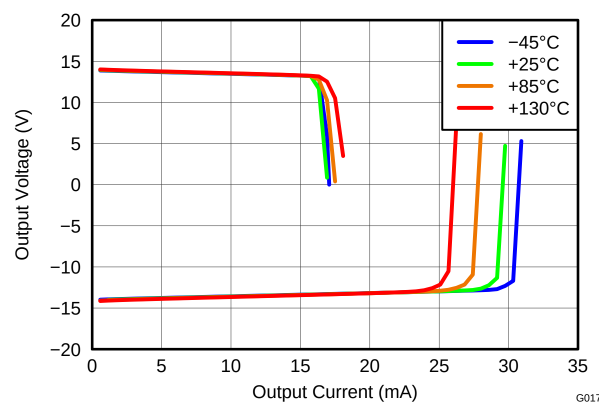


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

GAIN vs FREQUENCY

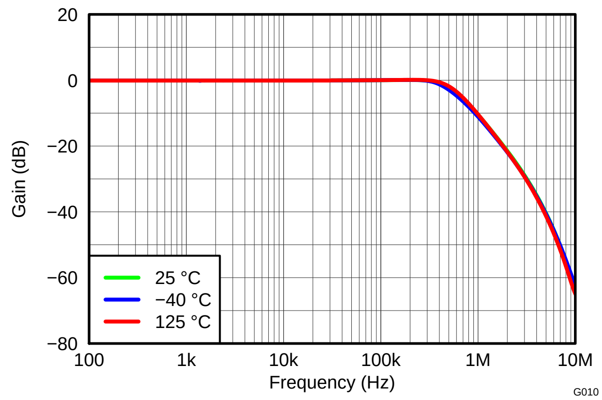


Figure 13.

NOISE SPECTRAL DENSITY vs FREQUENCY

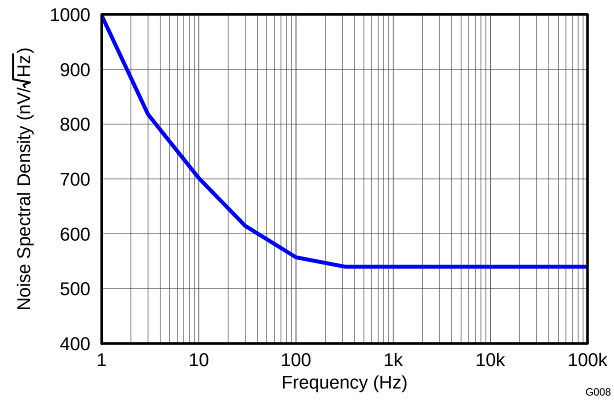


Figure 14.

0.01 Hz TO 10 Hz NOISE

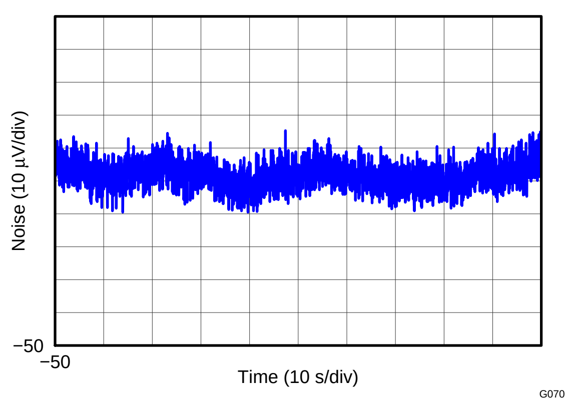


Figure 15.

POSITIVE PSRR vs FREQUENCY

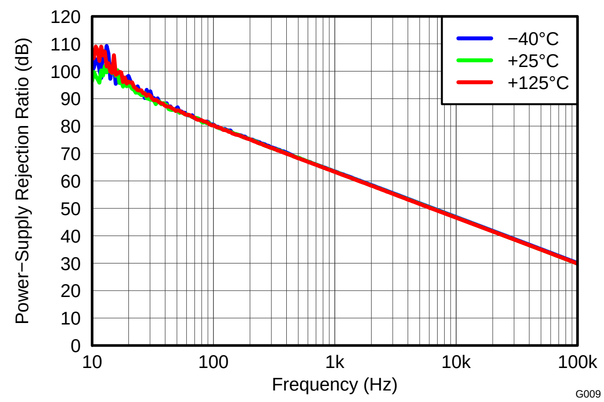


Figure 16.

NEGATIVE PSRR vs FREQUENCY

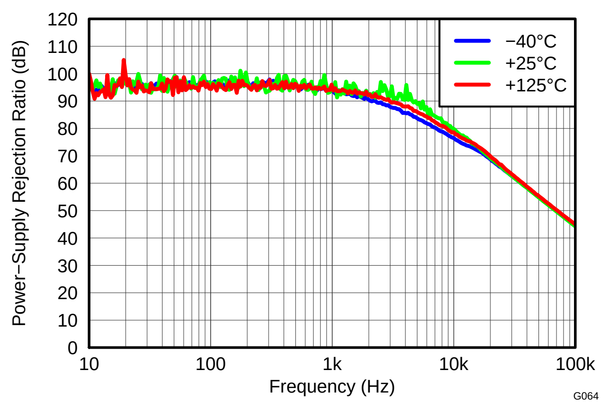


Figure 17.

MAXIMUM POWER DISSIPATION vs TEMPERATURE

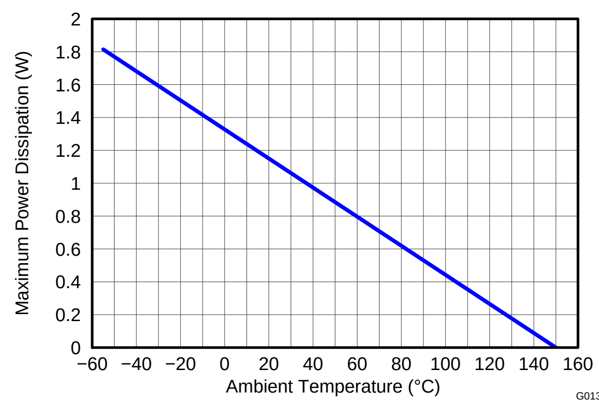


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

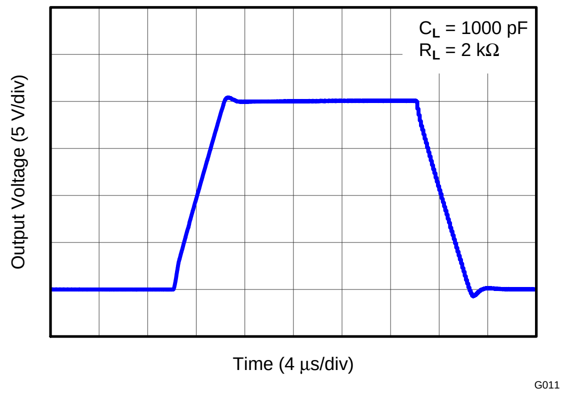


Figure 19.

SMALL-SIGNAL STEP RESPONSE

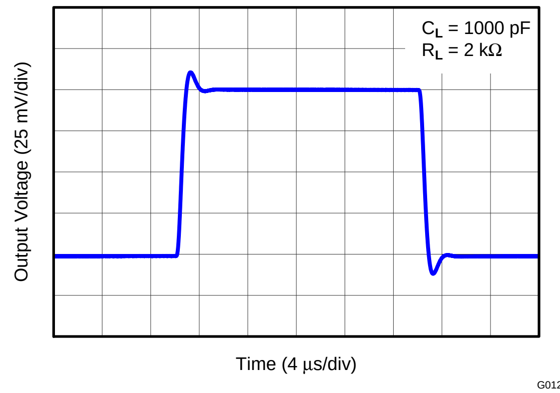


Figure 20.

SMALL-SIGNAL RESPONSE vs CAPACITIVE LOAD

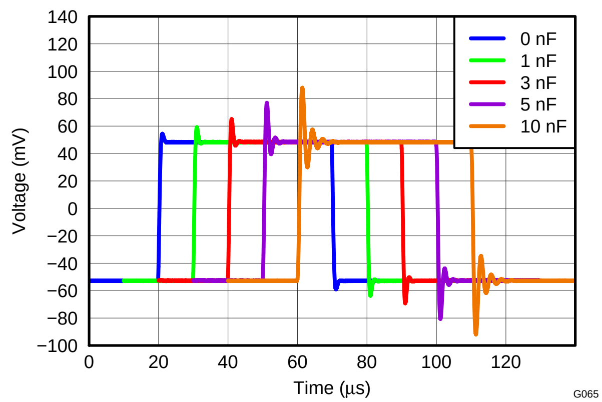


Figure 21.

SETTLING TIME

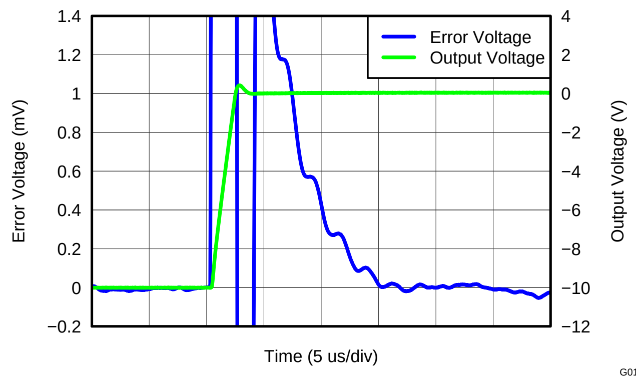


Figure 22.

SETTLING TIME

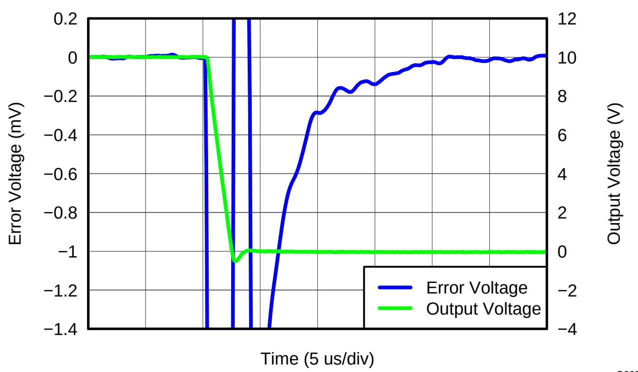


Figure 23.

CMRR HISTOGRAM

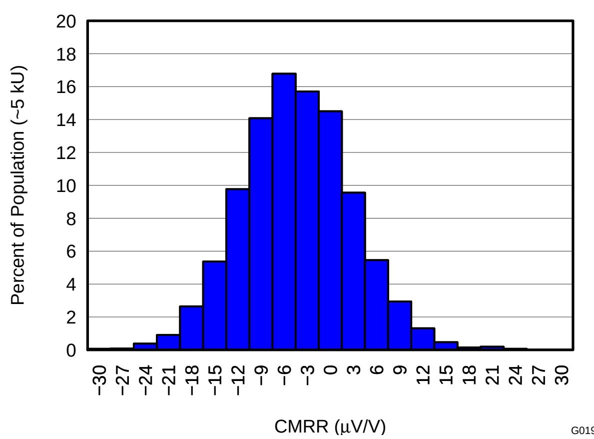


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

OFFSET VOLTAGE HISTOGRAM

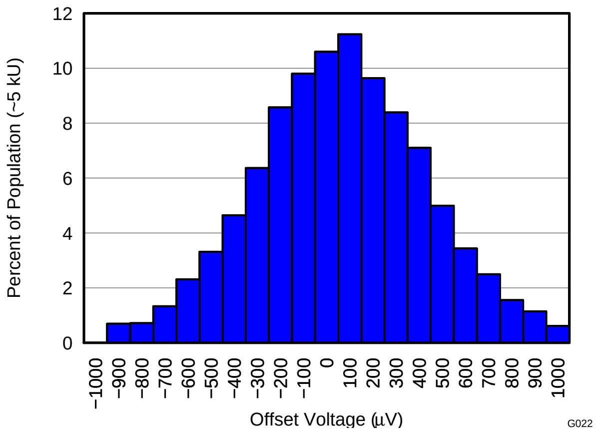


Figure 25.

DIFFERENTIAL GAIN ERROR HISTOGRAM

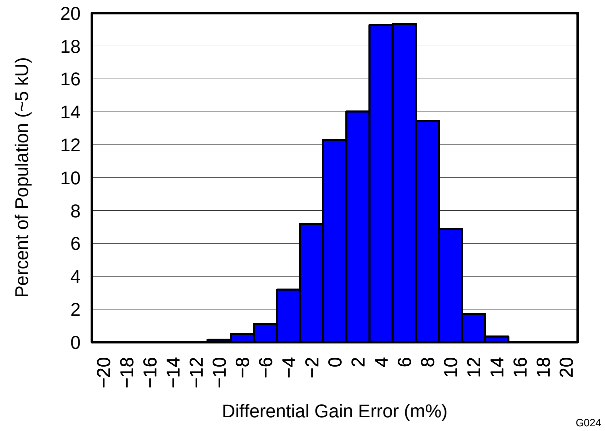


Figure 26.

PSRR HISTOGRAM

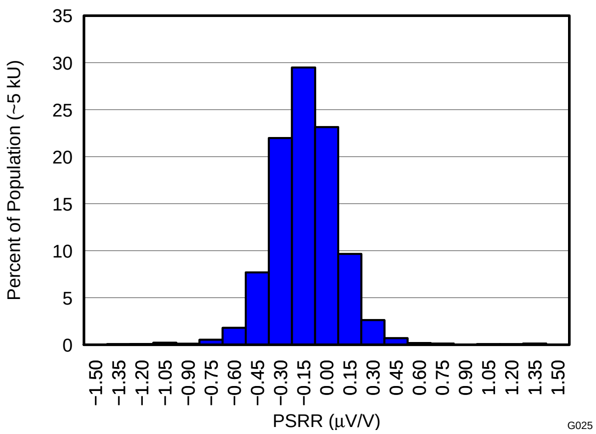


Figure 27.

GAIN NONLINEARITY HISTOGRAM

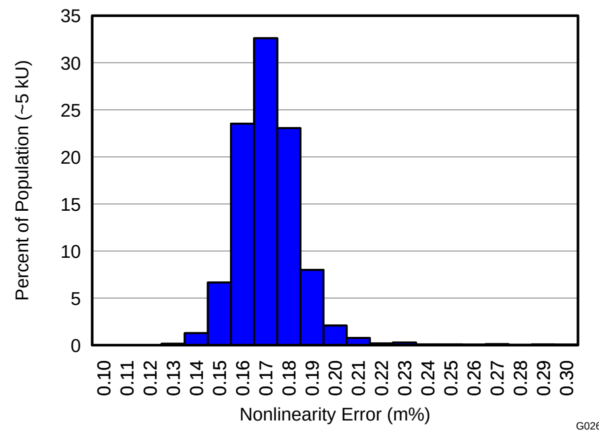


Figure 28.

OFFSET VOLTAGE vs TEMPERATURE

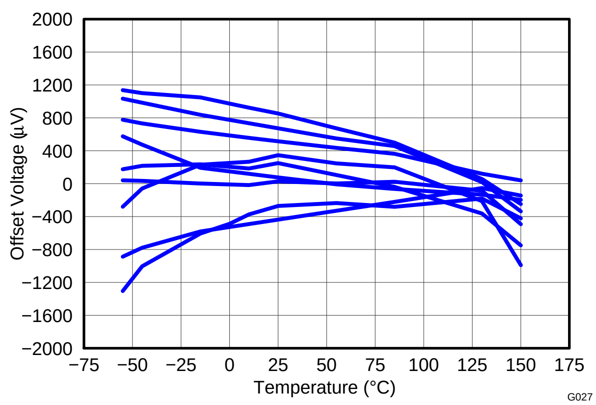


Figure 29.

CMRR vs TEMPERATURE

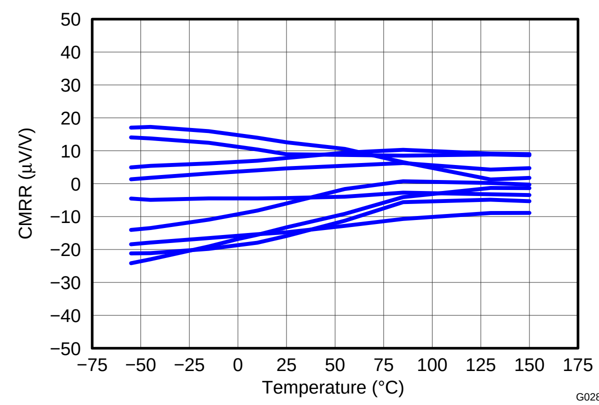


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

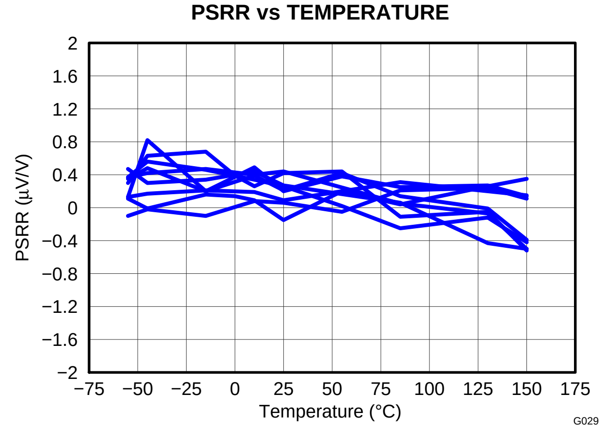


Figure 31.

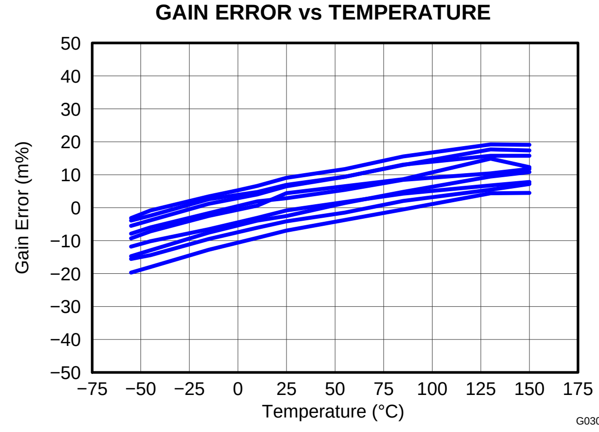


Figure 32.

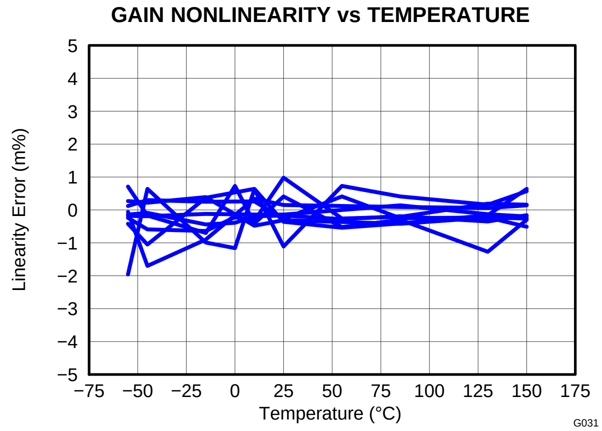


Figure 33.

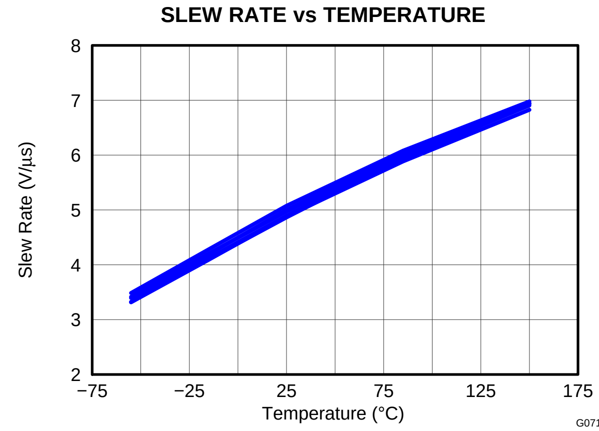


Figure 34.

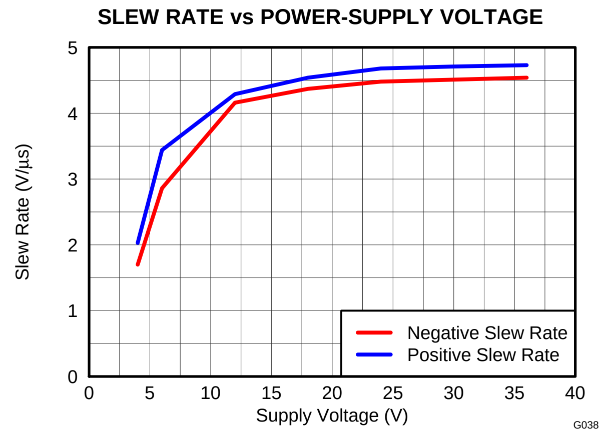


Figure 35.

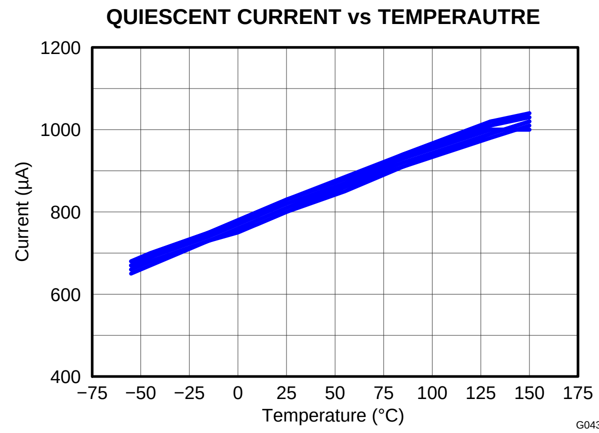


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 2 kΩ connected to ground, and V_S = ±15 V, unless otherwise noted.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

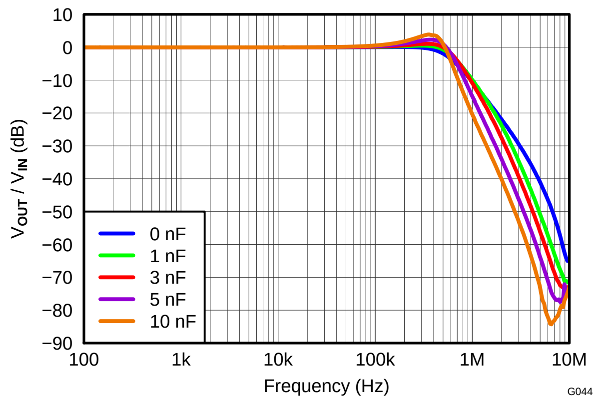


Figure 37.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

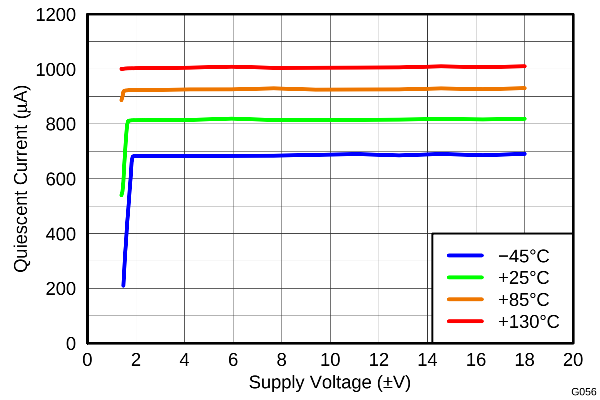


Figure 38.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

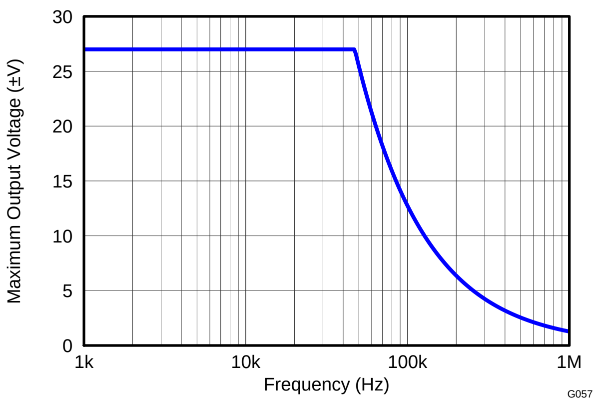


Figure 39.

OVERLOAD RECOVERY

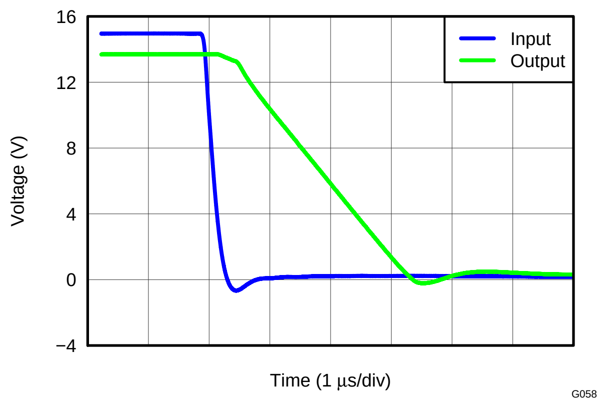


Figure 40.

OVERLOAD RECOVERY

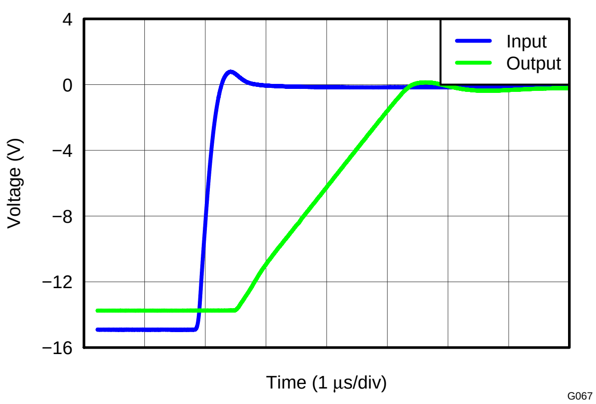


Figure 41.

QUIESCENT CURRENT HISTOGRAM

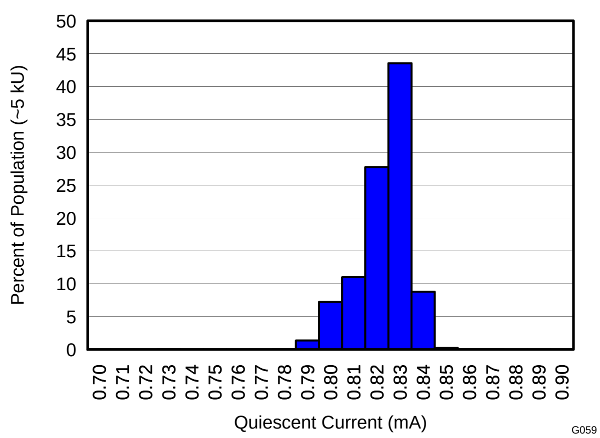


Figure 42.

APPLICATION INFORMATION

BASIC INFORMATION

Figure 43 shows the basic connections required for dual-supply operation. Applications with noisy or high-impedance power-supply lines may require decoupling capacitors placed close to the device pins. The output voltage is equal to the differential input voltage between pins 2 and 3. The common-mode input voltage is rejected. Figure 44 shows the basic connections required for single-supply operation.

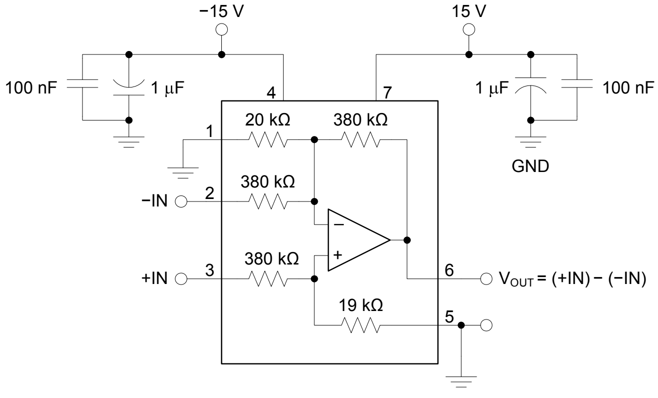


Figure 43. Basic Power and Signal Connections for Dual-Supply Operation

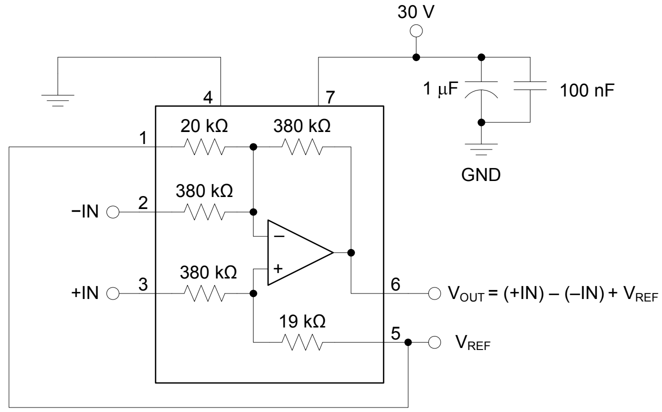


Figure 44. Basic Power and Signal Connections for Single-Supply Operation

TRANSFER FUNCTION

Most applications use the INA149 as a simple unity-gain difference amplifier. The transfer function is given in Equation 1:

$$V_{OUT} = (+IN) - (-IN) \quad (1)$$

Some applications, however, apply voltages to the reference terminals (REF_A and REF_B). The complete transfer function is given in Equation 2:

$$V_{OUT} = (+IN) - (-IN) + 20 \times REF_A - 19 \times REF_B \quad (2)$$

COMMON-MODE RANGE

The high common-mode range of the INA149 is achieved by dividing down the input signal with a high precision resistor divider. This resistor divider brings both the positive input and the negative input within the input range of the internal operational amplifier. This input range depends on the supply voltage of the INA149.

Both Figure 2 and Figure 3 can be used to determine the maximum common-mode range for a specific supply voltage. The maximum common-mode range can also be calculated by ensuring that both the positive and the negative input of the internal amplifier are within 1.5 V of the supply voltage.

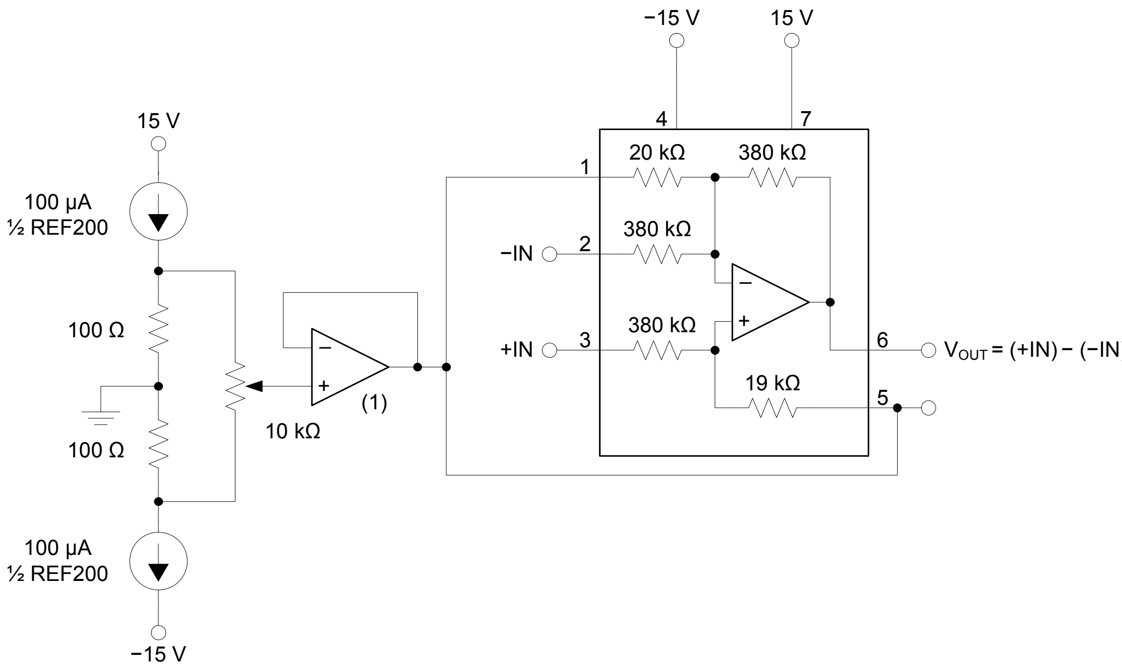
In case the voltage at the inputs of the internal amplifier exceeds the supply voltage, the internal ESD diodes start conducting current. This current must be limited to 10 mA to make sure not to exceed the absolute maximum ratings for the device.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA149 depends on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedance driving the two inputs. A 75-Ω resistance in series with pins 2 or 3 decreases the common-mode rejection ratio (CMRR) from 100 dB (typical) to 74 dB.

Resistance in series with the reference pins also degrades CMR. A 4-Ω resistance in series with pins 1 or 5 decreases CMRR from 100 dB to 74 dB.

Most applications do not require trimming. Figure 45 shows an optional circuit that may be used for trimming offset voltage and common-mode rejection.



(1) The OPA171 (a 36-V, low-power, RRO, general-purpose operational amplifier) can be used for this application.

Figure 45. Offset Voltage Trim Circuit

MEASURING CURRENT

The INA149 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 46 shows the INA149 used to measure the supply currents of a device under test.

The sense resistor imbalances the input resistor matching of the INA149, thus degrading its CMR. Also, the input impedance of the INA149 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor (R_C), equal to the value of R_S, as shown in Figure 46. If R_S is less than 5 Ω, degradation in the CMR is negligible and R_C can be omitted. If R_S is larger than approximately 1 kΩ, trimming R_C may be required to achive greater than 90-dB CMR. This error is caused by the INA149 input impedance mismatch.

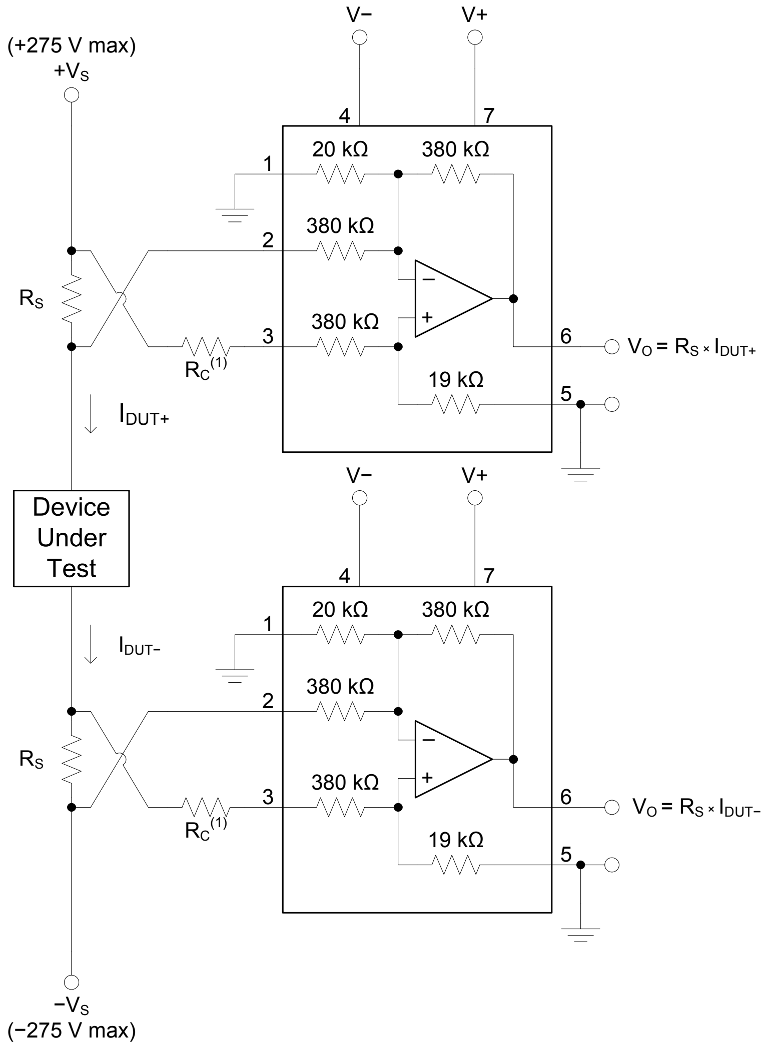


Figure 46. Measuring Supply Currents of a Device Under Test

If R_S is more than approximately 50 Ω, the gain error is greater than the 0.02% specification of the INA149. This gain error can be corrected by slightly increasing the value of R_S. The corrected value (R_S') can be calculated by

$$R_S' = R_S \times 380\ k\Omega/(380\ k\Omega - R_S) \quad (3)$$

Example: For a 1-V/mA transfer function, the nominal, uncorrected value for R_S would be 1 kΩ. A slightly larger value (R_S' = 1002.6 Ω), compensates for the gain error as a result of loading.

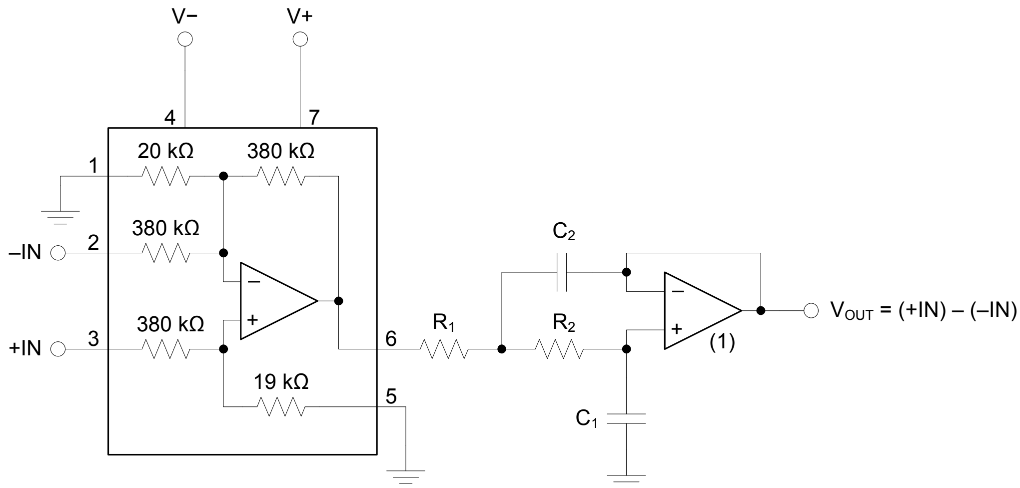
The 380-kΩ term in the equation for R_S' has a tolerance of 25%, thus sense resistors above approximately 400 Ω may require trimming to achive gain accuracy better than 0.02%.

NOISE PERFORMANCE

The wideband noise performane of the INA149 is dominated by the internal resistor network. The thermal or *Johnson noise* of these resistors measures approximately 550 nV/√Hz. The internal op amp contributes virtually no excess noise at frequencies above 100 Hz.

Many applications may be satisfied with less than the full 500-kHz bandwidth of the INA149. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 47 limits bandwidth and reduces noise. Because the INA149 has a 1/f noise corner frequency of approximately 100 Hz, a cutoff frequency below 100 Hz does not further reduce noise.

Component values for different filter frequencies are shown in Table 1.



(1) For most applications, the OPA171 can be used as an operational amplifier. For directly driving successive-approximation register (SAR) data converters, the OPA140 is a good choice.

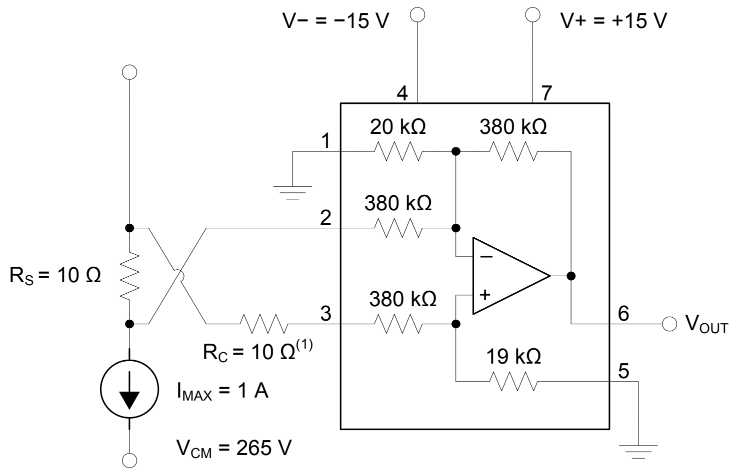
Figure 47. Output Filter for Noise Reduction

Table 1. Components Values for Different Filter Bandwidths

BUTTERWORTH LOW-PASS ($f_{-3\ dB}$)	OUTPUT NOISE (mV_{PP})	R_1	R_2	C_1	C_2
200 kHz	1.8	No filter			
100 kHz	1.1	11 kΩ	11.3 kΩ	100 pF	200 pF
10 kHz	0.35	11 kΩ	11.3 kΩ	1 nF	2 nF
1 kHz	0.11	11 kΩ	11.3 kΩ	10 nF	20 nF
100 Hz	0.05	11 kΩ	11.3 kΩ	0.1 µF	0.2 µF

ERROR BUDGET ANALYSIS

The following error budget analysis demonstrates the importance of a high common-mode rejection ratio when measuring small differential signals in the presence of high common-mode voltages. Figure 48 shows a typical current measurement application.



(1) See the *Measuring Current* section for details about R_C.

Figure 48. Typical Current Measurement Application

The maximum current through the shunt resistor (R_S) is 1 A and generates a full-scale voltage drop of 10 V. All error sources in this calculation are shown in relation to this full-scale voltage. The common-mode voltage in this scenario is 265 V and the temperature range is from room temperature (+25°C) to +85°C. Table 2 shows the dominant error sources for the INA149 and a competitor device.

Table 2. Error Budget Analysis

ERROR SOURCE	INA149	COMPETIOR A	ERROR (ppm of FS)	
			INA149	COMPETITOR A
Accuracy, T_A = +25°C				
Initial gain error	0.02% FS	0.05% FS	200	500
Offset voltage	1100 μV	1000 μV	110	100
Common mode	265 V/90 dB = 8380 μV	265 V/77 dB = 37432 μV	838	3743
		Total acuracy error	1148	4343
Temperature drift				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset voltage	10 μV/°C × 60°C	20 μV/°C × 60°C	60	120
		Total drift error	660	720
		Total error	**1808**	**5063**

If a smaller shunt resistor is used, the full-scale voltage drop is also smaller. A shunt resistor of 1 Ω causes a 1-V voltage drop with a current of 1 A flowing through it. The error of 1808 ppm for a full-scale voltage of 10 V becomes 18080 ppm (1.6%) for a full-scale voltage of only 1 V.

This example demonstrates that the dominate source of error, even over temperature, comes from the CMRR specification of the devices. The common-mode error is 46% of the total error for the INA149 and 74% of the total error for the competitor device.

BATTERY CELL VOLTAGE MONITOR

The INA149 can be used to measure the voltages of single cells in a stacked battery pack. Figure 49 shows an examples for such an application.

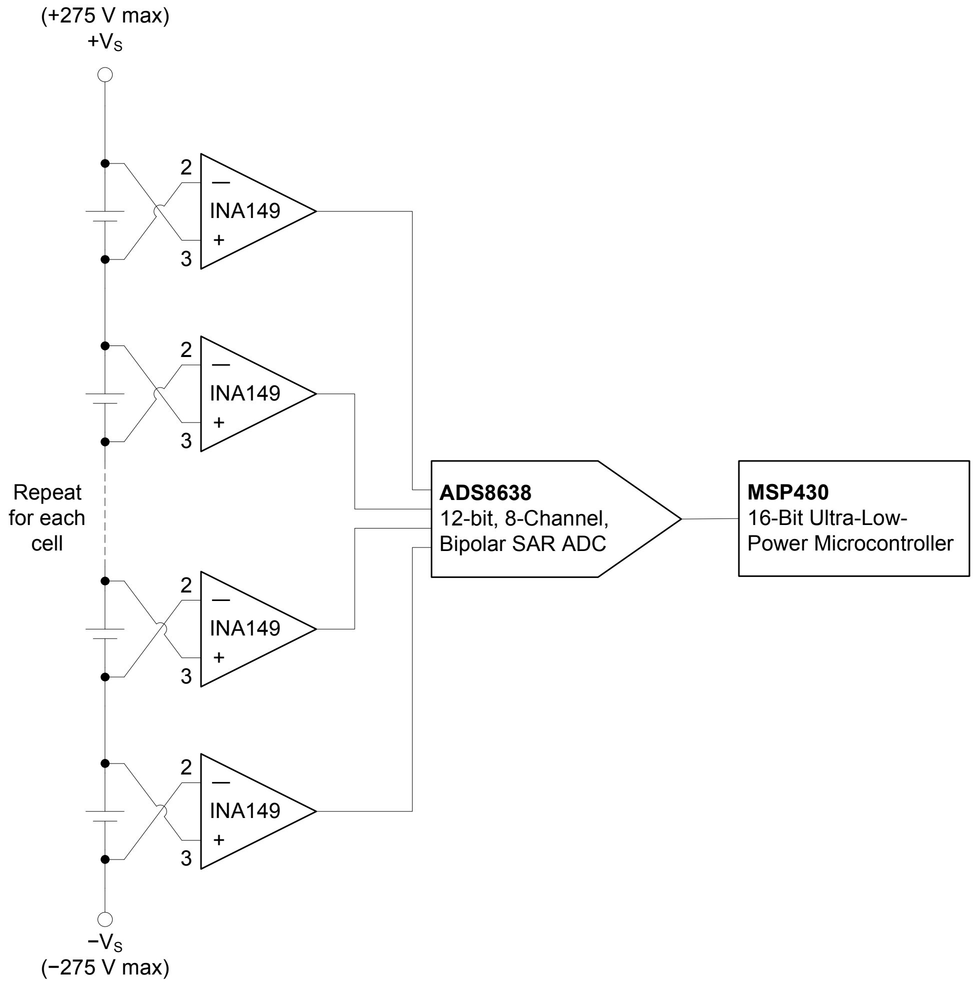


Figure 49. Battery Cell Voltage Monitor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
INA149AID	ACTIVE	SOIC	D	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
INA149AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

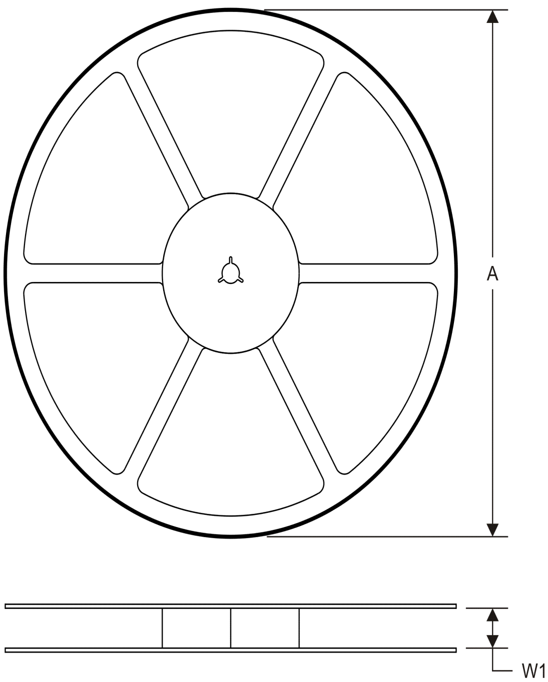
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

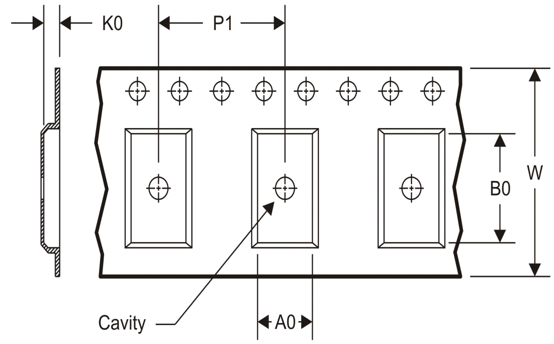
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

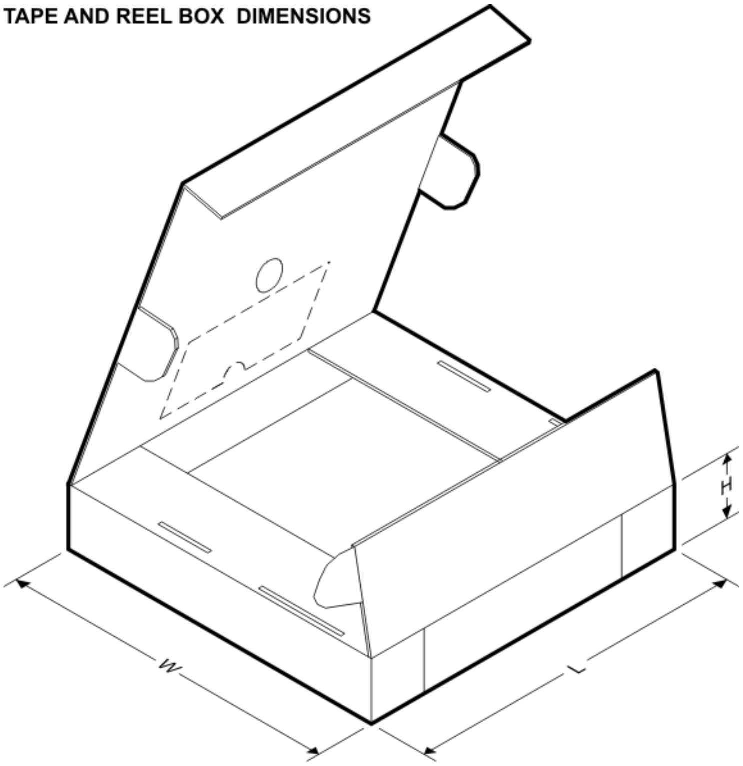


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

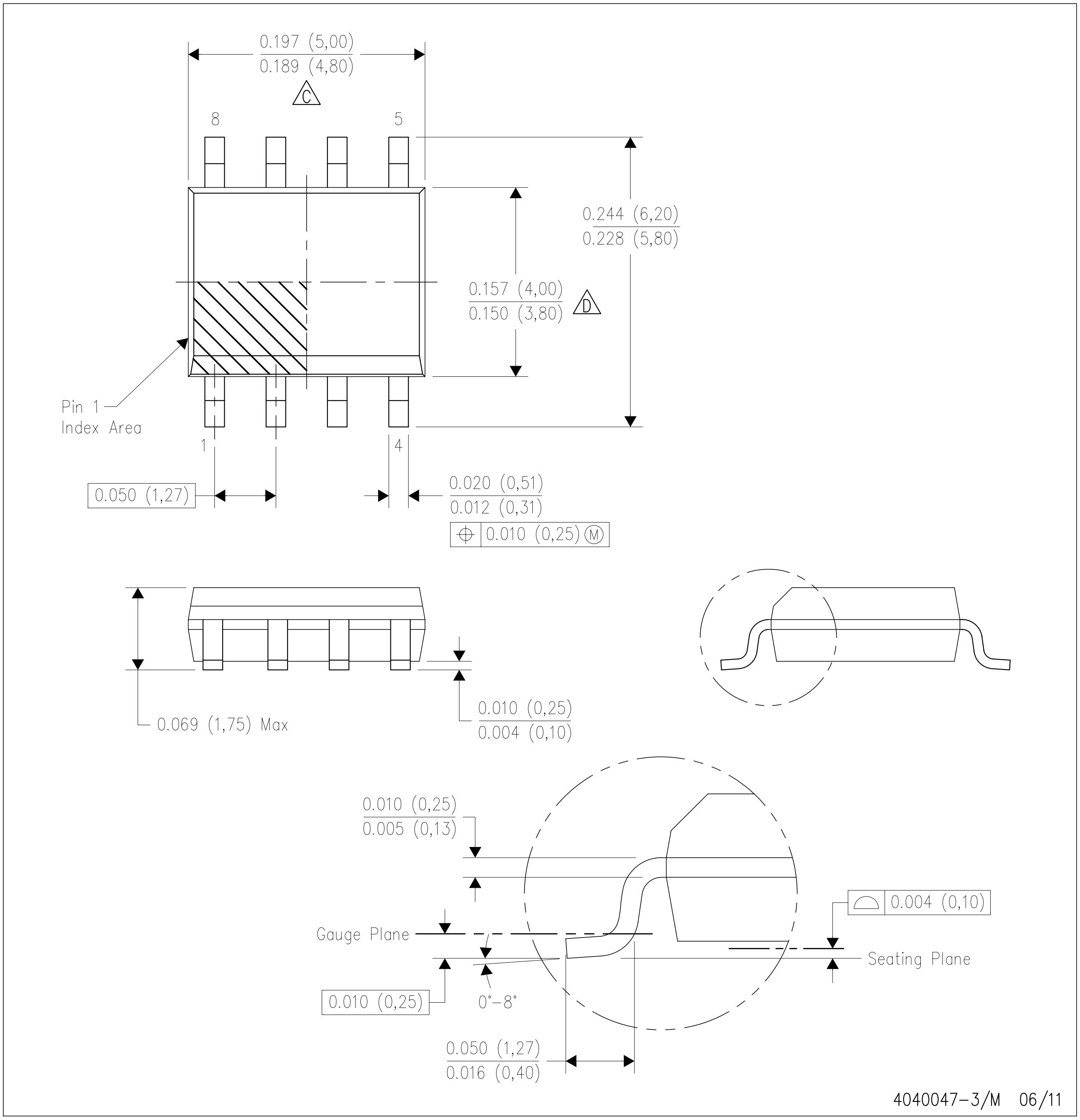
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA149AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



*All dimensions are nominal

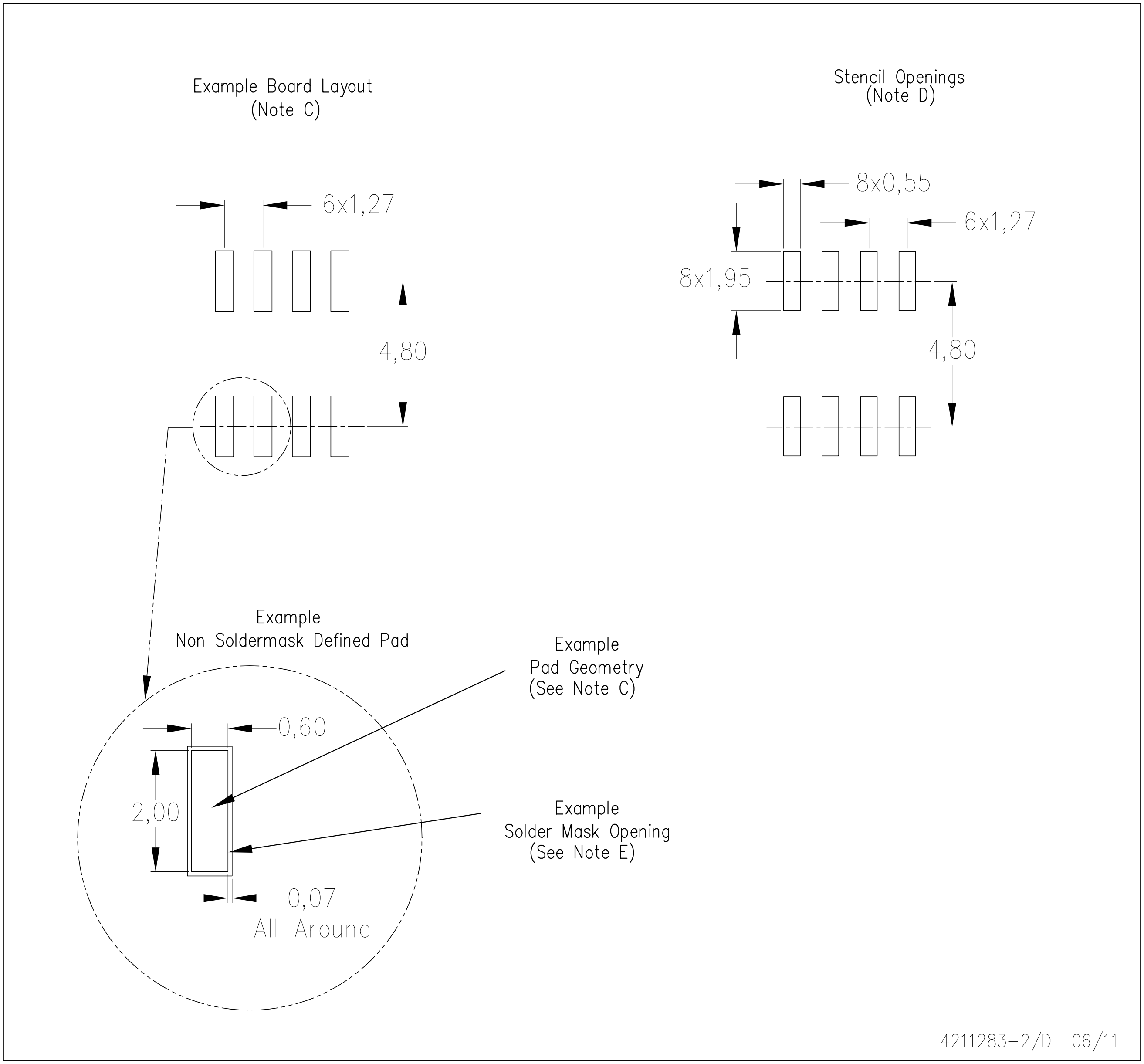
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA149AIDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.