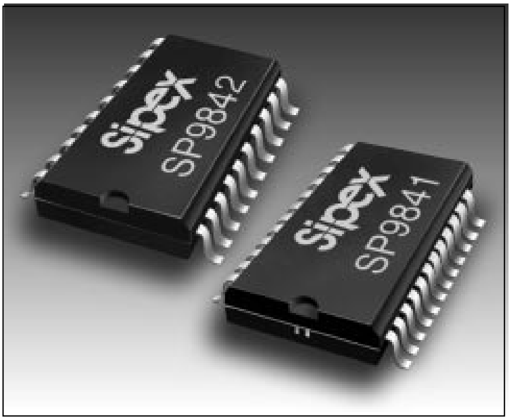
8-Bit Octal, 2-Quadrant Multiplying, BiCMOS DAC

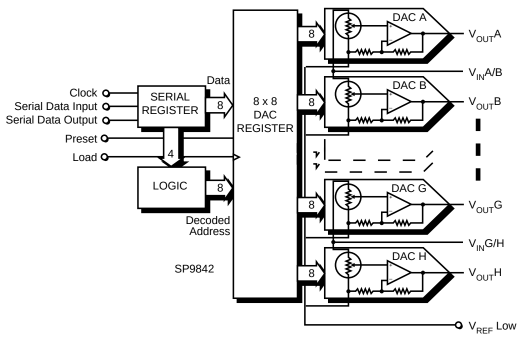
- Replaces 8 Potentiometers and 8 Op Amps
- Operates from Single +5V Supply
- 6.3 MHz 2-Quadrant Multiplying Gain Bandwidth
- No Signal Inversion
- Eight Reference Inputs, Eight Voltage Outputs (SP9841)
- Four Reference Inputs, Eight Voltage Outputs (SP9842)
- 3-Wire Serial Input
- 0.8MHz Data Update Rate
- +3.25 Volt Output Swing
- Midscale Preset
- Low 65 mW Power Dissipation (8mW/DAC)

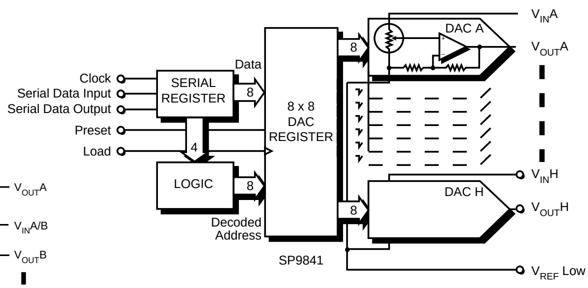


DESCRIPTION…

The **SP9841** and **SP9842** are general purpose octal DACs in a single package. The **SP9841** features eight individual reference inputs, while the **SP9842** provides four pair of voltage reference inputs. Both parts feature 6.3MHz bandwidth, two–quadrant multiplication, and a three–wire serial interface. Other features include midscale preset, no signal inversion and low power dissipation from a single +5V supply. Devices are available in commercial and industrial temperature ranges.

SP9842 Block Diagram



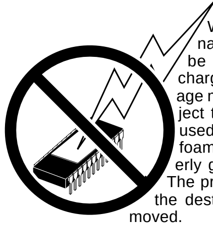


SP9841 Block Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} to GND .... -0.3V, +7V
$V_{IN}X$ to GND .... V_{DD}
$V_{REF}L$ to GND .... V_{DD}
$V_{OUT}X$ to GND .... V_{DD}
Short Circuit $I_{OUT}X$ to GND .... Continuous
Digital Input & Output Voltage to GND .... V_{DD}
Operating Temperature Range
Commercial: SP9841K/SP9842K .... 0°C to +70°C
Extended Industrial: SP9841B/SP9842B .... -40°C to +85°C
Maximum Junction Temperature (T_J max) .... +150°C
Storage Temperature .... -65° to 150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Power Dissipation .... (T_J max - T_A)/∅JA
Thermal Resistance $\varnothing_{JA}$
P-DIP .... 57°C/W
SOIC-24 .... 70°C/W



CAUTION:
While all input and output pins have internal protection networks, these parts should be considered ESD (ElectroStatic Discharge) sensitive devices. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(V_{DD} = +5V, All $V_{IN}X$= +1.625V, $V_{REF}L$ = 0V, T_A = 25° C for commercial–grade parts; $T_{MIN} \leq T_A = T_{MAX}$ for industrial–grade parts; specifications apply to all DAC's unless noted otherwise.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SIGNAL INPUTS					
Input Voltage Range	0		1.625	V	V_{REFL} = GND, V_{DD} = 4.75V
Input Resistance					D = 55_H; Code Dependent
SP9841	5	10		kΩ	
SP9842	2.5	5		kΩ	
Input Capacitance					Code Dependent
SP9841		19	30	pF	
SP9842		38	60	pF	
V_{REFL} Resistance	0.375	0.75		kΩ	All D = AB_H; Code Dependent
V_{REFL} Capacitance		190	250	pF	Code Dependent
DIGITAL INPUTS					
Logic High	2.4			V	
Logic Low			0.8	V	
Input Current			±10	µA	
Input Capacitance			8	pF	
Input Coding		Binary			
STATIC ACCURACY					
Resolution		8		Bits	
Integral Nonlinearity		±0.25	±1.0	LSB	Note 1
Differential Nonlinearity		±0.2	±1.0	LSB	Note 1
Half-Scale Output Voltage	1.600	1.625	1.650	V	$\overline{PR}$ = LOW, Sets D = 80_H
Zero-Scale Output Voltage		20	100	mV	D = 00_H
Output Voltage Drift		25		µV/°C	$\overline{PR}$ = LOW, Sets D = 80_H
DYNAMIC PERFORMANCE					
Multiplying Gain Bandwidth	4	6.3		MHz	$V_{IN}X$ = 100 mV p-p+ 1.0V dc
Slew Rate					Measured 10% to 90%
Positive	3.0	7.9		V/µs	$V_{OUT}X$ = 100mV to +3.1V
Negative	–3.0	–8.3		V/µs	$V_{OUT}X$ = +3.1V to 100mV
Total Harmonic Distortion		0.005		%	$V_{IN}X$ = 0.8V_{DC} + 1.4V p-p D= FF_H; 1kHz, f_{LP} = 80 kHz
Output Settling Time		0.7		µs	±1 LSB Error Band, 8_H to 255_H
Crosstalk	60	70		dB	Note 2
Digital Feedthrough		6		nVs	$V_{REF}L$ = +1.625V, D = 0 to FF_H
Wideband Noise		42.5		µV rms	V_{OUT} = 3.25V; 400Hz to 80kHz

SPECIFICATIONS *(continued)*

(V_{DD} = +5V, All V_{IN}X= +1.625V, V_{REF}L = 0V, T_A = 25° C for commercial–grade parts; $T_{MIN} \le T_A = T_{MAX}$ for industrial–grade parts; specifications apply to all DAC's unless noted otherwise.)

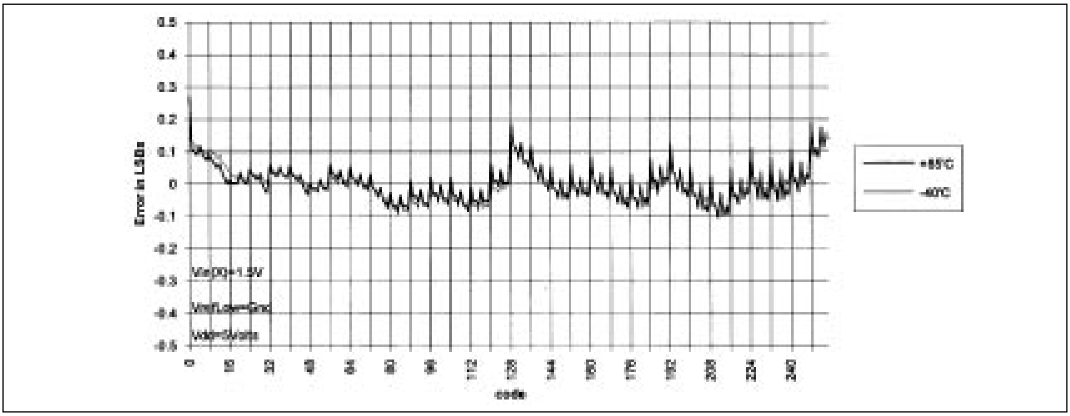
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DYNAMIC PERFORMANCE					
SINAD		85		dB	V_{IN}X = 0.8V_{DC} + 1.4V p-p D= FF_H; 1kHz, f_{LP} = 80 kHz
Digital Crosstalk		6		nVs	SP9842 only; measured between adjacent channels of same pair; D = $7F_H$ to 80_H
DAC OUTPUTS					
Voltage Range	0		V_{DD}–1.5	V	R_L = 5kΩ; V_{DD} = 4.75V
Output Current	±10	±15		mA	ΔV_{OUT} < 10mV, V_{IN}X=1.625V, $\overline{PR}$ = LOW
Capacitive Load		47,000		pF	No Oscillation
DIGITAL OUTPUT					
Logic High	3.5			V	I_{OH} = -0.4mA
Logic Low			0.4	V	I_{OL} = 1.6mA
POWER REQUIREMENTS					
Power Supply Range	4.75	5.00	5.25	V	To rated specifications
Positive Supply Current		13		mA	$\overline{PR}$ = LOW
Power Dissipation		65		mW	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range					
Commercial	0		+70	°C	
Industrial	–40		+85	°C	
Storage Temperature Range	–65		+150	°C	
Package					
SP9841N	24–pin Plastic DIP				
SP9841S	24–pin SOIC				
SP9842S	20–pin SOIC				Note 3

Notes:

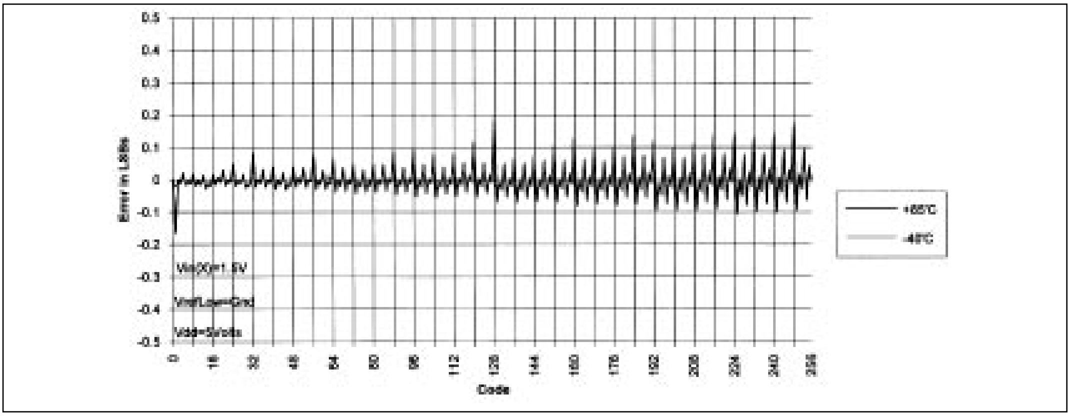
1 The op amp limits the linearity for $V_{OUT} \le$ 100mV. When V_{REFL} is driven above ground such that the output voltage remains above 100mV, then the linearity specifications apply to all codes. For V_{REFL} = GND, V_{IN} = 1.5V, codes 0 through 7 are not included in differential or integral linearity tests. Integral and differential linearity are computed with respect to the best fit straight line through codes 8 through 255.

2 **SP9841** is measured between adjacent channels, f = 100kHz; **SP9842** is measured between adjacent pairs, f = 100kHz.

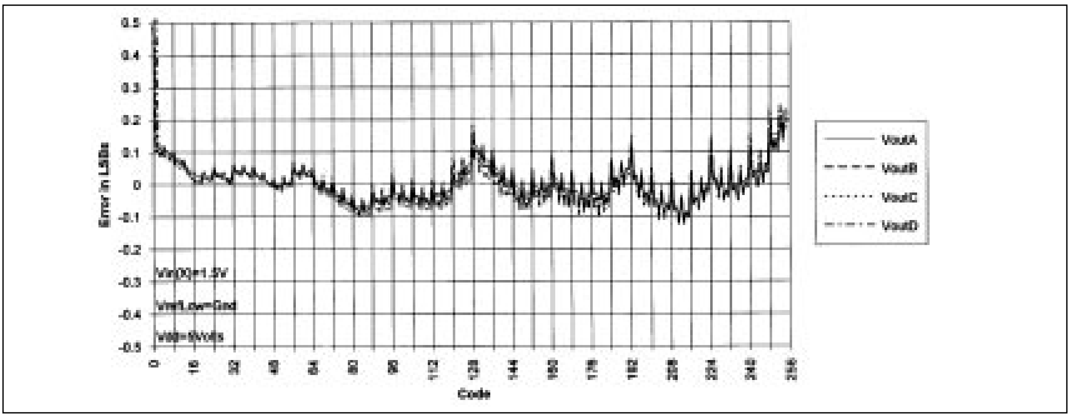
3 For plastic DIP packaging of **SP9842**, please consult factory.



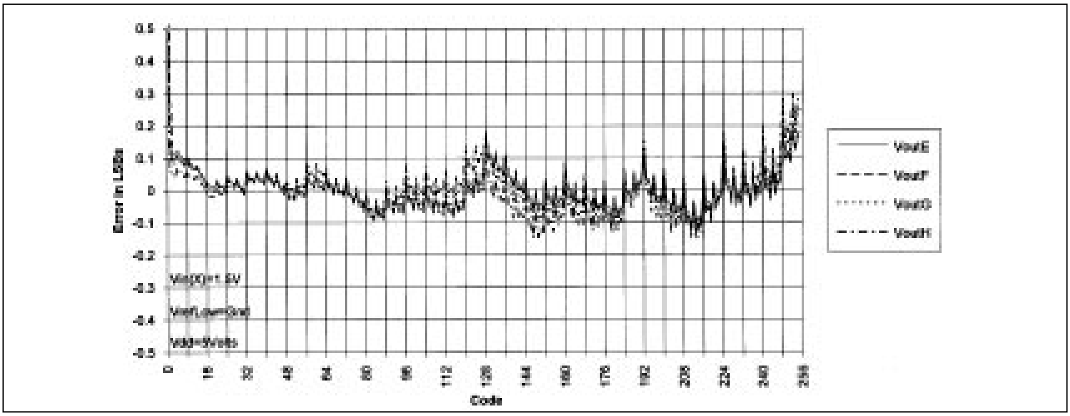
Plot 1. Integral Linearity Error versus Code.



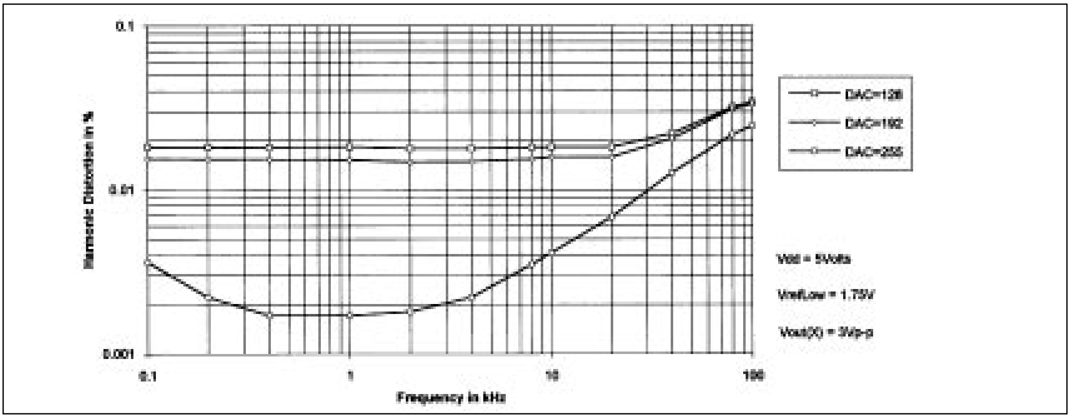
Plot 2. Differential Non–linearity Error versus Code.



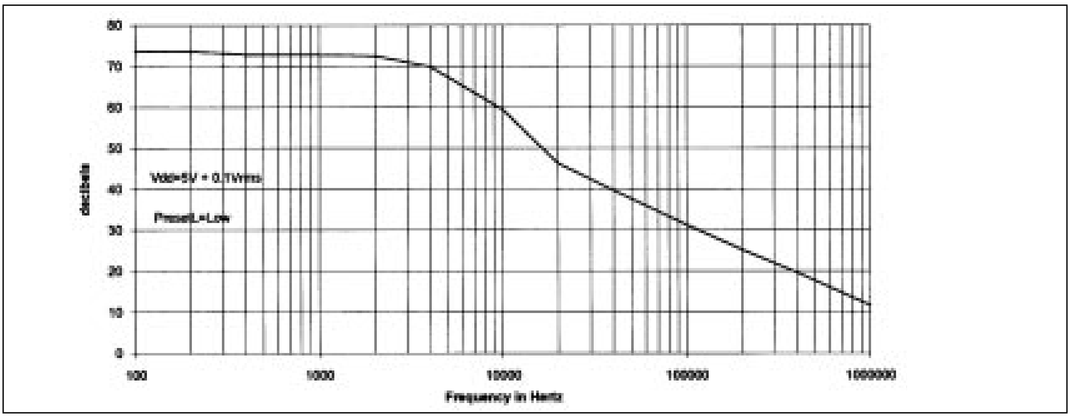
Plot 3. Integral Linearity Matching; V_{OUT} A through V_{OUT} D.



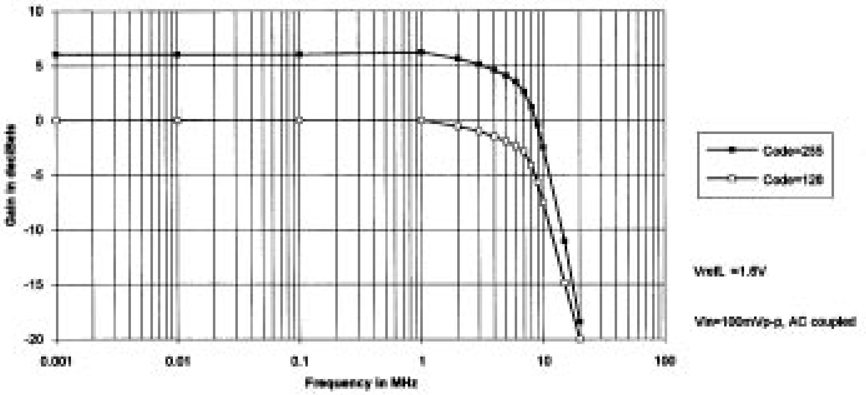
Plot 4. Integral Linearity Matching; V_{OUT} E through V_{OUT} H.



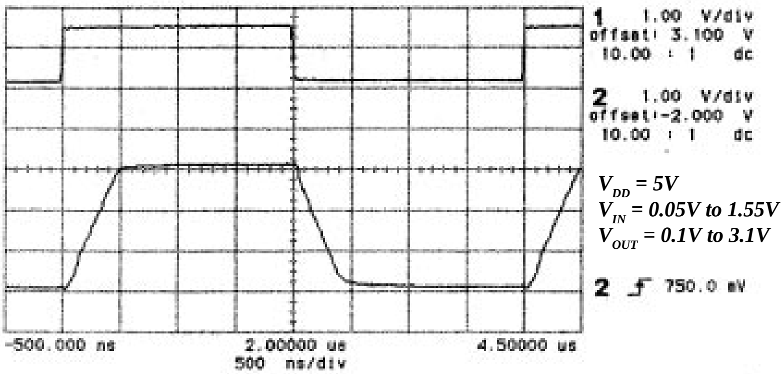
Plot 5. THD versus Frequency.



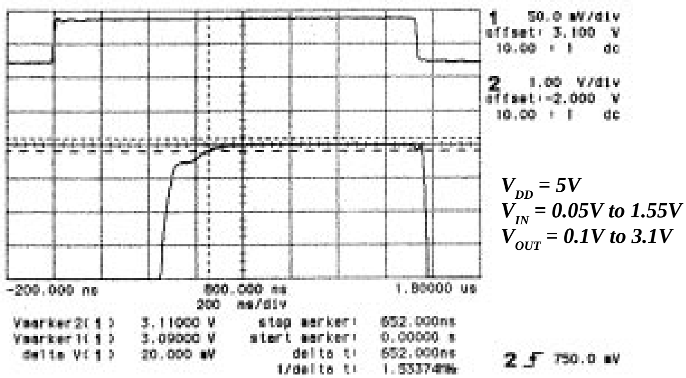
Plot 6. PSRR versus Frequency.



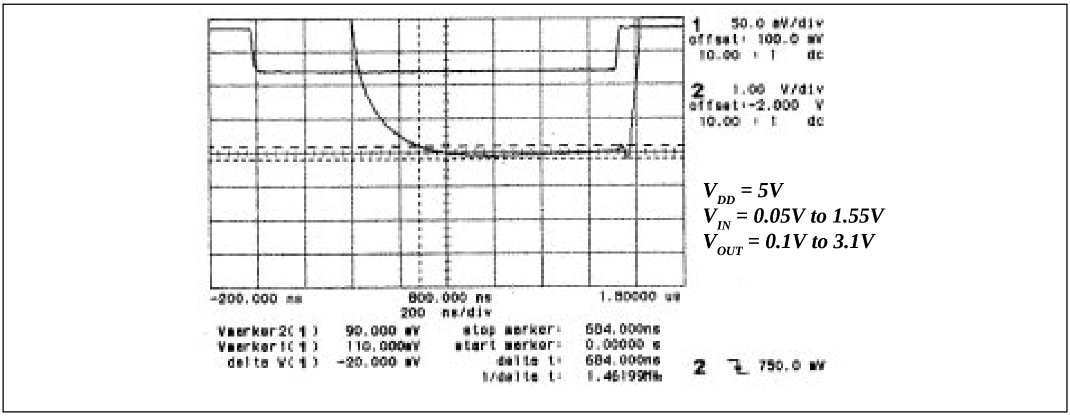
Plot 7. Small Signal Gain versus Frequency.



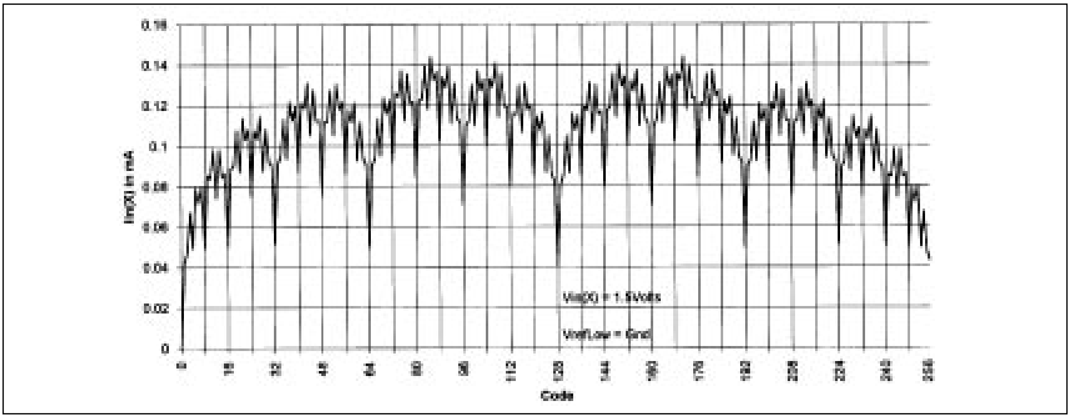
Plot 8. Full Scale Pulse Response.



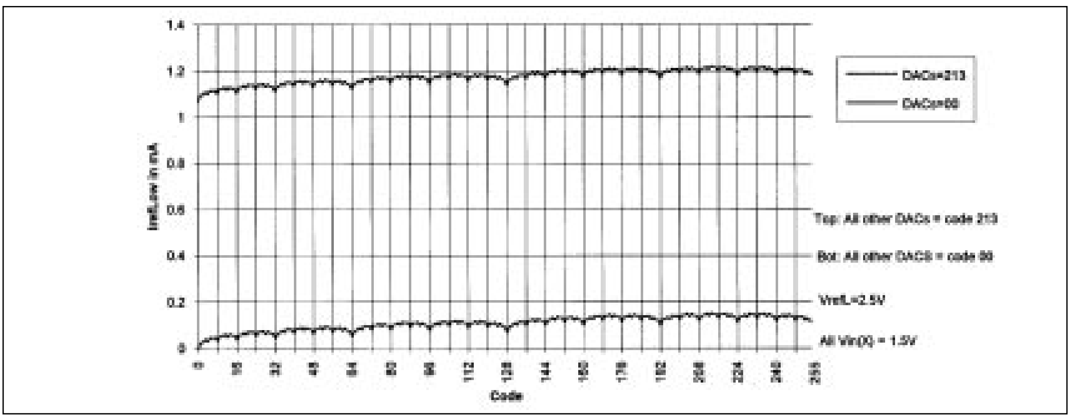
Plot 9. Positive Full Scale Settling.



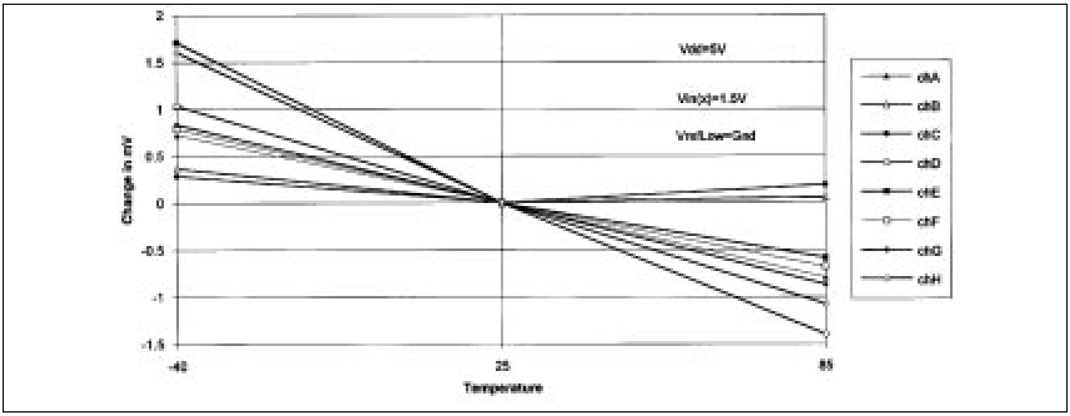
Plot 10. Negative Full Scale Settling.



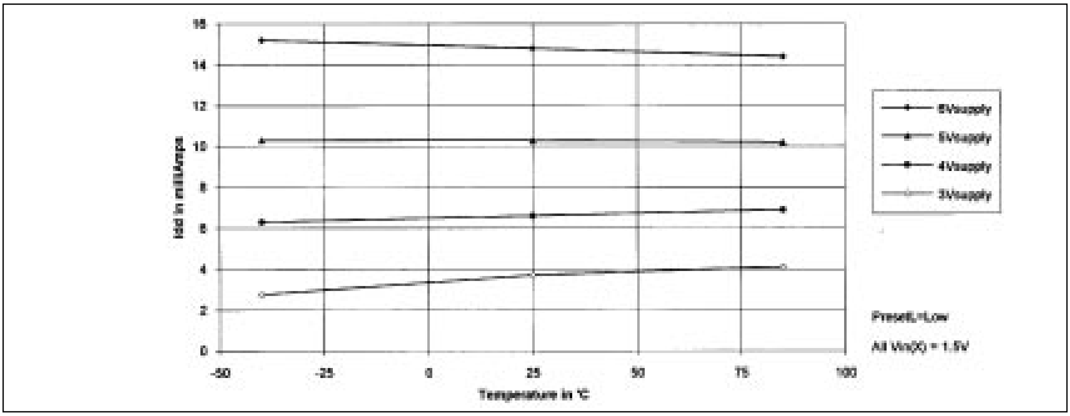
Plot 11. V_{IN}(X) Current versus Code.



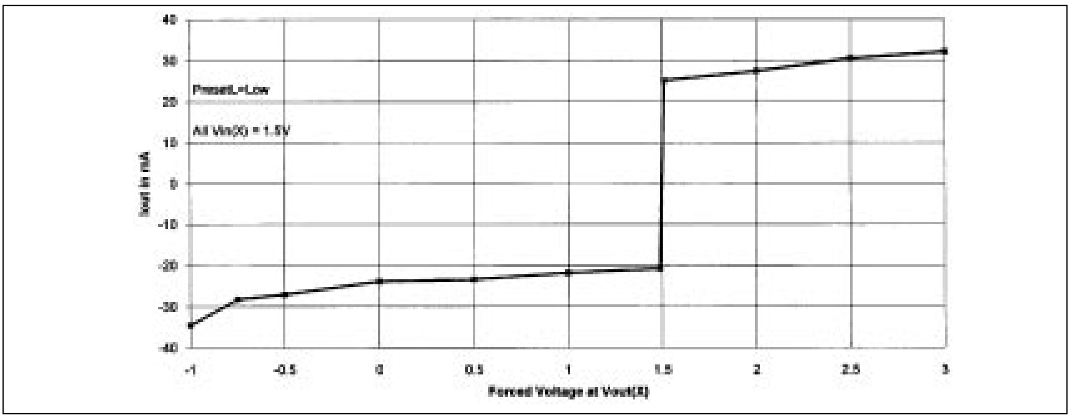
Plot 12. I_{REFL} Current Input Current versus Code.



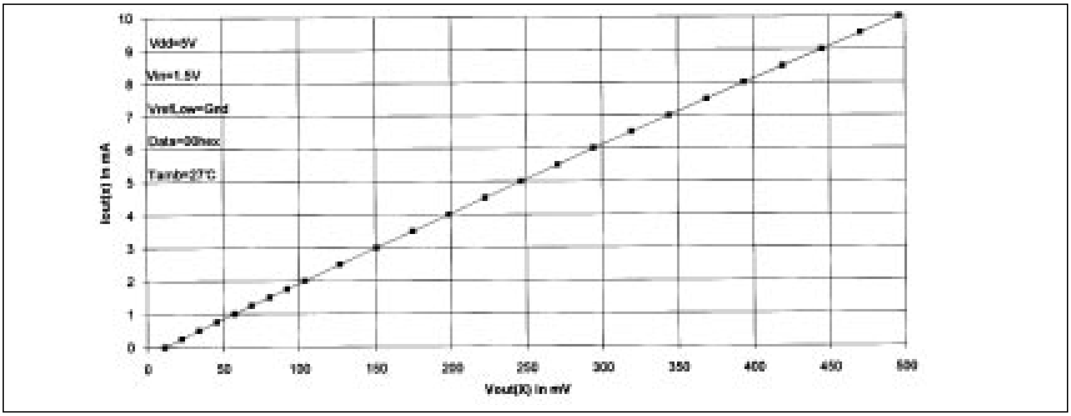
Plot 13. Typical Midscale Output versus Temperature.



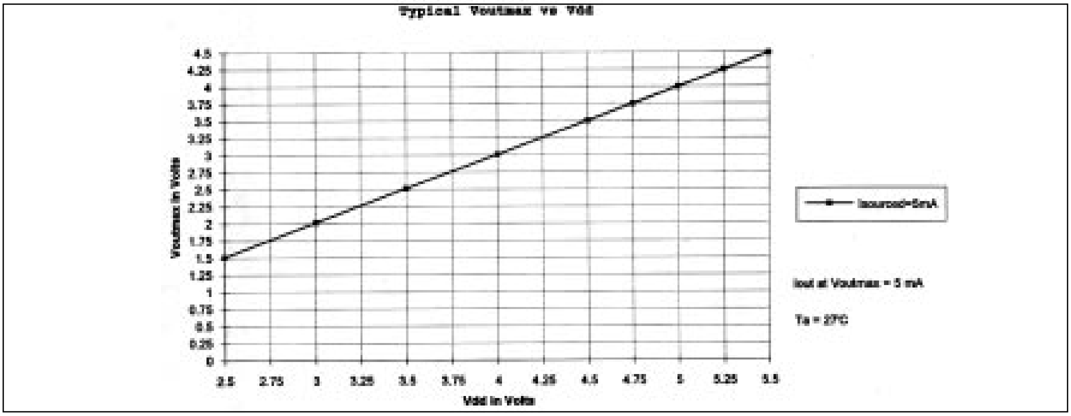
Plot 14. Supply Current versus Temperature.



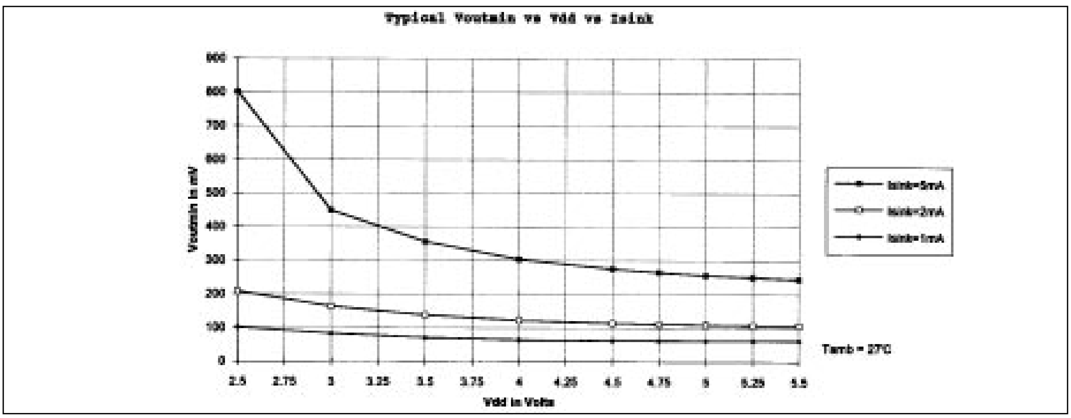
Plot 15. Output Short Circuit Current versus $V_{OUT}(X)$.



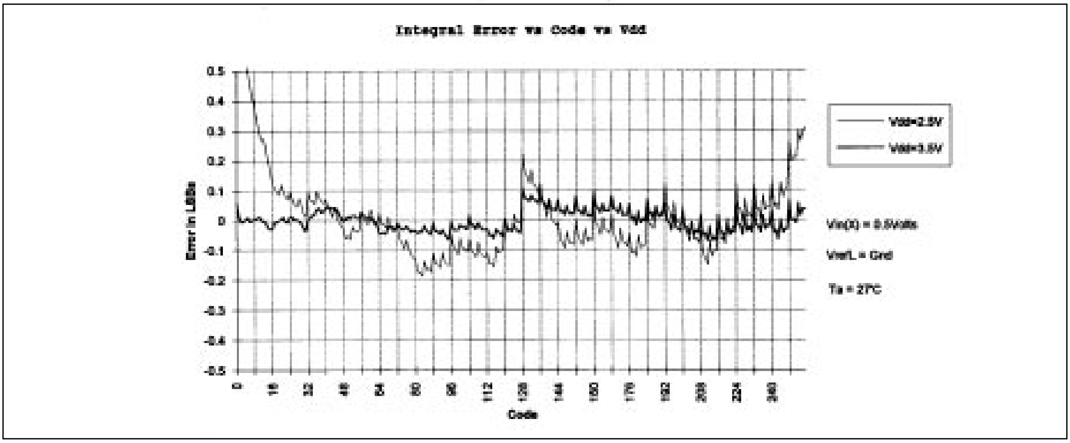
Plot 16. Sink Current at Zero Scale.



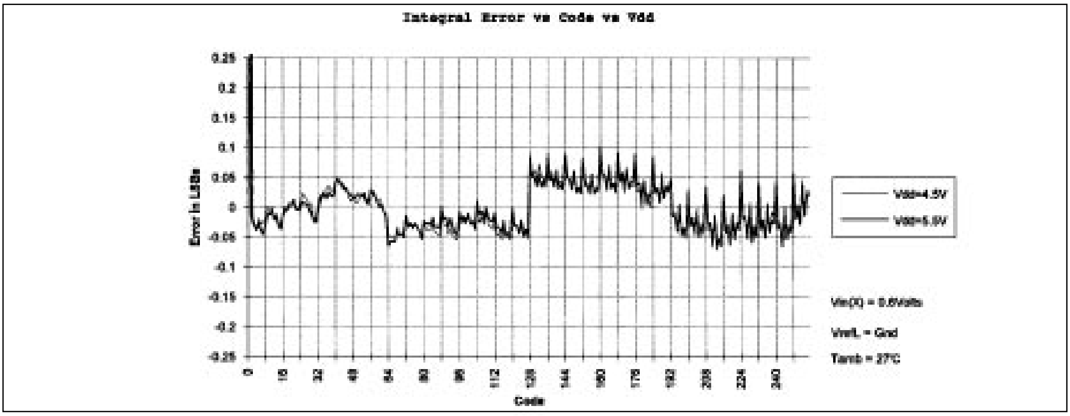
Plot 17. Typical V_{OUT}max versus V_{DD}.



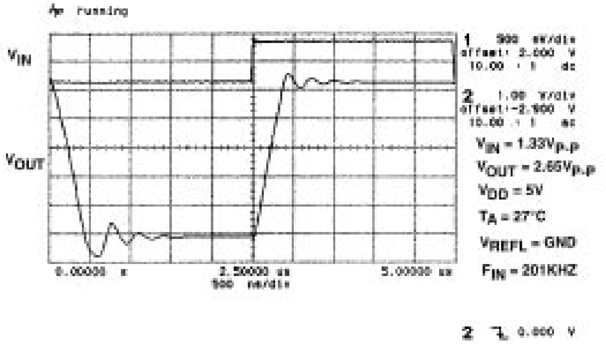
Plot 18. Typical V_{OUT} min versus V_{DD} versus I_{SINK}.



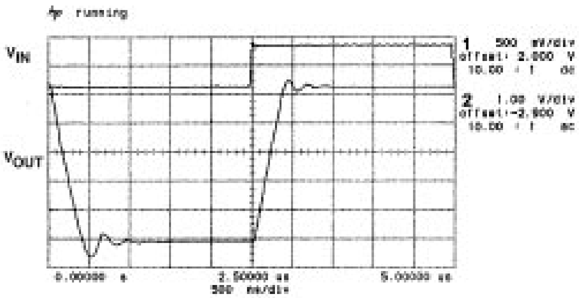
Plot 19. Integral Error versus Code versus V_{DD}; $V_{IN}(X)$ = 0.5V.



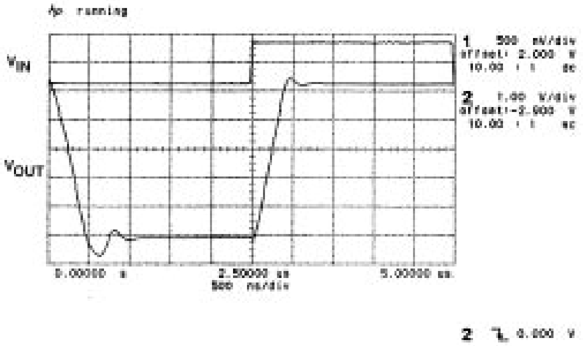
Plot 20. Integral Error versus Code versus V_{DD}; $V_{IN}(X)$ = 0.6V.



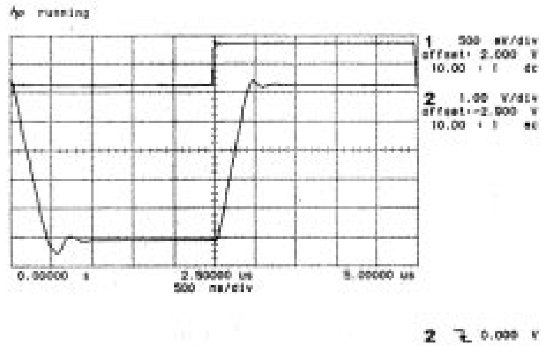
a)



b)

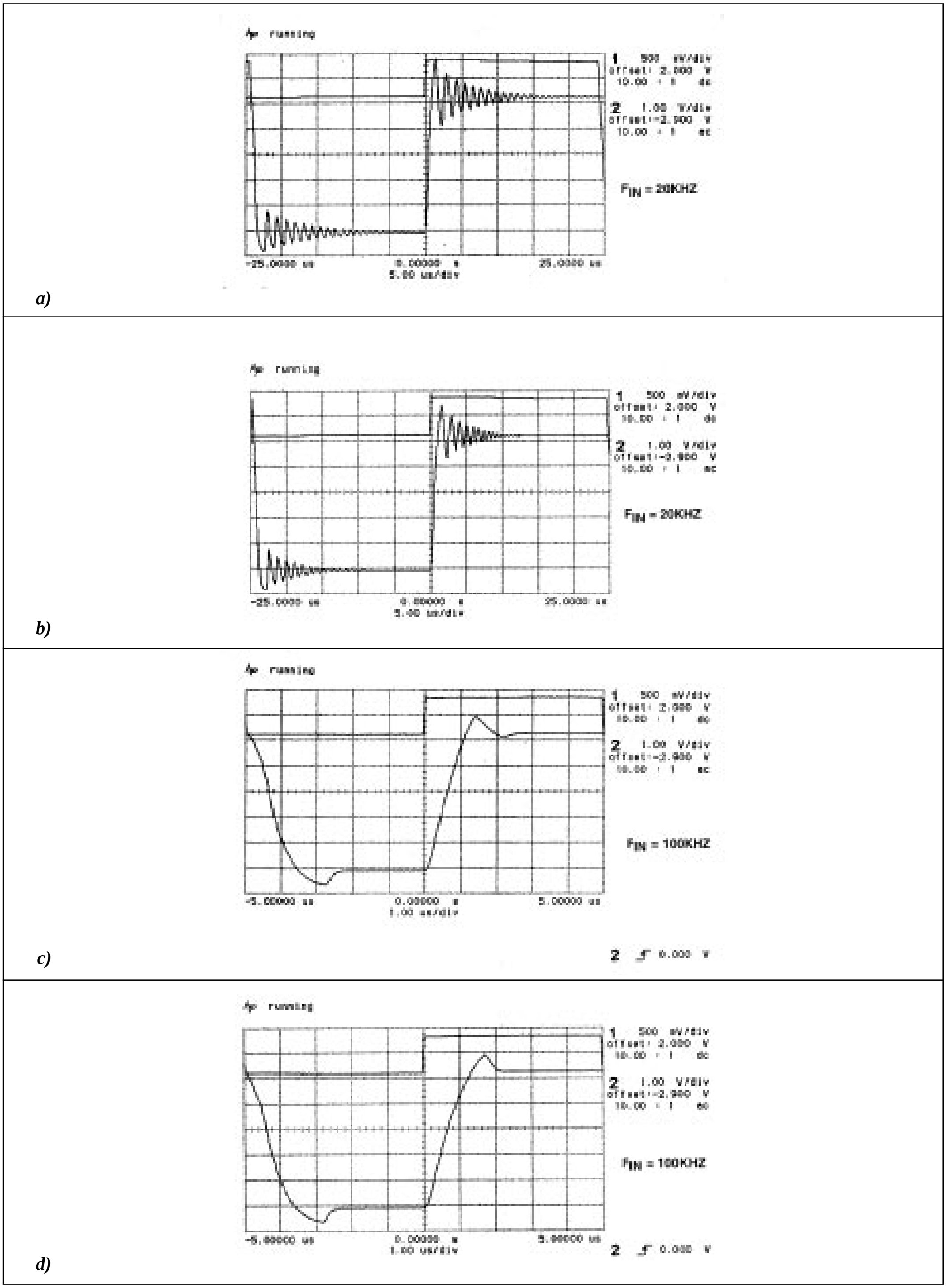


c)

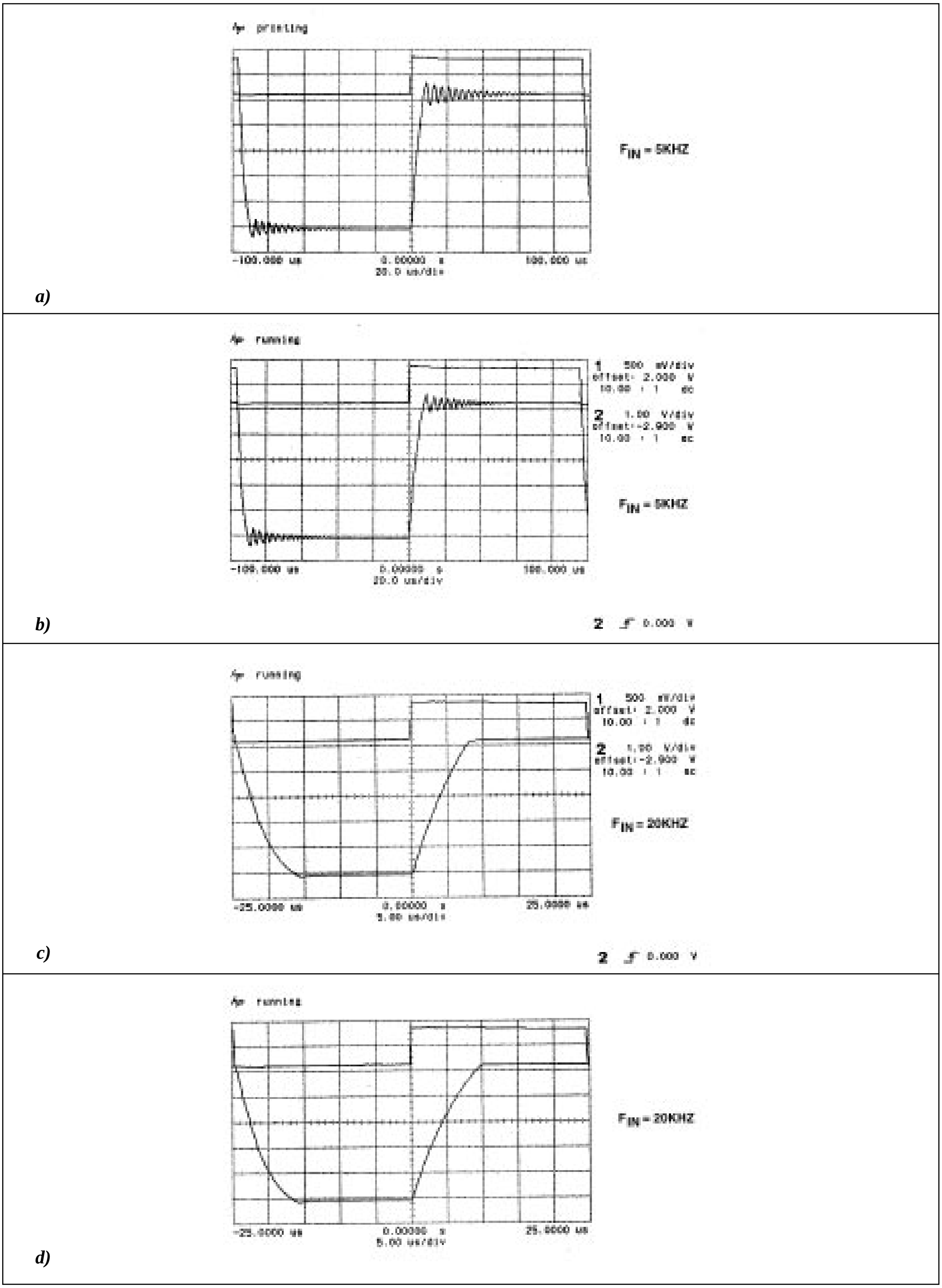


d)

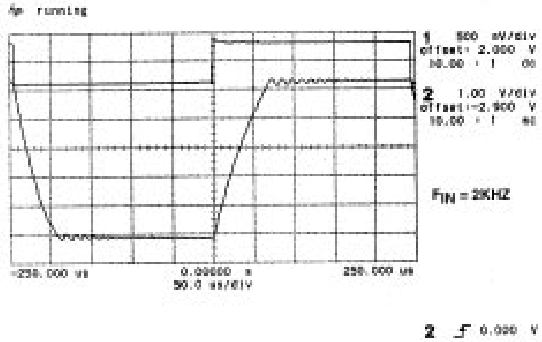
Plot 21. Pulse Response — a) C_{LOAD} = 470pF, R_{LOAD} = 10MOhm; b) C_{LOAD} = 470pF, R_{LOAD} = 1kOhm; c) 50Ohms in series with C_{LOAD} = 470pF; d) R_{LOAD} = 1kOhm, 50Ohms in series with C_{LOAD} = 470pF.



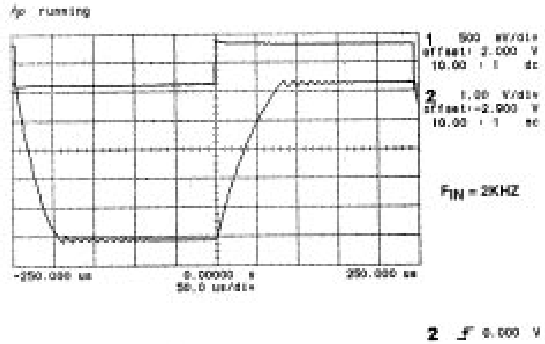
Plot 22. Pulse Response — a) C_{LOAD} = 4,700pF; b) C_{LOAD} = 4,700pF, R_{LOAD} = 1kOhm; c) 30 Ohms in series with C_{LOAD} = 4,700pF; d) R_{LOAD} = 1kOhm, 30Ohms in series with C_{LOAD} = 4,700pF.



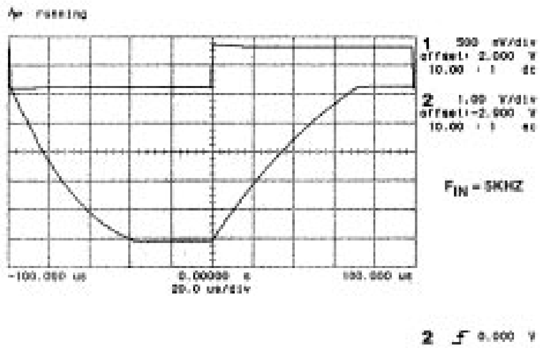
Plot 23. Pulse Response — a) C_{LOAD} = 47,000pF; b) C_{LOAD} = 47,000pF, R_{LOAD} = 1kOhm; c) 15 Ohms in series with C_{LOAD} = 47,000pF; d) R_{LOAD} = 1kOhm, 15 Ohms in series with C_{LOAD} = 47,000pF.



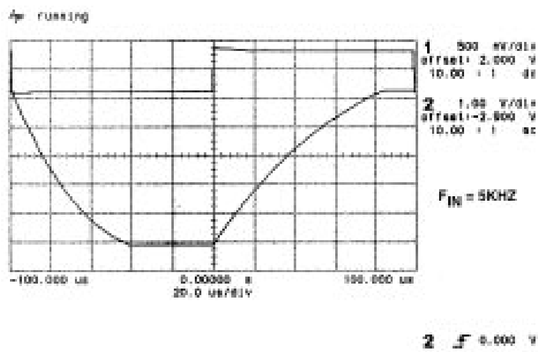
a)



b)



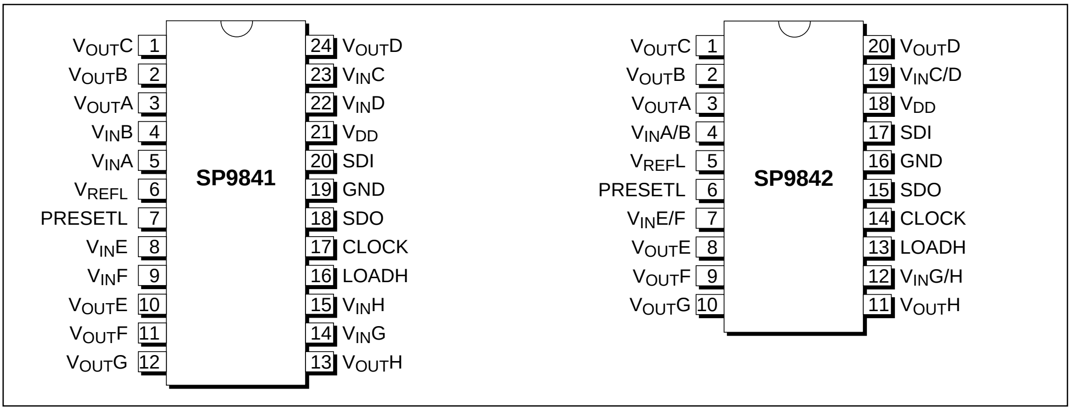
c)



d)

Plot 24. Pulse Response — a) C_{LOAD} = 0.47µF; b) C_{LOAD} = 0.47µF, R_{LOAD} = 1kOhm; c) 8.2 Ohms in series with C_{LOAD} = 0.47µF; d) R_{LOAD} = 1kOhm, 8.2 Ohms in series with C_{LOAD} = 0.47µF.

PINOUT



SP9841 PINOUT

Pin 1 — V_{OUT}C — DAC C Voltage Output.

Pin 2 — V_{OUT}B — DAC B Voltage Output.

Pin 3 — V_{OUT}A — DAC A Voltage Output.

Pin 4 — V_{IN}B — DAC B Reference Voltage Input.

Pin 5 — V_{IN}A — DAC A Reference Voltage Input.

Pin 6 — V_{REF}L — DAC Reference Voltage Input Low, common to all DACs.

Pin 7 — PRESETL — Preset Input; active low; all DAC registers forced to 80_H.

Pin 8 — V_{IN}E — DAC E Reference Voltage Input.

Pin 9 — V_{IN}F — DAC F Reference Voltage Input.

Pin 10 — V_{OUT}E — DAC E Voltage Output.

Pin 11 — V_{OUT}F — DAC F Voltage Output.

Pin 12 — V_{OUT}G — DAC G Voltage Output.

Pin 13 — V_{OUT}H — DAC H Voltage Output.

Pin 14 — V_{IN}G — DAC G Reference Voltage Input.

Pin 15 — V_{IN}H — DAC H Reference Voltage Input.

Pin 16 — LOADH — Load DAC Register Strobe; active high input that transfers the data bits from the Serial Input Register into the decoded DAC Register. Refer to Table 1.

Pin 17 — CLOCK — Serial Clock Input; positive–edge triggered.

Pin 18 — SDO — Serial Data Output; active totem–pole output.

Pin 19 — GND — Ground.

Pin 20 — SDI — Serial Data Input.

Pin 21 — V_{DD} — Positive 5V Power Supply.

Pin 22 — V_{IN}D — DAC D Reference Voltage Input.

Pin 23 — V_{IN}C — DAC C Reference Voltage Input.

Pin 24 — V_{OUT}D — DAC D Voltage Output.

SP9842 PINOUT

Pin 1 — V_{OUT}C — DAC C Voltage Output.

Pin 2 — V_{OUT}B — DAC B Voltage Output.

Pin 3 — V_{OUT}A — DAC A Voltage Output.

Pin 4 — V_{IN}A/B — DAC A and B Reference Voltage Input.

Pin 5 — V_{REF}L — DAC Reference Voltage Input Low, common to all DACs.

Pin 6 — PRESETL — Preset Input; active low; all DAC registers forced to 80_H.

Pin 7 — V_{IN}E/F — DAC E and F Reference Voltage Input.

Pin 8 — V_{OUT}E — DAC E Voltage Output.

Pin 9 — V_{OUT}F — DAC F Voltage Output.

Pin 10 — $V_{OUT}G$ — DACG Voltage Output.

Pin 11 — $V_{OUT}H$ — DACH Voltage Output.

Pin 12 — $V_{IN}G/H$ — DACG and H Reference Voltage Input.

Pin 13 — LOADH — Load DAC Register Strobe; active high input that transfers the data bits from the Serial Input Register into the decoded DAC Register. Refer to Table 1.

Pin 14 — CLOCK — Serial Clock Input; positive–edge triggered.

Pin 15 — SDO — Serial Data Output; active totem–pole output.

Pin 16 — GND — Ground.

Pin 17 — SDI — Serial Data Input.

Pin 18 — V_{DD} — Positive 5V Power Supply.

Pin 19 — $V_{IN}C/D$ — DACC and D Reference Voltage Input.

Pin 20 — $V_{OUT}D$ — DACD Voltage Output.

FEATURES…

The **SP9841** and **SP9842** include eight separate op amp–buffered eight–bit DACs. These can be used to replace up to eight trimpots with eight low–impedance programmable sources. The **SP9841** uses eight separate multiplying reference inputs, while the **SP9842** provides four pair of multiplying inputs. All of the reference inputs, in either case, are returned to a common voltage reference low pin. The inherent 2X gain from the two–quadrant multiplying reference inputs to the outputs allows the use of AC or DC multiplying reference inputs generated from a single, low supply voltage.

Each DAC has its own data register which holds its output state. These data registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded such that the first 4 bits determine the address of the DAC register to be loaded and the last 8 bits are the data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in mul-

LAST → FIRST

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A_0	A_1	A_2	A_3
LSB			DATA				MSB	LSB	ADDRESS		MSB

A_3	A_2	A_1	A_0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DACA
0	0	1	0	DACB
0	0	1	1	DACC
0	1	0	0	DACD
0	1	0	1	DACE
0	1	1	0	DACF
0	1	1	1	DACG
1	0	0	0	DACH
1	0	0	1	No Operation
.	.	.	.	.
.	.	.	.	.
1	1	1	1	No operation

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DAC Output Voltage $V_{OUT} = D/128 (V_{IN} - V_{REF}L) + V_{REF}L$
0	0	0	0	0	0	0	0	$V_{REF}L$
0	0	0	0	0	0	0	1	$1/128 (V_{IN} - V_{REF}L) + V_{REF}L$
				.				.
				.				.
0	1	1	1	1	1	1	1	$127/128 (V_{IN} - V_{REF}L) + V_{REF}L$
1	0	0	0	0	0	0	0	V_{IN} (Preset Value)
1	0	0	0	0	0	0	1	$129/128 (V_{IN} - V_{REF}L) + V_{REF}L$
				.				.
				.				.
1	1	1	1	1	1	1	0	$254/128 (V_{IN} - V_{REF}L) + V_{REF}L$
1	1	1	1	1	1	1	1	$255/128 (V_{IN} - V_{REF}L) + V_{REF}L$

Table 1. Serial Input Decoded Truth Table

tiple DAC applications without additional external decoding logic.

The **SP9841/9842** consume only 65 mW from a single +5V power supply. The **SP9841** is available in 24-pin plastic DIP and SOIC packages. The **SP9842** is available in a space–saving 20–pin SOIC package.

For applications requiring code–controlled output polarity reversal regardless of the reference input level (i.e. four–quadrant multiplication), please see the **SP9840/SP9843** product data sheet.

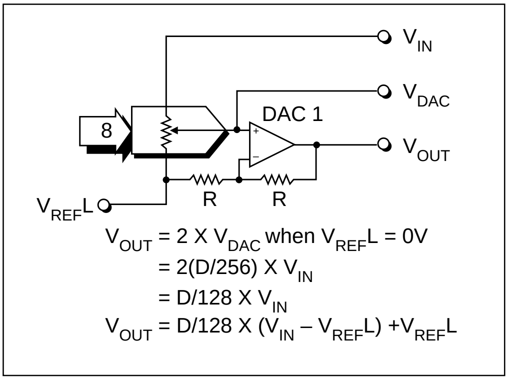


Figure 1. DAC and Output Amplifier Circuit

USING THE SP9841/9842
Theory of Operation

Each of the eight channels of the **SP9841/SP9842** can be used for signal reconstruction, as a programmable dc source, or as a programmable gain/attenuation block, multiplying an ac reference input by factors of 0 to 1.992. The rugged, wideband output amplifiers provide both current sink and source capability for dc applications, even those driving difficult loads. The dc source mode mimics the functionality of a programmable trimpot with the added benefit of a low impedance buffered output. The amplifier's bandwidth and high open–loop gain allow its use in programmable gain applications where even a low distortion, high resolution signal (such as audio) must be gated on and off or gain–controlled over a –42 to +6dB range.

Each channel consists of a voltage–output DAC, implemented using CMOS switches and thin–film resistors in a inverted R–2R ladder configuration. Each DAC drives the positive terminal of an op amp configured for a non–inverting gain of 2 using equal value thin–film feedback and gain–setting resistors. Signal ground is the V_{REFL} pin, the common reference input return for the 8 DAC–op amp channels. As shown in *Figure 1*, the DAC section can be thought of as a potentiometer across $V_{IN}(X)$ to V_{REFL}. When this potentiometer reaches its maximum output value of 255/256 times V_{IN}, the output will be $1+(R_{FB}/R_{GAIN})$ or 2 times the value of V_{DAC} (actually up to 1.9921875 times the input voltage, with V_{REFL} tied to ground). When the potentiometer is at its minimum value of 0/256, the output will try to be 0V, again assuming V_{REFL} is tied to ground.

The true relation between the dc levels at the V_{IN} pin, V_{REFL} and the output can be described as:

$$V_{OUT} = ((1 + R_{FB}/R_G) * (Data/256) * (V_{IN} - V_{REFL})) + V_{REFL}$$

where Data is programmable from 0 to 255, and $R_{FB} = R_G$.

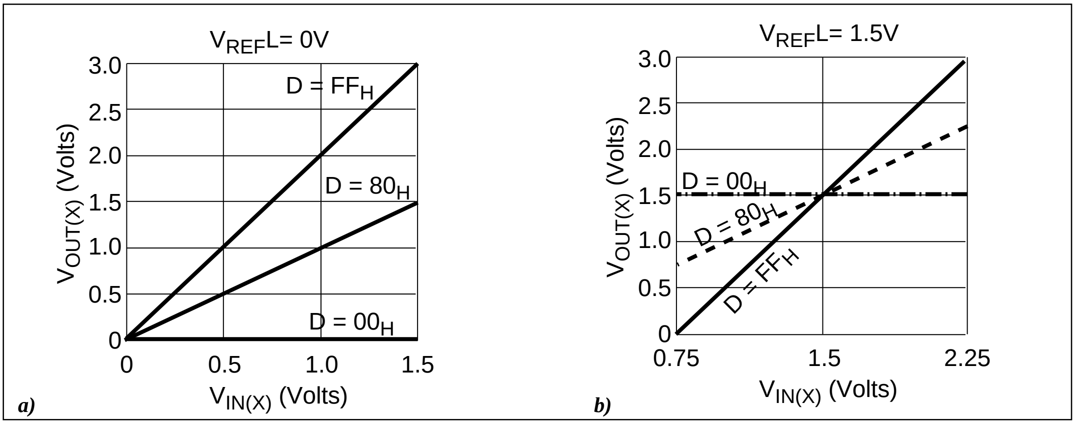


Figure 2. a) Single–Quadrant, and b) Two–Quadrant Operation

When V_{REFL} is tied to ground, this expression reduces to:

V_{OUT} = (Data/128) *V_{IN}

Multiplication of Input Voltages

While both the **SP9841** and **SP9842** are capable of two–quadrant multiplication, this terminology is not very precise when describing a system which runs from a single positive supply. Traditionally, the quadrants have been defined with respect to 0V. A two–quadrant multiplying DAC could produce negative output voltages only if a negative voltage reference were applied. A four–quadrant device could also produce a code–controlled negative output from a positive reference, or a code–controlled positive output from a negative reference. If ground is used to delineate the quadrants, then the **SP9841/SP9842** should be considered single–quadrant multiplying devices, as their output op amps cannot produce voltages below ground.

In reality, it is possible to define a dc voltage as a signal ground in a single supply system. If the DAC's V_{REFL} pin is driven to the voltage chosen as pseudoground, then each voltage output will exhibit 2–quadrant behavior with respect to pseudoground; that is the output voltage will enter the quadrant below the pseudoground only when the reference input voltage goes below pseudoground. This mode of operation is useful when implementing programmable gain/attenuator sections, especially when the input signal is bipolar with respect to pseudoground, or is ac–coupled into the V_{IN}(X) pin. When V_{REFL} is tied to power supply ground, only output voltages greater than V_{REFL} are possible, and the device performs single–quadrant multiplication, much like a buffered programmable trimpot across a single supply. *Figures 2a* and *2b* show single–quadrant and 2–quadrant performance of the **SP9841/SP9842**. Applications which require 4–quadrant operation with respect to pseudoground should use the **SIPEX SP9840** or **SP9843** 4–quadrant multiplying DACs.

The choice of voltage to use for the pseudoground is limited by the legal voltage swing at the op amp output. The op amp exhibits excellent linearity for output voltages between, conservatively, 100mV and V_{DD} – 1.5V. The op amp BiCMOS output stage consists of an npn follower loaded by an NMOS common sourced to ground. This circuit exhibits wide bandwidth and can source large currents, while retaining the capability of driving the output to voltages close to ground.

At output voltages below 25mV, feedback forces some op amp internal nodes toward the supply rails. The NMOS pull–down device gets driven hard and the NMOS device enters the linear range — it begins to function in the same manner as a 50 ohm resistor. In reality, the wideband amplifier output stage sinks some internal quiescent current even when driving the output towards ground. This sunk current drops across the output stage NMOS transistor ON–resistance and internal routing resistance to provide a minimum output voltage, below which the amplifier cannot drive. This minimum voltage is in the 15 to 25mV range. It varies within a package with each op amp's offset voltage and biasing variations. If an input voltage lower than this minimum, such as code 0 or 1, when V_{REFL} is ground,

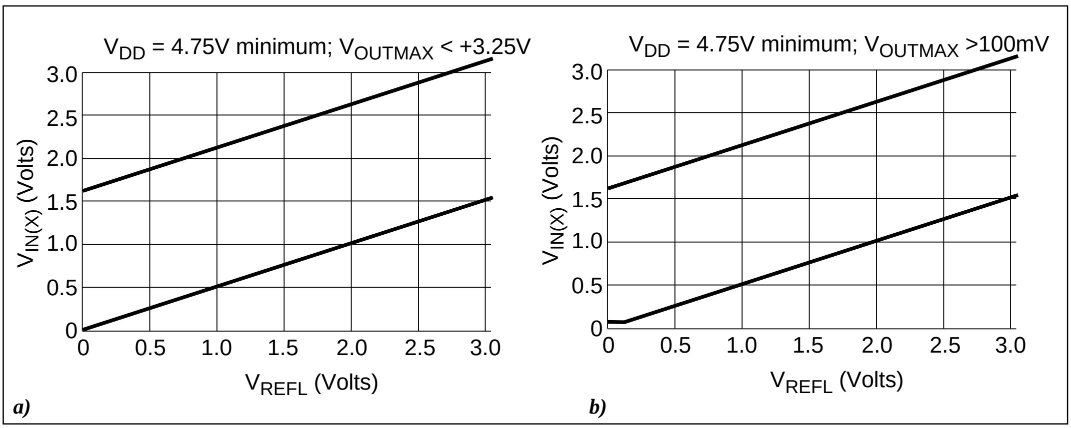


Figure 3. Reference Voltages a) Normal Operation; b) Maximum Linearity Near Code 1

is requested, feedback within the op amp circuit will force internal nodes to the rails, while the output will remain saturated near this minimum value. Non–saturated monotonic behavior returns between 25mV and 100mV at the output, but full open loop gain and linearity are not apparent until the output voltage is nearly 100mV above the negative supply. Applications which require good linearity for codes near zero should drive the V_{REFL} input at least 100mV above the ground pin, as this insures that the output voltage will not go below 100mV for any legal input voltage. Two–quadrant applications (programmable gain/attenuator) usually bias V_{REFL} up at system pseudoground, well above this saturation region, and therefore maintain linearity even at high attenuations (i.e. at code 1).

The allowable, useful values of V_{IN}(X) and V_{REFL} are limited if a legal output value is to be expected for all input codes. At maximum gain (DAC code 255) V_{OUT} is approximately equal to $2V_{IN}(X) – V_{REFL}$. By solving this equation twice, once with V_{OUT} set to 0V, and then again with Vout set to V_{DD}–1.5V, the chart of *Figure 3a* results. This chart can be used to find the maximal V_{IN}(X) voltage excursions for any given voltage driven into V_{REFL}. The upper line plots the maximum voltage at V_{IN}(X) and the lower line plots the minimum voltage at V_{IN}(X) at each value of V_{REFL} drive. Normal operation would be for V_{IN}(X) anywhere between the two lines. For example, assume a 4.75V supply voltage, and that the DAC code is set to 255. If V_{REFL} is driven to 1.6V, V_{IN}(X) below 0.8V would require the output amplifier to swing below ground. V_{IN}(X) above 2.425V would require output voltages greater than V_{DD} – 1.5V, or 3.25V.

Figure 3b shows the limits on V_{IN} when the minimum V_{OUT} is constrained to be greater than 100mV, for extremely linear operation, even at DAC code 1. In this case, the lower line is 50mV above its position in *Figure 3a*, except that below V_{REFL} = 100mV, the minimum input voltage stays at 100mV. It should be noted that V_{IN}(X) can always be driven to or slightly beyond the supply rails without harm. Under such circumstances, the DAC code can always be set to provide sufficient attenuation to get an undistorted output.

Driving the Reference Inputs

The V_{IN} inputs exhibit a code–dependent input resistance, as shown in the specifications. In general, these inputs should be driven by an amplifier capable of handling the specified load resistance and capacitance. The reference inputs are useful for both ac and dc input sources. However, series resistance into these pins will degrade the linearity of the DAC. A series resistance of 50 Ohms can cause up to 0.5LSB of additional integral linearity degradation for codes near full scale, due to the code–dependent input current dropping across this error resistance. AC–coupled applications should use the largest capacitor value (lowest series resistance) which is practical, or, use an external buffer to drive the inputs.

The DAC switches function in a break–before–make manner in order to minimize current spikes at the reference inputs. As previously noted, the reference inputs can withstand driving voltages slightly beyond the power supply rails without harm. The gain of 2 at the op amps limits the choice of V_{IN}/V_{REFL} combinations if clipping is to be avoided at the higher codes.

Output Considerations

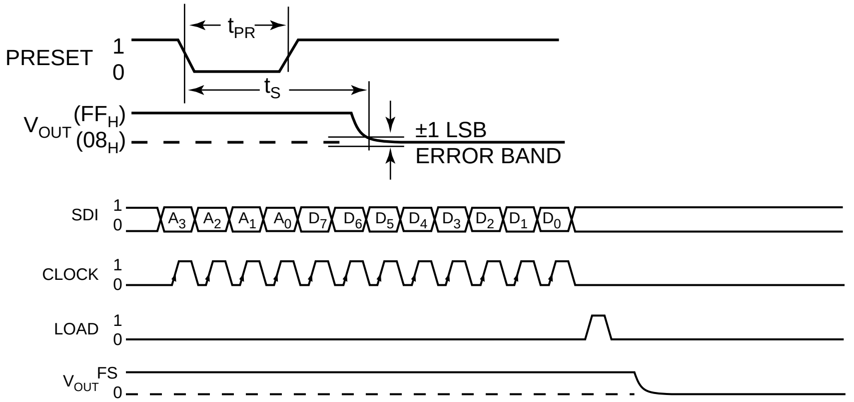
Each DAC output amplifier can easily drive 1Kohm loads in parallel with 15pF at its rated slew rate. The unique BiCMOS amplifier design also ensures stability into heavily capacitive loads — up to 47,000pF. Under these conditions, the slew rate will be limited by the instantaneous current available for charging the capacitance — the slew rate will be severely degraded, and some damped ringing will occur. Especially under heavy capacitive loading, a large, low impedance local bypass capacitor will be required. A 0.047µF ceramic in parallel with a low–ESR 2.2 to 10µF tantalum are recommended for worst–case loads.

The amplifier outputs can withstand momentary shorts to V_{DD} or ground. Continuous short circuit operation can result in thermally induced damage, and should be avoided.

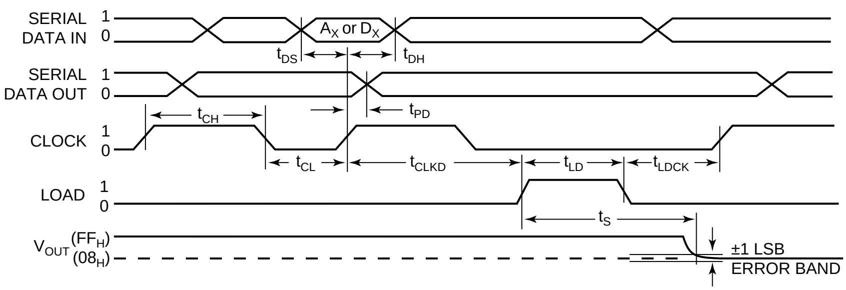
If the input reference voltage is reduced to 0.6V, then both the amplifier and DAC are functional at room temperature at supply voltages as low as 2.5V. At V_{DD} = 2.7V, power dissipation is 9.3mW typical, with the serial clock at 4MHz, or 7.0mW typical with the serial clock gated off.

Interfacing to the SP9841/SP9842

A simple serial interface, similar to that used in a 74HC594 shift–register with output latch, has been implemented in these products. A serial clock is used



SERIAL DATA INPUT TIMING DETAIL ($\overline{PRESET}$ = Logic "1"; $V_{IN(X)}$ = 1.5V; $V_{REF}L$ = 0V)



CHARACTERISTICS

(Typical @ 25°C with V_{DD} = +5V unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Clock Pulse Width (t_{CH}, t_{CL})	50			ns	
Data Setup Time (t_{DS})	30			ns	
Data Hold Time (t_{DH})	20			ns	
CLK to SDO Propagation Delay (t_{PD})			100	ns	
DAC Register Load Pulse Width (t_{LD})	50			ns	
Preset Pulse Width (t_{PR})	50			ns	
Clock Edge to Load Time (t_{CKLD})	30			ns	
Load Edge to Next Clock Edge(t_{LDCK})		60		ns	

Figure 4. Timing.

SDI	CLK	LOADH	PRESETL	LOGIC OPERATION
X	L	L	H	No Change
Data	↑	L	H	Shift In One Bit from SDI Shift Out 12–clock delayed data at SDO
X	X	X	L	All DAC Registers Preset to 80_H (Note 1)
X	L	H	H	Load Serial Register Data into DAC(X) Register

Note 1: "Preset" may not persist at all DACs if LOADH is high when PRESETL returns high.

Table 2. Logic Control Input Truth Table.

to strobe serial data into a 12–stage shift–register at each rising clock edge. The first four serial bits contain the address of the DAC to be updated, MSB first. The next 8 bits contain the binary value to be loaded into the desired DAC, again MSB first. After the 12th serial bit is clocked in, the LOADH line can be strobed to latch the 8 bits of data into the data holding register for the desired DAC. The address bits feed a decoding network which steers the LOADH pulse to the clock input of the desired DAC data holding register. The output of the 12th shift–register is also buffered and brought out as the SERIAL DATA OUT (SDO), which can be used to cascade multiple devices, or for data verification purposes.

The address field is set up such that DAC A is addressed at 0001 (binary). Address 0000(binary) will not affect the operation of any channel, as this combination is easily generated inadvertently at power–up. Other no–operation addresses exist at 1001(binary) through 1111(binary). Another use for no–operation addresses is to mask off updates of any DAC channel in a multiple–part system with cascaded serial inputs and outputs. By sending a valid address and data only to the desired channel, it is possible to simplify the system hardware by driving the LOADH pin at each part in parallel from a single source. *Table 1* shows a register–level diagram of the addresses, data, and the resulting operation.

A fourth control pin, PRESETL, can be used to simultaneously preset all DAC data holding registers to their mid–scale (80_H) values. This will asynchronously force all DAC outputs to buffer the voltages at their respective inputs to their outputs with unity gain. This feature is useful at power–up, as a simple resistor to the supply and capacitor to ground can insure that all DAC outputs start at a known voltage. It can also be used to implement stand-alone (non–programmed) applications, such as a unity gain octal cable driver. *Table 2* summarizes the operation of the four digital control inputs.

The four digital control input pins have been designed to accept TTL (0.8V to 2.0V minimum) or full 5V CMOS input levels. Timing information is shown in *Figure 4*. Serial data is fully clocked into the shift–register after 12 clock rising edges, subject to the described setup and hold times. After the shift–register data is valid, the LOADH line can be pulsed high to load data into the desired DAC data register, which switches the DAC to the new input code. The serial clock input should not see a rising edge while the LOADH pulse is high in order to prevent shift–register data from corruption during data register loading.

The serial clock and data input pins are designed to be compatible as slaves under **National Semiconductor**'s Microwire™ and MicrowirePlus™ protocols and under **Motorola**'s SPI™ and QSPI™ protocols. In some micro–controllers, the interface is completed by programming a bit in a general–purpose I/O port as a level, used to strobe the LOADH line at the DACs. This is done in a manner similar to that used for generating a $\overline{CS}$ signal, which is necessary when driving some other Microwire™ peripherals.

Low Voltage Operation

At nominal V_{DD}, the CMOS switches used in the DAC obtain sufficient drive to maintain an ON-resistance much lower than the thin–film resistors. This keeps the non–linear voltage–dependent portion of their ON-resistances low, and guarantees both excellent DAC linearity versus code, and low–distortion multiplication of large–swinging AC inputs. The devices in the op amp also receive sufficient drive to guarantee the specified bandwidth and output drive current. However, all circuits within the DACs are quite "functional" at very low values of V_{DD}. By reducing the reference voltages such that the maximum V_{OUT} is near the target of V_{DD}-1.5V, the DACs will provide better than 0.5LSB typical integral performance for DC output voltages between 100mV and V_{DD}-1.5V. Reducing the reference voltage actually aids the linearity of the DACs, even at nominal V_{DD}. This occurs because the NMOS half of the CMOS switches are more fully utilized at reference voltages closer to ground, thus further reducing the ON–resistance of the switches. Reference input currents are proportional to the reference voltages and will also decrease with the reference voltages.

Plot 19 shows typical DC output linearity for V_{IN}(X) set to 0.5V, with V_{DD} at 2.5, and then 3.5V. Note that at 3.5V, the linearity is actually much better than the ±0.25LSB typical performance at V_{IN}(X) = 1.625V and V_{DD} = 5V. Similarly, *Plot 20* shows that this performance level persists for V_{DD} = 4.5V and 5.5V, with V_{IN}(X) set to 0.6V. The price paid for low voltage operation is in op amp gain, bandwidth and es–pecially current sinking at the DAC output. *Plots 17*

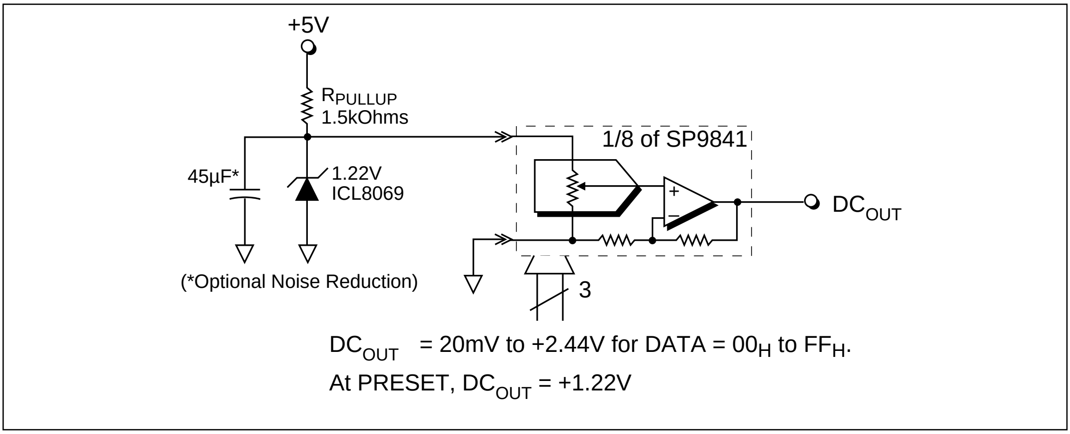


Figure 5. Inexpensive DC Source.

through 19 show that for lower output current values less than 1 mA, the **SP9841/9842** can be used effectively even with V_{DD} in the range of 2.7 to 3.3V.

Application Circuits

Figure 5 shows an inexpensive single–quadrant DC source for generating voltages from near ground to near 2.44V. When using a two–terminal reference, the pull–up resistor should be chosen so that the minimum input resistance of 5kOhms at each $V_{IN}(X)$ can be driven at the lowest expected V_{DD}. At V_{DD} = 4.75V, and V_{REFL} = 1.25V, each input to be driven needs 0.248mA, and the regulator needs 0.1mA to stay well regulated. Thus, to drive all eight inputs, R_{PULLUP} should be chosen to supply at least 2mA. To operate at 4.75V, 1.75kOhms is required; the 1.5kOhms shown will suffice even if its value is 5% high. To drive a single input, a 10kOhm value could be used. In order to reduce reference and supply generated noise, an optional capacitor of 1 to 100µF bypasses the reference.

Figure 6 shows a circuit which generates DC voltages roughly symmetric with respect to 2.446V. Two bandgap references are stacked to first drive V_{REFL} to 1.223V, and the input to 2.446V. The pull–up resistor value should again be scaled for worst–case loading — in order to drive all eight inputs at 4.75V, a value of 620 Ohms is required. At fullscale, the DAC output is near 3.65V. While typical units will source 5mA at an output voltage

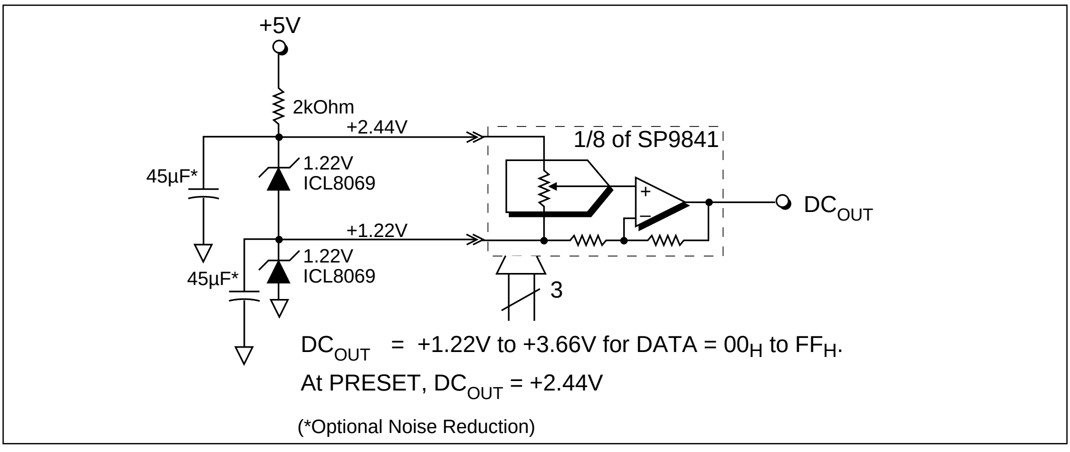


Figure 6. Pseudo Bipolar Source Generates Voltages Above and Below 2.44V.

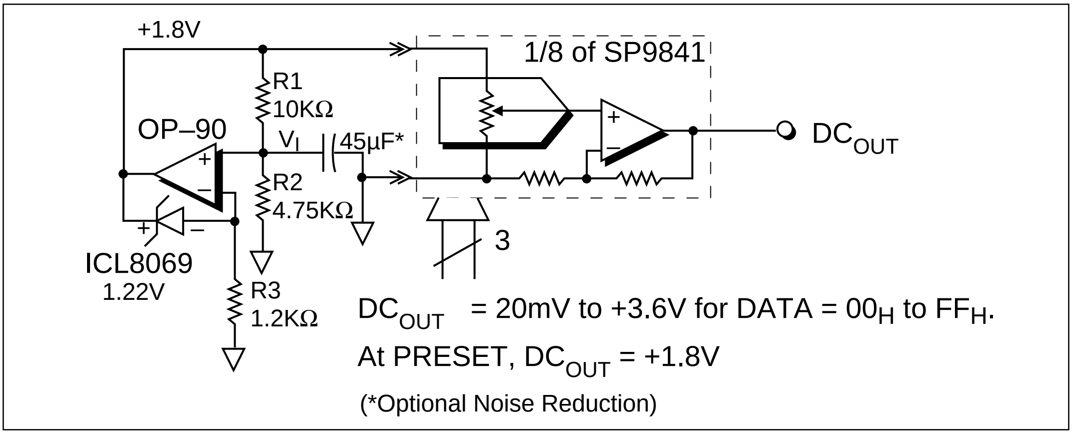


Figure 7. Generating Programmable DC Voltages.

of 3.75V while running from a 4.75V supply, this behavior is not tested in device production. If maximum linearity is required near the 3.66V fullscale voltage, then output loading should be kept under 1mA.

Figure 7 uses a 1.8V reference to provide an output voltage range from near ground to almost 3.6V. The external micropower reference uses a bandgap in a bootstrapped configuration, which guarantees excellent supply rejection. Voltage at V_1 is set by

$$1.223 * \left(\frac{R2}{(R1 + R2)} \right)$$

V_{OUT} is 1.223V $+V_1$. R_3 is used to set the quiescent current through the bandgap, $I=V_1/R_3$. The op amp will easily drive one to all eight inputs.

Figure 8 shows a non–programmed standalone application. By tying PRESETL to ground, all channels are permanently set to unity gain. While preset, the input impedance at each input is set to 40kOhms nominal (20kOhms minimum), which minimizes required input current drive. The TL431 reference is programmed by resistors R_1 and R_2 for 3.3V. R_3 is chosen to provide at least 165µA for each input driven, plus 0.5mA for the reference at the minimum supply value to be considered. In the *Figure*, the 560 Ohms shown will drive all eight inputs. The excellent capacitive load capability of the output amplifiers handles any value of capacitive bypass loads without oscillation; however, to minimize ringing at powerup, load capacitance can be chosen to be greater than 0.1µF or less than 1,000pF.

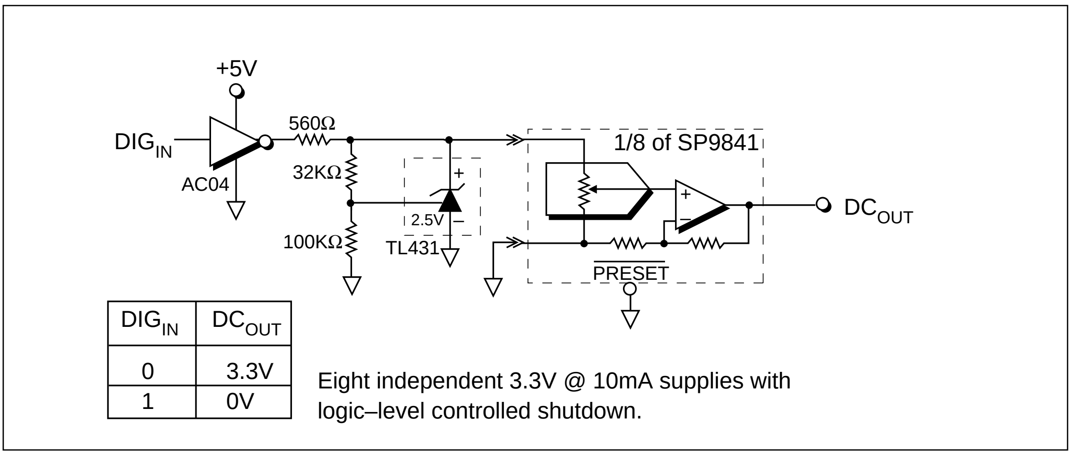


Figure 8. Generating Up to Eight (8) 3.3V @ 10mA DC Supplies with Logic–Level Controlled Shutdown (Non–Programmed).

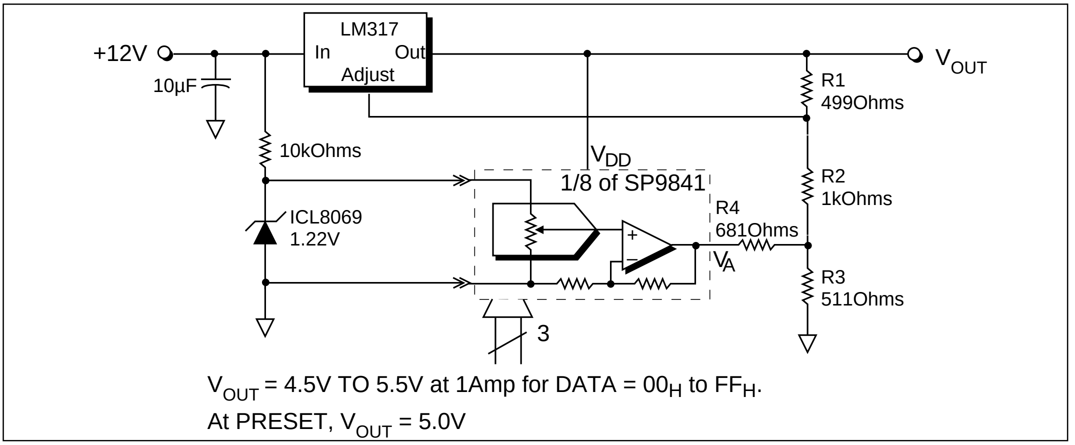
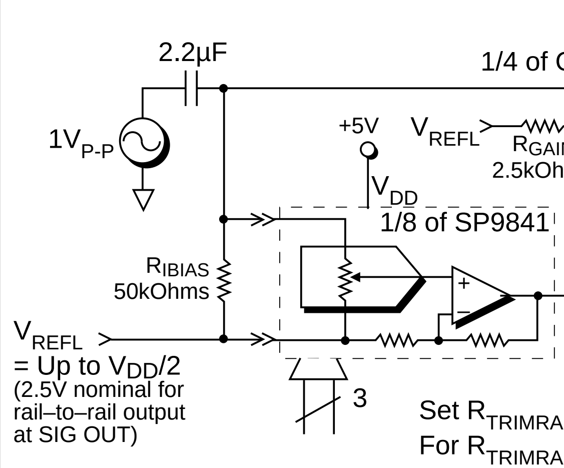


Figure 9. Programmable 1Amp Power Source.

Figure 9 shows a DAC channel controlling the output voltage of an LM317 voltage regulator. By programming the code, the DAC changes its own supply voltage. This circuit can be modified for wider output voltage ranges by reducing the value of R_4. However, the circuit as shown requires the DAC to sink 1mA to the negative rail at code 0 at its lowest V_{DD}, at which point the output voltage is 62mV. Thus, programming codes 0 through 5 will do little to influence the output. If R_4 is replaced with a short circuit, useful operation would be between 3.9V and 6.15V output; however, the DAC output must then sink 2.5mA at V_{DD} = 3.9V, which results in a minimum DAC output voltage of around 150mV. Codes above 17 will then provide equally spaced output voltage increments.

Figure 10 shows how the gain of an external non–inverting op amp can be programmed. R_F and R_G are chosen for nominal gain. $R_{TRIMRANGE}$ is then ratioed to R_F to provide the desired range of gain trim. A wide gain grange is achievable — for example, with R_F = 11kOhms, R_G = 1kOhms and $R_{TRIMRANGE}$ = 2.74kOhms, gain would be programmed linearly from 8 to just under 16.

The OP–491 shown in *Figure 10* is capable for



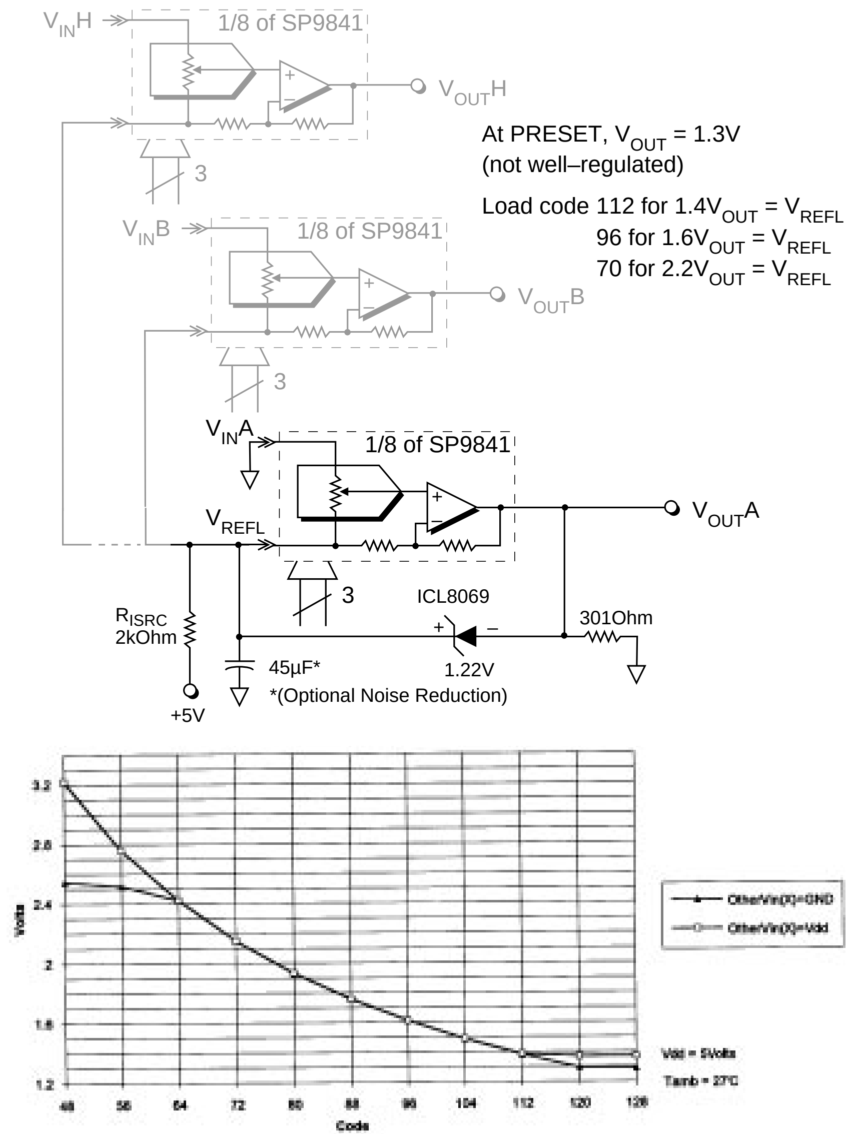
$$A_V = 1 + \frac{R_F}{R_G} + \left(1 - \frac{D}{128}\right)\frac{R_F}{R_{TRIMRANGE}}, \text{ D = 0 to 255}$$

Set $R_{TRIMRANGE}$ for desired gain-trim range.
For $R_{TRIMRANGE}$ = 20kOhms:
Code 0, A_V = +5.5
Code 128, A_V = +5.0
Code 255, A_V = +4.51

Figure 10. Adjustable Gain of External Non–Inverting Opamp Circuit; V_{OUT} = Rail–to–rail.

rail–to–rail output swing. In order to obtain this performance, V_{REFL} must be externally driven to $V_{DD}/2$, perhaps by use of the circuit of *Figure 11*. At V_{REFL} near 2.5V and V_{DD} = 4.75V, the typical positive output headroom at the DAC is limited to 1.15V above 2.5V, so that this circuit is useful for rail–to–rail outputs for gains higher than 4.35 (i.e. $1.15V_{PP}$ maximum input). Note that while an AC–coupled input is shown, this circuit is just as useful for DC–coupled inputs which are generated with respect to the V_{REFL} pseudoground voltage. R_{IBIAS} is used for the AC–coupled circuit for opamp bias current return when the DAC is programmed to code 0, as no current flows into V_{IN}(X) at code 0.

Figure 11 shows a minimal parts count method



The usable range for the bootstrapped V_{REFL} circuit is 1.4 to $2.4V_{OUT}$ at V_{DD} = 5V, R_{ISRC} = 2kOhms. To increase the upper usable limit, decrease value of R_{ISRC}.

Figure 11. Programmable, Bootstrapped, 1.4V to 2.2V V_{REFL} Drive.

of generating a programmable pseudoground voltage at the V_{REFL} terminal. A pseudoground is very useful if any channels are to be used in AC–multiplying applications. In such applications, the pseudoground will set the DC offset of the output signal. The voltage output of this circuit as the code is decreased is non–linear because the DAC bootstraps the increased output voltage by a larger fraction at each code. It is really meant to be programmed only over a range of codes between 104 and perhaps 60. It does exhibit a fairly well–defined output, even if non–intentional codes are programmed. For codes above 112, the output stage resembles a 50 Ohm resistor to ground, and the V_{REFL} output will be near 1.3V, depending upon the loading at the other $V_{IN}(X)$ inputs. For codes below 60, the output voltage will continue to rise until limited by available current through R_{ISRC}. Note that R_{ISRC} supplies the actual current into V_{REFL}, and must be chosen in order to supply enough current for all channels, especially if any of the other eight inputs are to be grounded. A plot of V_{REFL} versus code is shown with the *Figure*, for all other inputs either grounded or tied to the supply.

Figure 12 shows a programmable gain/attenuator section using the programmable VREFL drive. The VREFL of each DAC is actually internally connected. When the optional 45µF noise reduction capacitor is included, this circuit is capable of 86dB of SNR and 74 to 84dB of SINAD at 1kHz, depending on the pro-

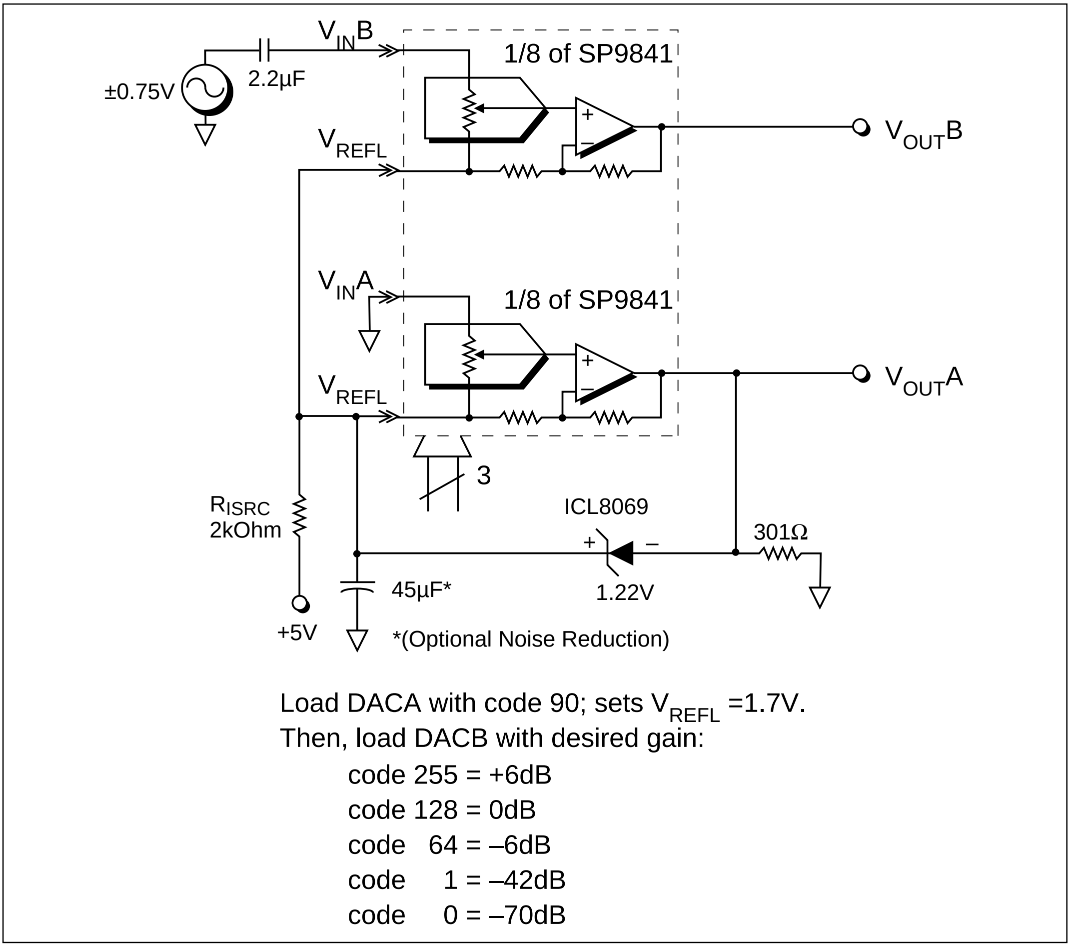


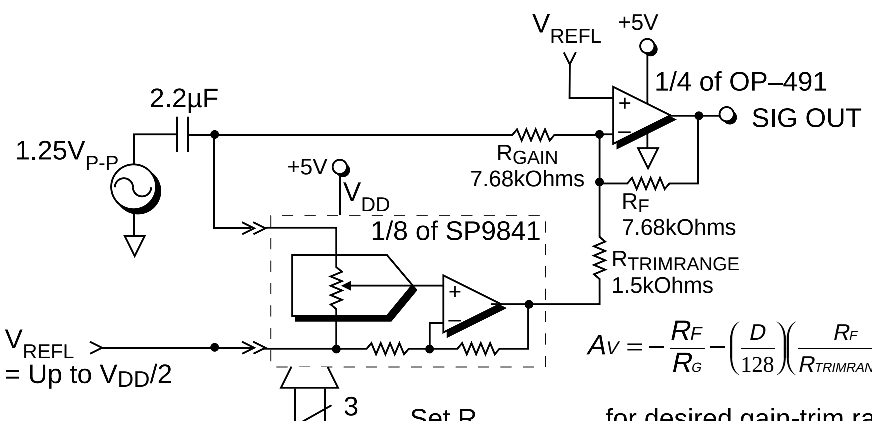
Figure 12. AC–Coupled, Programmable Gain/Attenuator with Bootstrapped Programmable Output DC Offset (V_{REFL} Drive).

grammed gain. Please refer to the THD versus Frequency plot, which was generated by terminating a 600 Ohm source with 150 Ohms to ground, then into this circuit. For the best gain linearity versus code, use the largest (lowest series impedance) coupling capacitor available, or externally buffer the input.

Figure 13 shows an external op amp with an inverting programmable gain. In this circuit the maximum output swing at the DAC occurs at the maximum circuit gain. Thus, the headroom restriction at the DAC output applies at the maximum gain, which, for rail–to–rail outputs (V_{REFL} = 2.5V or $V_{DD}/2$) should be greater than 4.3. By making the programmable gain range large, this circuit can be used to provide rail–to–rail outputs even at the lower gains. This circuit has been ratioed to provide exact integer gain increments for every increase in 25 codes, over the range of –1 to –11. This large range of gain comes at a slight cost — the output offset of the DAC amplifier will be gained up by –5.12 times at SIG OUT. If this is a problem, a second DAC channel can be set up with a programmable DC offset adjustment with its output summed through a large resistor into the OP–491 inverting terminal. Note that when RTRIMRANGE is set up for only unity gain change range as in *Figure 12*, only –0.5 times the DAC output offset will appear at SIG OUT.

Another application for the circuits of both *Figure 10* and *13* could be to force precise gains from circuits made from imprecise resistors. By restricting the programmable gain range to ±2% (by setting $R_{TRIMRANGE}$ to be 100 times R_F), the resistors could be 1% values and the programmable gain resolution would increase to better than 12–bits (0.0156%). In this case, only 1% of the DAC output offset voltage would appear at SIG OUT.

Figure 14 shows a window comparator and two channels of programmable-gain input. While the input signal is shown as AC–coupled, DC signals of up to rail–to–rail amplitude could be measured by setting the attenuation at the signal



$$A_V = -\frac{R_F}{R_G} - \left(\frac{D}{128}\right)\left(\frac{R_F}{R_{TRIMRANGE}}\right), \text{ D = 0 to 255}$$

Set $R_{TRIMRANGE}$ for desired gain-trim range.
For $R_{TRIMRANGE}$ = 1.5kOhms:
Code 0, A_V = -1
Code 25, A_V = -2
Code 75, A_V = -4
Code 175, A_V = -8
Code 225, A_V = -10
Code 250, A_V = -11
Gain resolution = 4%

Figure 13. Adjustable Gain of External Inverting Opamp Circuit, V_{OUT} = Rail–to–Rail.

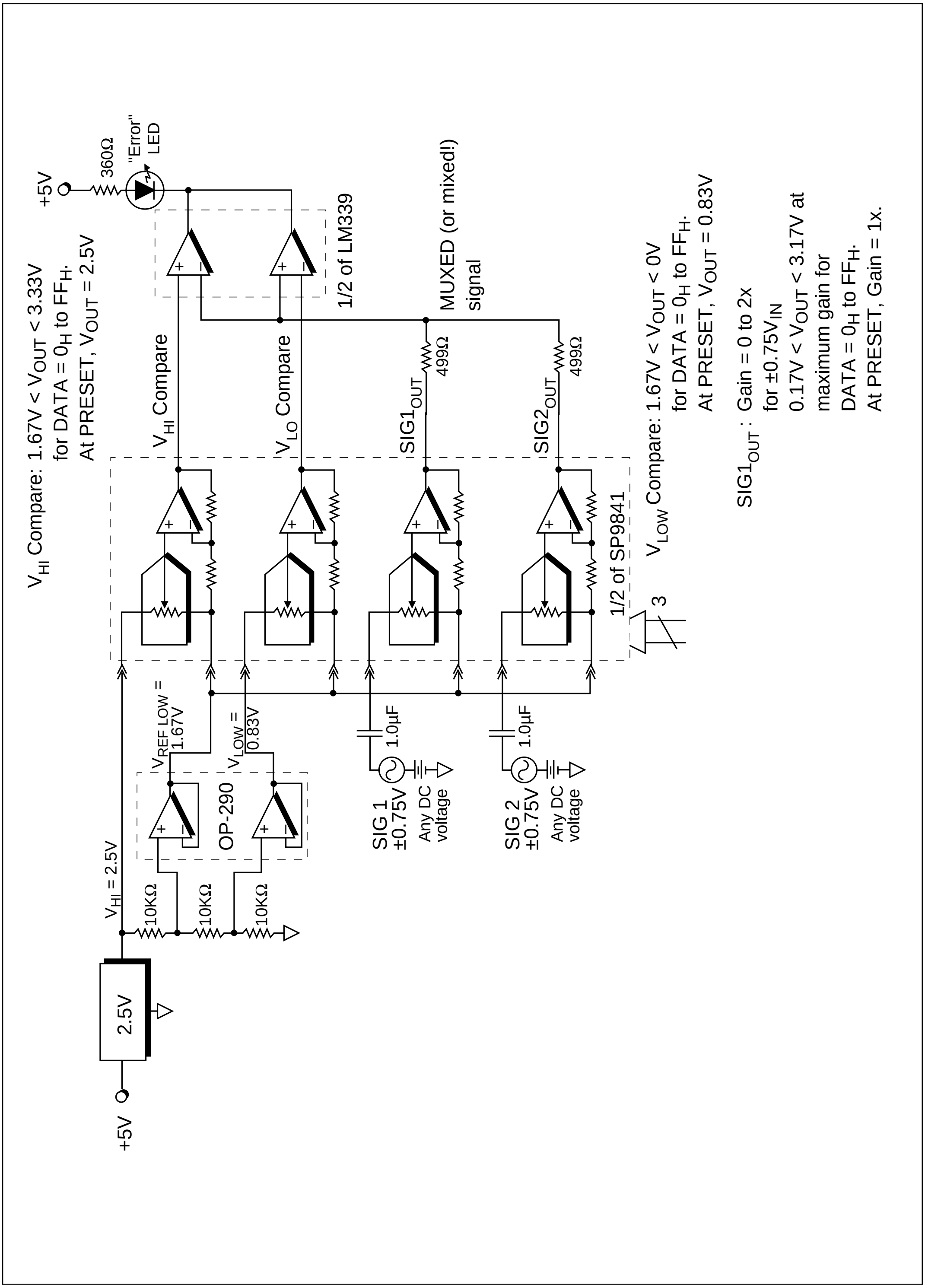


Figure 14. Two–Channel Multiplexed Window Comparator with Programmable Gain and Limits.

input DACs to the proper code. The LM339 does not really drive the LED to full illumination, due to limited output current, but a pull–up resistor alone will yield a functional TTL error signal. External op amps could use the V_{REFL} voltage as pseudoground. The outputs of the two signal DACs must be isolated with resistors if the two signals are to be multiplexed. This will reduce the signal gain to 255/256 maximum, due to the resistive divider created at the comparator input. If only a single channel was to be window–compared, then the maximum gain to the comparator would be the usual 255/128.

Figure 15 shows the schematic of an evaluation board, which can be used with an IBM–compatible (XT or AT) computer and the simple QuickBasic routine of *Figure 16* to load each DAC channel with its desired code. A straight–through 25-pin cable can be used, or the board can be plugged directly into the back of the PC.

Data is first latched into each 'HC165 parallel–to–serial converter. Then a small state machine is initiated by strobing $\overline{\text{INI}}$. It clocks the latched data into the serial data input and strobes the LOADH input at the DAC. A pair of banana jacks is used for applying V_{DD} from an external supply. A trimpot–adjustable voltage reference is tied to all eight DAC inputs. On the evaluation board, jumpers will allow this reference to drive any V_{IN}(X) input or the V_{REFL} pin. The other three op amps in the quad OP–491 are available for breadboarding circuits, such as in *Figures 1* through *14*. If the reference voltage is adjusted down to 0.5V, the DAC and the board should function with V_{DD} as low as 2.5V.

Driving Capacitive Loads

Unlike many other products, the **SP9841/9842** will not oscillate under purely capacitive loading. However, fullscale step outputs will show overshoot and ringing of up to 40% at worst–case purely capacitive loading (between 1,000 and 10,000pF). *Figures 17* through *20* show near fullscale steps under capacitive loads of between 470pF and 0.47µF. For capacitance up to 10,000pF, the addition of a resistive load to ground at the op amp output will decrease settling times without adversely affecting the positive–going slew rate. For higher capacitances, this settling time enhancement comes at the expense of positive slew rate, as not all instantaneous current can be used to charge the capacitor. For all values of capacitive load, settling time can be dramatically reduced by adding a small resistor in series with the DAC outputs. Such series resistors will degrade the current sinking ability at the DAC outputs for voltages near ground; while the DACs typically sink 2mA at V_{DD} =5V at V_{OUT} = 110mV, the addition of a 50Ohm resistor would require 210mV after the resistor to sink 2mA. Large capacitances require lower values of series resistance in order to obtain critical damping.

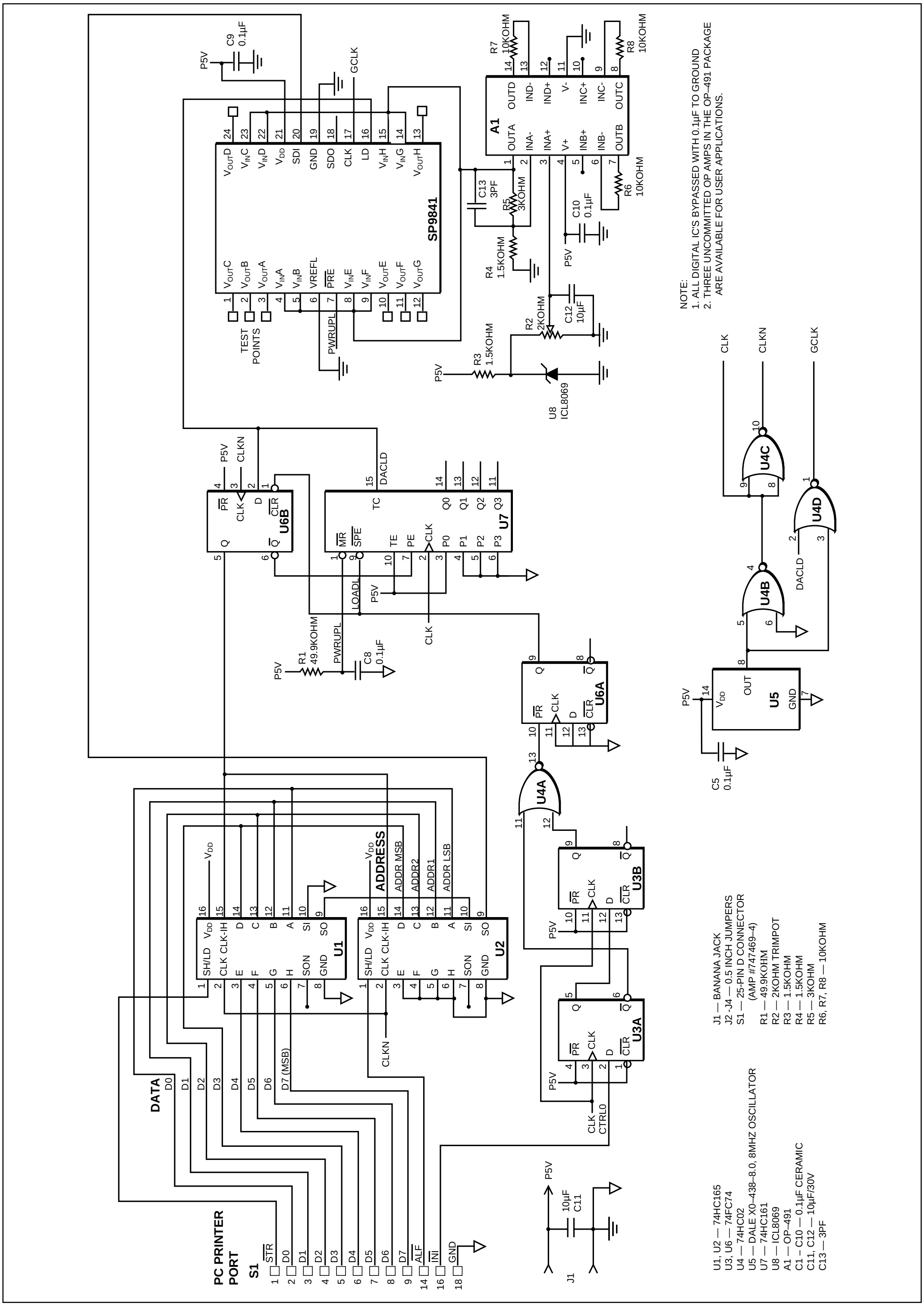


Figure 15. Evaluation Board — Loads SP9841/9842 from IBM PC Parallel Port

```
                              SP9841.BAS

'This program accepts an address (1 through 8) and data (0 through 255)
'in decimal and sends them to the DAC.  Addresses 1 through 8 will
'correspond to converters A through H respectively.  The appropriate
'output will be:  Vout-(data/128)*VREF volts.

'We found that for our IBM PC/AT the LPT1 port address was 378H (Data
'Register 378H and control register 37AH) while for our IBM PC/XT the
'LPT1 port address was 3BCH (Data Register #BCH and control register 3BEH).

DIM lsb AS INTEGER
DIM msb AS INTEGER
DIM datareg AS INTEGER
DIM contrlreg AS INTEGER
DIM n AS INTEGER
CLS
     DO
     INPUT "Enter type of PC, AT or XT: ", type$
     IN UCASE$(type$) = "AT" OR UCASE$(type$) = "XT" THEN
     EXIT DO
     ELSE PRINT "Please enter either AT or XT.": PRINT
     END IF
     LOOP

IF UCASE$(type$) = "AT" THEN datareg = &H378: cntrlreg = &H37A
IF UCASE$(type$) = "XT" THEN datareg = &H3BC: cntrlreg = &H3BE
CLS
n=0
DO   WHILE n=0
     DO
     test$ =""
     INPUT "Enter Address (1 through 8): ", lsb
     IF lsb < 1 or lsb> 8 THEN test$ = "false"
     IF test$ = "false" THEN PRINT "Please enter a valid address.": PRINT
     LOOP UNTIL test$ <> "false"

     DO
     test$ = ""
     PRINT
     INPUT      "Enter Data (0 through 255 in decimal): ", msb
     IF msb < 0 or msb > 255 THEN test$ = "false"
     IF test$ = "false" THEN PRINT "Please enter valid data.": PRINT
     LOOP UNTIL test$ <> "false"

     OUT cntrlreg, $H3          'set both latch clocks low
     OUT datareg, &H0 + msb     'send most significant byte to port
     OUT cntrlreg, &H2          'clock U1

     OUT datareg, &H0 + lsb     'send least significant byte to port
     OUT cntrlreg, &H0          'clock U2
     OUT cntrlreg, &H4          'enable U7, set U1 & U2 to serial out mode

     PRINT :   PRINT "Strike spacebar to enter new data or Q to quit."
               DO
               X$ = INKEY$
               IF UCASE$(X$) = "Q" THEN n=1
               LOOP UNTIL X$ = " " OR UCASE$(X$) = "Q"
LOOP
END
```

Figure 16. Microsoft qbasic Program to Load Evaluation Board with Desired Codes.

ORDERING INFORMATION

Model	Reference Inputs	Temperature Range	Package
SP9841KN	Eight, independent	0° to + 70°C	24–pin, 0.3" Plastic DIP
SP9841KS	Eight, independent	0° to + 70°C	24–pin, 0.3" SOIC
SP9842KS	Four pair	0° to + 70°C	20–pin, 0.3" SOIC
SP9841BN	Eight, independent	–40° to + 85°C	24–pin Plastic, 0.3" DIP
SP9841BS	Eight, independent	–40° to + 85°C	24–pin, 0.3" SOIC
SP9842BS	Four pair	–40° to + 85°C	20–pin, 0.3" SOIC