# Quad Reset Supervisor with Manual Reset Input

**Check for Samples: TPS386596L33**

## FEATURES

- **4 Voltage Monitors**
- **Threshold Accuracy: 0.25% (Typical)**
- **Fixed 50ms $\overline{\text{RESET}}$delay time**
- **Active Low Manual Reset Input**
- **Very Low Quiescent Current: 7µA typical**
- **SVS-1: Fixed Threshold for monitoring 3.3V**
- **SVS-2/3/4 – Adjustable Threshold Down to 0.4V**
- **Open Drain $\overline{\text{RESET}}$ Output**
- **Space Saving 8-pin MSOP Package**

## APPLICATIONS

- **Notebook / Desktop Computers**
- **Industrial Equipment**
- **Telecom, Networking Infrastructure**
- **Server, Storage Equipment**
- **DSP and Microcontroller Applications**
- **FPGA/ASIC Applications**

## DESCRIPTION

The TPS386596L33 monitors four power rails and asserts the $\overline{\text{RESET}}$ signal when any of the SENSE inputs drop below their respective thresholds. SVS-1 can be used to monitor a 3.3V nominal power supply with no external components required. SVS-2, SVS-3, and SVS-4 are adjustable using external resistors and can be used to monitor any power supply voltage higher than 0.4V. All SENSE inputs have a threshold accuracy of 0.25% (typical). The TPS386596L33 also has an active low Manual Reset ($\overline{\text{MR}}$) that can be used to assert the RESET signal as desired by the application. The open drain, active low $\overline{\text{RESET}}$output de-asserts using a fixed 50ms delay.

The TPS386596L33 has a low quiescent current of 7µA typical and is available in a space saving 8-pin MSOP package.

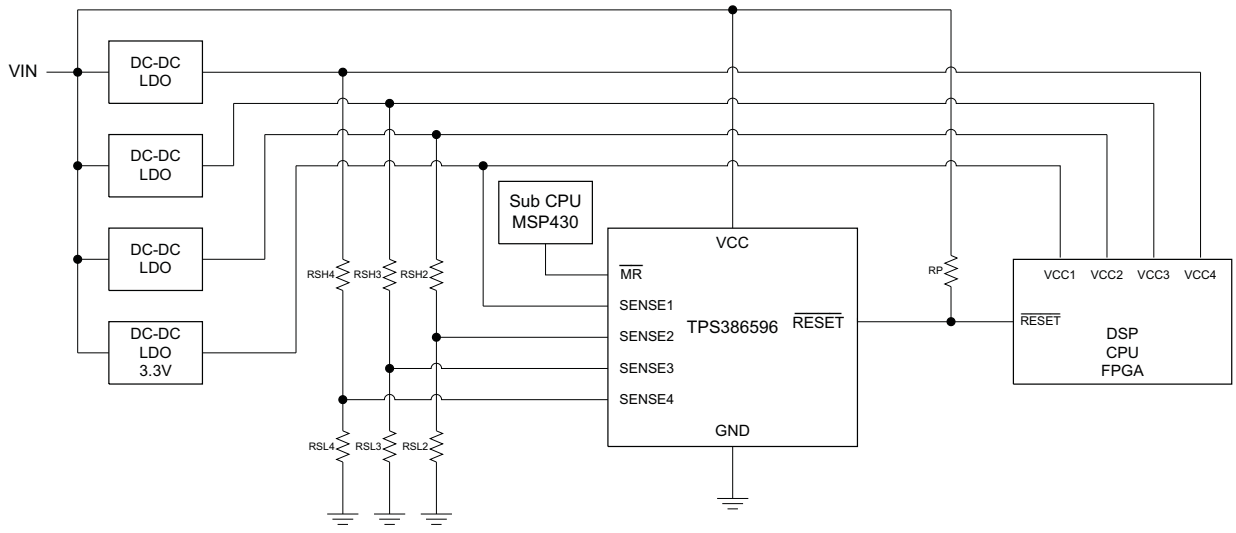



**Figure 1. TPS386596L33 Typical Application Circuit**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Custom threshold voltages from 0.80V to 4.6V, 4.8V to 6.0V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | TPS386596 | UNIT |
|---|---|---|
| Input voltage range, VCC | –0.3 to 7.0 | V |
| Other voltage ranges: $V_{MR}$, $V_{SENSE1}$, $V_{SENSE2}$, $V_{SENSE3}$, $V_{SENSE4}$, $V_{RESET}$ | –0.3 to 7.0 | V |
| $\overline{RESET}$pin current | 5 | mA |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 500 | V |
| Continuous total power dissipation | See Thermal Information Table | |
| Operating virtual junction temperature range, $T_J$ | –40 to 150 | °C |
| Operating ambient temperature range, $T_A$ | –40 to 125 | °C |
| Storage temperature range, $T_{stg}$ | –65 to 150 | °C |

(1) Stresses beyond those listed under *Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS386596 DGK (8 PINS) | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 183.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 70.7 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 72.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 68.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

Over the operating temperature range of $T_J$ = –40°C to +125°C. 1.8V < VCC < 6.5V, $R_{/RESET}$ = 100kΩ to VCC, $C_{/RESET}$ = 50pF to GND, unless otherwise noted. Typical values are at $T_J$ = +25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VCC}$ | Input supply range | | 1.8 | | 6.5 | V |
| $I_{VCC}$ | VCC Supply current (current into VCC pin) | $V_{CC}$ = 3.3V, $\overline{RESET}$ not asserted | | 7 | 19 | µA |
| | | $V_{CC}$ = 6.5V, $\overline{RESET}$ not asserted | | 7.5 | 22 | µA |
| | Power-up Reset Voltage(1) (2) | $V_{OL(max)}$ = 0.2V, IRESET = 15µA | | | 0.9 | V |
| $V_{ITn}$ | Negative-going Input Threshold Accuracy | SENSE1 | 2.87 | 2.90 | 2.93 | V |
| | | SENSE2, SENSE3, SENSE4 | 396 | 400 | 404 | mV |
| $V_{HYS}$ | Hysteresis (Positive-going) on VIT pin | SENSE1 | | 25 | 72 | mV |
| | | SENSE2, SENSE3, SENSE4 | | 3.5 | 10 | mV |
| $t_w$ | Input pulse width to SENSEn and $\overline{MR}$ pins | SENSEn: 1.05VIT ≥ 0.95VIT | | 4 | | µs |
| | | $\overline{MR}$: 0.7VCC ≥ 0.3VCC | | 50 | | ns |
| $I_{SENSE1}$ | Input Current at SENSE1 | VSENSE1 = 3.3V | 2.2 | 2.75 | 3.3 | µA |
| $I_{SENSEn}$ | Input Current at SENSEn pin, n = 2, 3, 4 | VSENSEn = 0.42V | -25 | | 25 | nA |
| $t_d$ | $\overline{RESET}$delay time | | 30 | 50 | 70 | ms |
| $V_{IL}$ | $\overline{MR}$ logic low input | | 0 | | 0.3Vcc | V |
| $V_{IH}$ | $\overline{MR}$logic high input | | 0.7Vcc | | | V |
| $R_{MR\_Pullup}$ | Internal pullup resistor on $\overline{MR}$ pin to VCC | | | 100 | | kΩ |
| $V_{OL}$ | Low-level $\overline{RESET}$ output voltage | $I_{OL}$ = 1mA | | | 0.4 | V |
| | | SENSEn = 0V, 1.3V < VCC < 1.8V, $I_{OL}$ = 0.4mA(1) | | | 0.3 | |
| $I_{LKG}$ | $\overline{RESET}$ Leakage Current | $V_{\overline{RESET}}$ = 6.5V, $\overline{RESET}$ not asserted | –300 | | 300 | nA |
| $C_{IN}$ | Input pin capacitance | | | 5 | | pF |

(1) These specs are out of recommended VCC range and only define $\overline{RESET}$ output performance during VCC ramp up.
(2) The lowest supply voltage (VCC) at which $\overline{RESET}$ becomes active. Trise(VDD) ≥ 15us/V.

## FUNCTIONAL BLOCK DIAGRAM

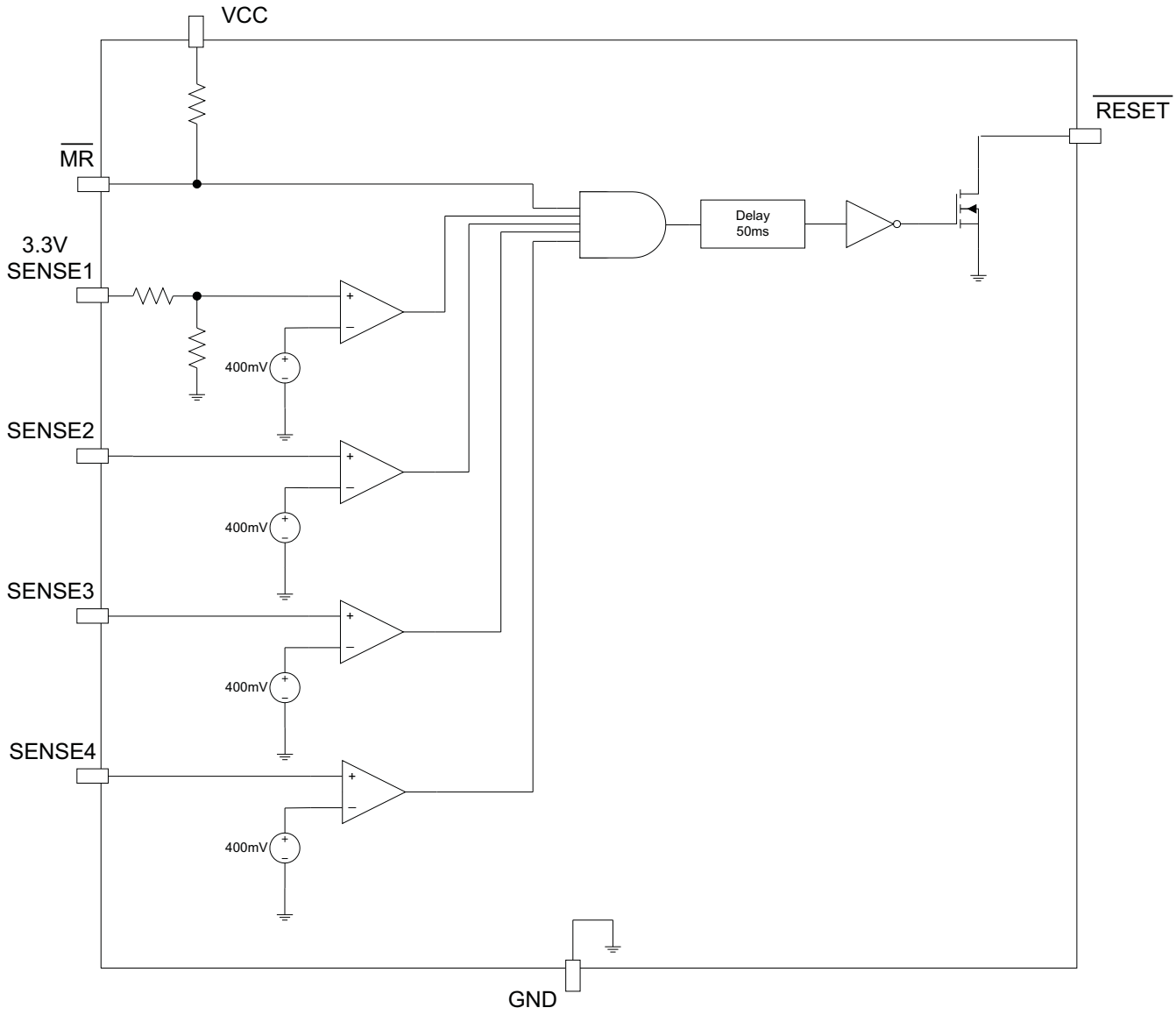
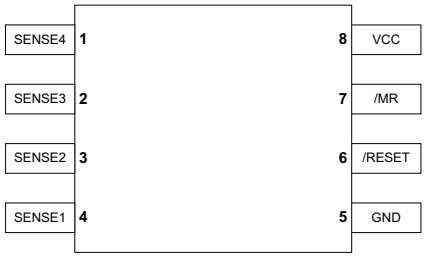



**Figure 2. TPS386596L33 Block Diagram**

# DEVICE INFORMATION

## PIN CONFIGURATION




MSOP-8

### PIN FUNCTIONS

| PIN | | DESCRIPTION | |
|---|---|---|---|
| NAME | NO. | | |
| SENSE1 | 4 | Monitor voltage input for Supply 1 | When the voltage at this terminal drops below the threshold voltage (VIT1= 2.9V), $\overline{\text{RESET}}$ is asserted. |
| SENSE2 | 3 | Monitor voltage input for Supply 2 | When the voltage at this terminal drops below the threshold voltage (VIT2= 0.4V), $\overline{\text{RESET}}$ is asserted. |
| SENSE3 | 2 | Monitor voltage input for Supply 3 | When the voltage at this terminal drops below the threshold voltage (VIT3= 0.4V), $\overline{\text{RESET}}$ is asserted. |
| SENSE4 | 1 | Monitor voltage input for Supply 4 | When the voltage at this terminal drops below the threshold voltage (VIT4= 0.4V), $\overline{\text{RESET}}$ is asserted. |
| $\overline{\text{MR}}$ | 7 | Manual reset input with internal 100k pull-up to Vcc and 50ns deglitch. Logic low level of this pin asserts $\overline{\text{RESET}}$. | |
| $\overline{\text{RESET}}$ | 6 | $\overline{\text{RESET}}$ is an open-drain output pin. When $\overline{\text{RESET}}$ is asserted, this pin remains in a low-impedance state. When $\overline{\text{RESET}}$ is released, this pin goes to a high-impedance state after 50ms. | |
| Vcc | 8 | Supply voltage. Connecting a 0.1 µF ceramic capacitor close to this pin is recommended. | |
| GND | 5 | Ground | |

# GENERAL DESCRIPTION

The TPS386596L33 multi-channel reset supervisor provides a complete single reset function for a four power supply system. The design of the SVS is based on the TPS386000 quad supervisor device series. TPS386596 is designed to assert the /RESET signal following the logic in Table 1. The $\overline{\text{RESET}}$ output remains asserted for a 50ms delay time after the event of reset release. The SENSE1 input has a fixed voltage threshold designed to monitor a 3.3V nominal supply. The trip point, $V_{IT1}$, for SENSE1 is 2.90 (TYP). Each of the remaining SENSEn inputs (n = 2,3,4) can be set to any voltage threshold above 0.4V using an external resistor divider. An active low manual reset ($\overline{\text{MR}}$) input is also provided for asserting the $\overline{\text{RESET}}$ signal as desired by the system.

## RESET OUTPUT

In a typical application of TPS386596, the $\overline{\text{RESET}}$ output is connected to the reset input of a processor (DSP, MCU, CPU, FPGA, ASIC, etc.) or connected to the enable input of voltage regulators (DC-DC, LDO, etc.).

TPS386596 provides an open drain reset output. Pull-up resistors must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. By connecting a pull-up resistor to the proper voltage rail (up to 6.5V), the $\overline{\text{RESET}}$ output can be connected to other devices at the right interface voltage level. The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the output transistor.

The $\overline{\text{RESET}}$ output is defined for VCC > 0.9V. To ensure that the target processor is properly reset, the VCC supply input should be fed by the power rail which is available as early as possible in the application.

Table 1 describes a truth table of how the $\overline{\text{RESET}}$ output is asserted or released. Figure 3 provides a timing diagram that shows how $\overline{\text{RESET}}$ is asserted and de-asserted in relation to $\overline{\text{MR}}$ and the SENSEn inputs. Once the conditions are met, the transitions from the asserted state to the release state are performed after a fixed 50ms delay time.

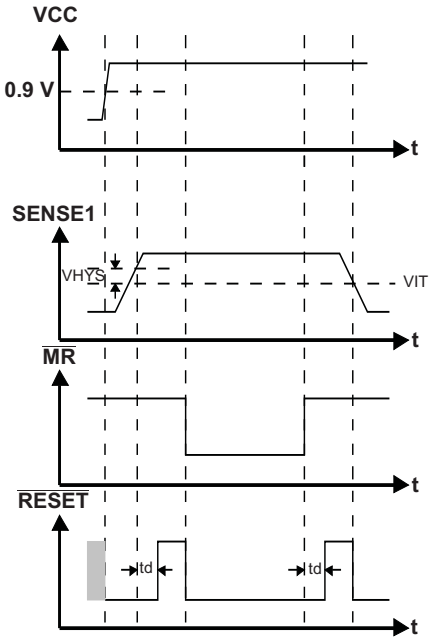



**Figure 3. Timing Diagram**

## SENSE INPUTS

The SENSEn inputs provide terminals at which the system voltages can be monitored. If the voltage at any one of the SENSEn pins drops below their respective VITn, then the $\overline{\text{RESET}}$ output is asserted. The comparators have a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$transitions. It is good analog design practice to use a 1nF to 10nF bypass capacitor at the SENSEn input to ground, to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device.

A typical connection of resistor dividers is show in Figure 4. SENSE1 is used to monitor a 3.3V nominal power supply voltage with a trip point = 2.90V, and the remaining SENSEn (n=2,3,4) inputs can be used to monitor voltage rails down to 0.4V. Threshold voltages can be calculated using the following equations.

VCC2_target = (1 + RS2H/RS2L) × 0.4 (V)
VCC3_target = (1 + RS3H/RS3L) × 0.4 (V)
VCC4_target = (1 + RS4H/RS4L) × 0.4 (V)

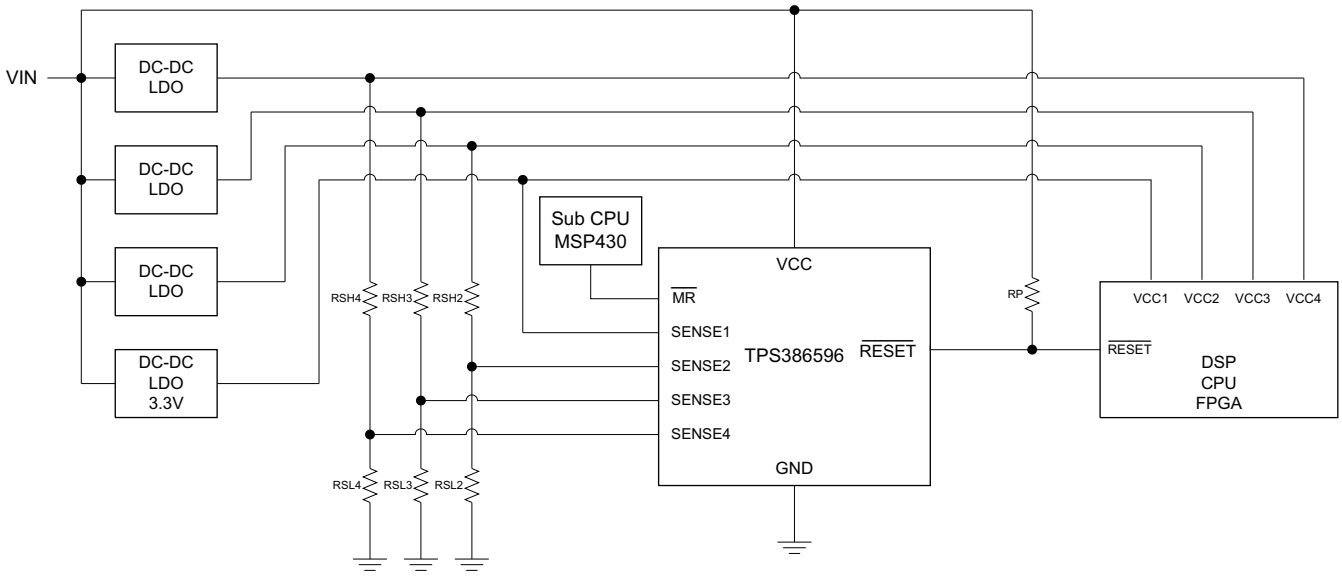



**Figure 4. Typical TPS386596L33 Application Diagram**

## MANUAL RESET

The manual reset $\overline{MR}$ input allows external logic signal from processors, other logic circuits, and/or discrete sensors to initiate a reset. The typical application of a TPS386596 has its $\overline{RESET}$ output connected to processor. A logic low at $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to a logic high and SENSEn are above their respective voltage thresholds, $\overline{RESET}$ is released after a fixed 50ms reset delay time. An internal 100kΩ pull-up to $V_{CC}$ is integrated on the $\overline{MR}$ input. There is also an internal 50ns (typical) deglitch circuit.

**Table 1. $\overline{RESET}$ Truth Table**

| CONDITION | | OUTPUT | |
|---|---|---|---|
| $\overline{MR}$ = L | SENSEn < VITn | $\overline{RESET}$ = L | Reset asserted |
| $\overline{MR}$ = L | SENSEn > VITn | $\overline{RESET}$ = L | Reset asserted |
| $\overline{MR}$ = H | SENSE1 < VIT1 OR<br>SENSE2 < VIT2 OR<br>SENSE3 < VIT3 OR<br>SENSE4 < VIT4 | $\overline{RESET}$ = L | Reset asserted |
| $\overline{MR}$ = H | SENSE1 > VIT1 AND<br>SENSE2 > VIT2 AND<br>SENSE3 > VIT3 AND<br>SENSE4 > VIT4 | $\overline{RESET}$ = H | **Reset released** |

## IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS386596 is relatively immune to short negative transients on the SENSEn pins. Sensitivity to transients is dependent on how much percentage the sense voltage drops below the threshold voltage, as shown in Figure 8. See Figure 5 for the measurement technique.

## PARAMETRIC MEASUREMENT INFORMATION

### TEST CONDITION

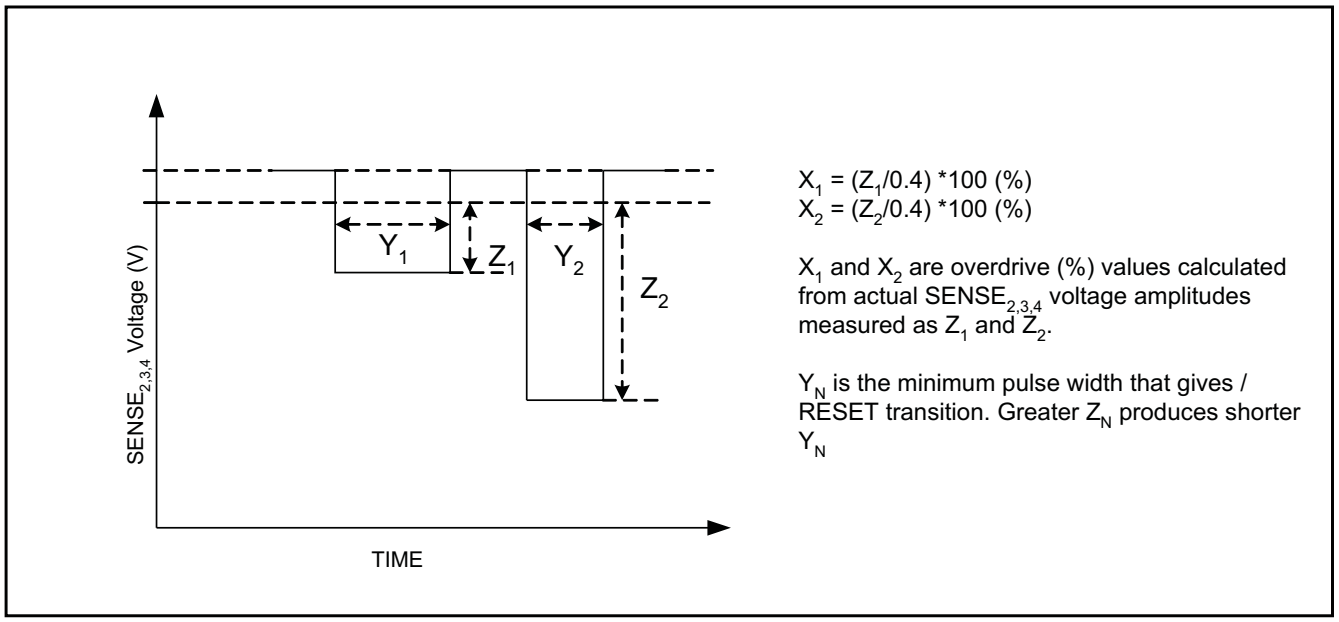



**Figure 5. Measurement Technique for Immunity to Sense Pin Voltage Transient**

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, and $V_{CC}$ = 3.3V, unless otherwise noted.

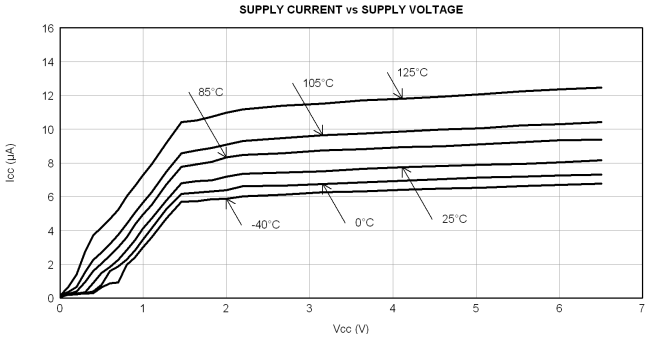



**Figure 6.**

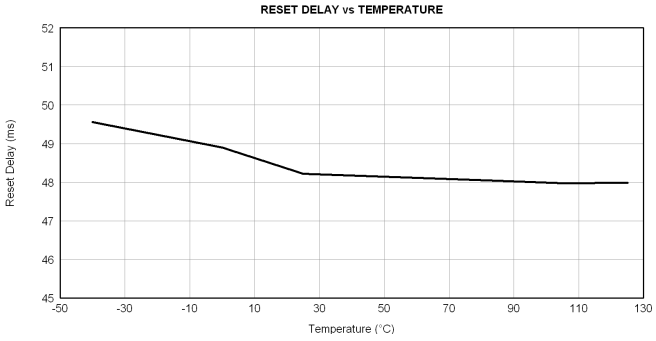



**Figure 7.**

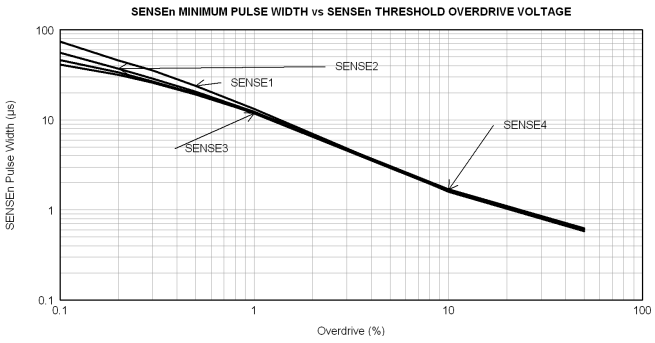



**Figure 8.**

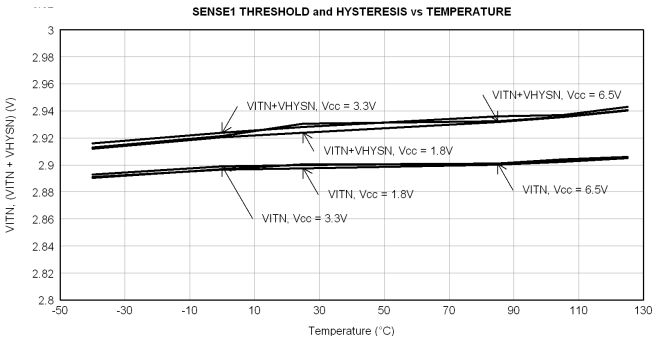



**Figure 9.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, and $V_{CC}$ = 3.3V, unless otherwise noted.

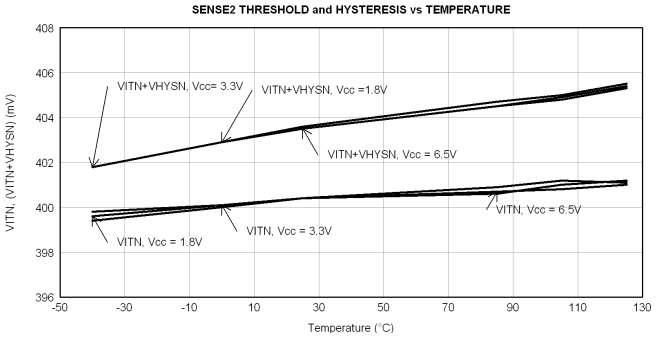



**Figure 10.**

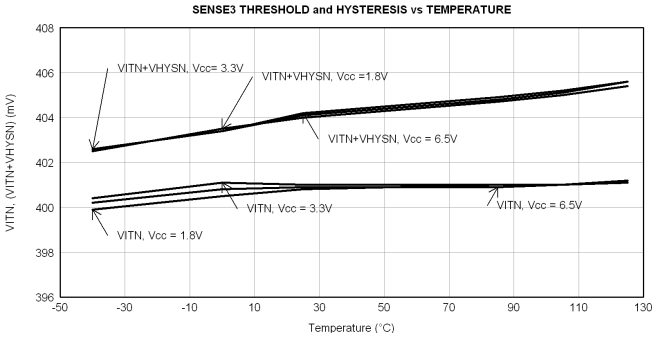



**Figure 11.**

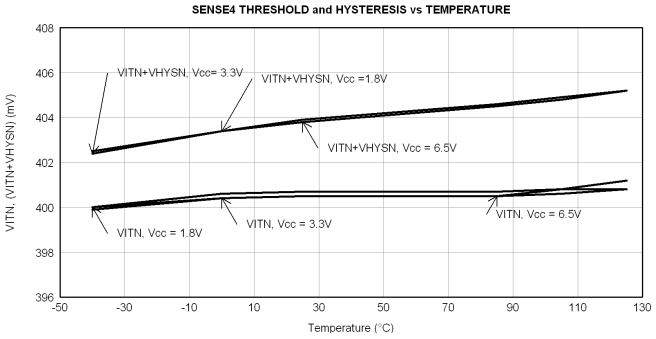



**Figure 12.**

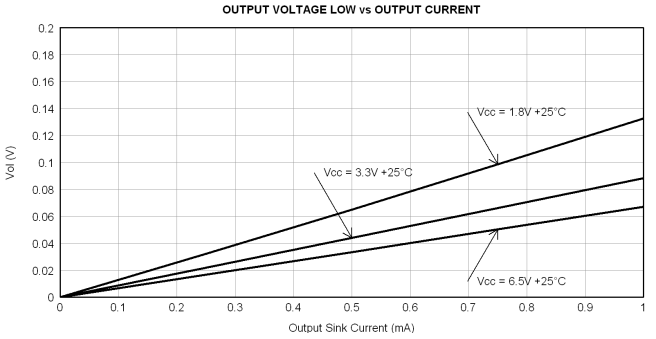



**Figure 13.**

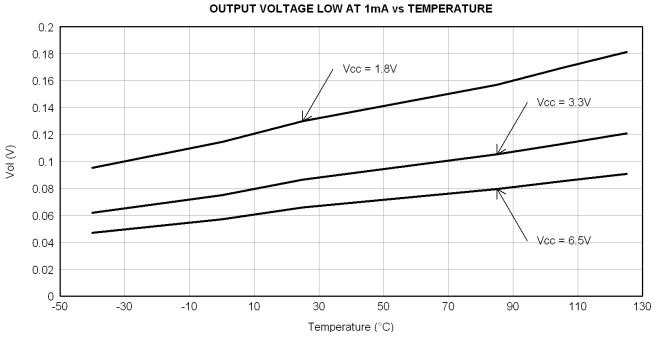



**Figure 14.**

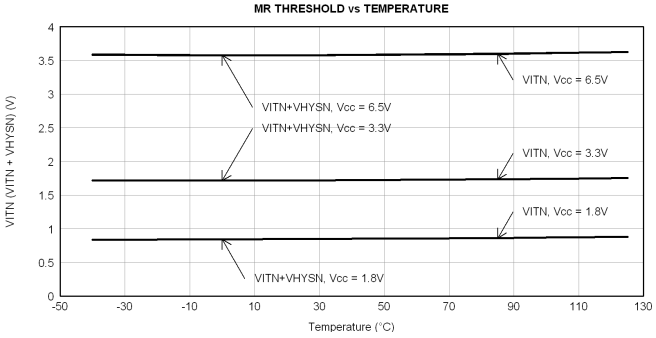



**Figure 15.**

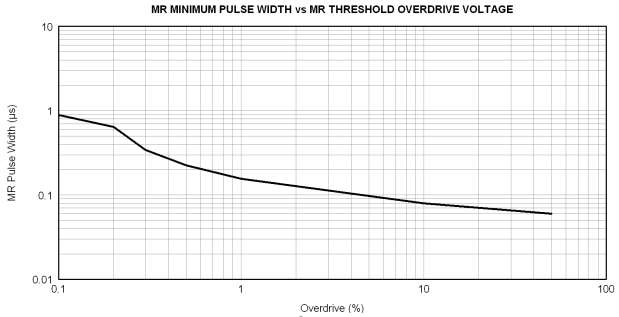



**Figure 16.**

## PACKAGING INFORMATION

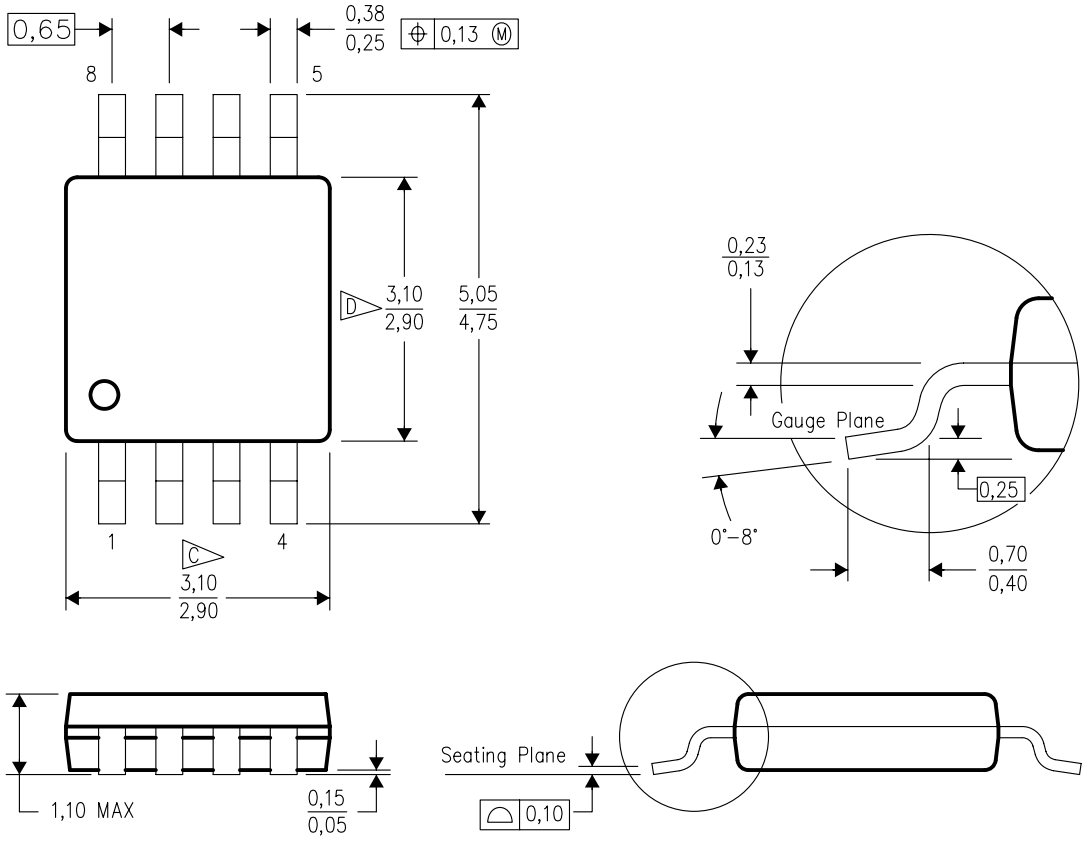
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS386596L33DGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| TPS386596L33DGKT | ACTIVE | MSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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