

GaAs Broadband Low Phase Noise Amplifier

APM-6848

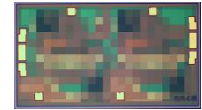
1. Device Overview

1.1 General Description

The APM-6848 is an integrated 2-stage broadband, low phase noise LO driver amplifier designed to provide a saturated +20 dBm output power from a 0-4 dBm input power with low DC power consumption. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to provide enough power to drive the LO port of an S-diode mixer from 2 GHz to 20 GHz or of an H or L diode mixer from 2 GHz to 32 GHz. This amplifier can be operated with a variety of bias conditions for both low power and high-power applications.



PA Module



Bare Die

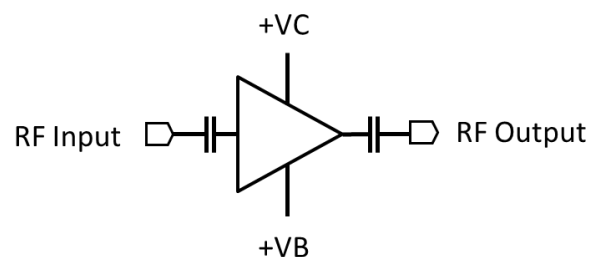
1.2 Features

- -165 dBc/Hz phase noise at 10 kHz offset frequency
- +21 dBm output power
- +23 dB gain
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable
- S-parameter files: [APM-6848CH.s2p](#)
- Integrated DC blocks – No bias-tees or off-chip blocking required

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G Transceivers
- Driver amplifier for S, H, and L – diode mixers
- Suitable as a T3 driver

1.4 Functional Block Diagram



1.5 Part Ordering Options¹

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
APM-6848CH	Wire Bondable Die	Bare Die	RoHS	Active	EAR99
APM-6848PA	Connectorized Module	PA	RoHS	Active	EAR99

¹ Refer to our [website](#) for a list of definitions for terminology presented in this table.

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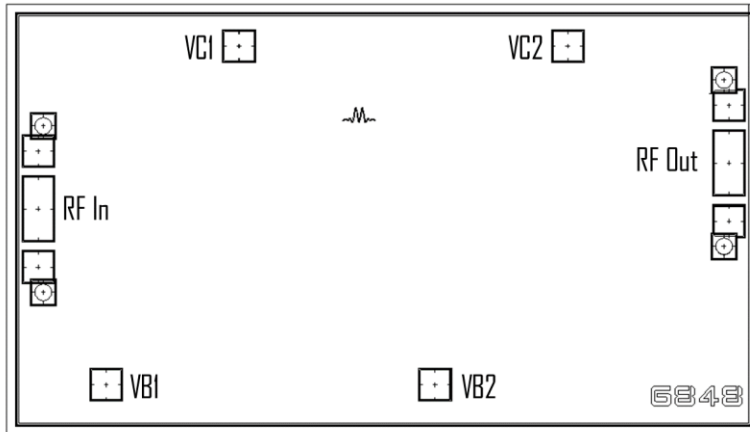
Revision History

Revision Code	Revision Date	Comment
-	October 2019	Datasheet Initial Release
A	January 2020	Revised Min. Psat/SSG Spec, Added Time Domain Plots
B	July 2020	Revised Max Operating Temperature
C	July 2020	Updated Thermal Resistance
D	October 2020	Updated Thermal Specs, Updated Min Specs
E	December 2020	Updated Performance Plots to Adhere to Max Input Power Spec

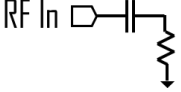
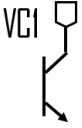

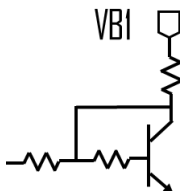
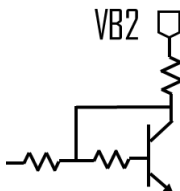
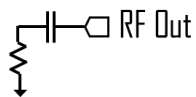

2. APM-6848 Port Configurations and Functions

2.1 APM-6848CH Port Diagram

A port diagram of the APM-6848CH is shown below.

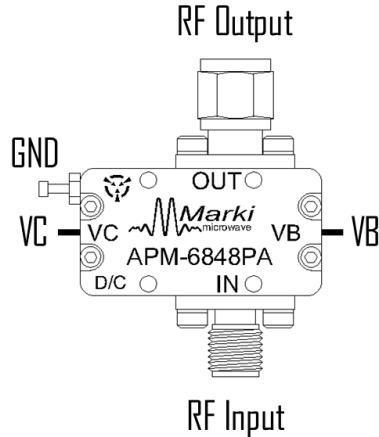


2.2 APM-6848CH Port Functions

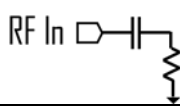
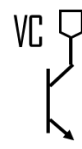
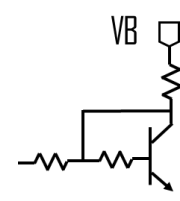
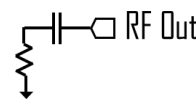

Port	Function	Description	Equivalent Circuit for Package
RF In	RF Input	This is the RF Input port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω . RF input pad is GSG with 175 μm pitch.	
VC1	Collector Supply Port 1	Pad VC1 is the DC voltage supply pad for the 1 st stage of the amplifier IC. See section 3.6 for performance at different bias conditions.	
VC2	Collector Supply Port 2	Pad VC2 is the DC voltage supply pad to the 2 nd stage of the amplifier IC. Larger VC voltage will result in larger power consumption and larger power output. See section 3.6 for performance at different bias conditions.	
VB1	Base Supply Port 1	Pad VB1 is the DC voltage supply pad for a current mirror which controls the collector current of the 1 st stage (Ic1). Larger voltages result in a higher current draw through pad VC1, effectively functioning as a gain control pin for the 1 st stage of the amplifier. See section 3.6 for performance at different bias conditions.	
VB2	Base Supply Port 2	Pad VB2 is the DC voltage supply pad for a current mirror which controls the collector current of the 2 nd stage (Ic2). Larger voltages result in a higher current draw through pad VC2, effectively functioning as a gain control pin for the 2 nd stage of the amplifier. See section 3.6 for performance at different bias conditions.	
RF Out	RF Output	This is the RF Output port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω . RF output pad is GSG with 175 μm pitch. Must have less than 7:1 VSWR when operating with voltage larger than 5V on VC1 or VC2.	
GND	Ground	Backside of the IC must be connected to a DC/RF ground with high thermal and electrical conductivity.	

2.3 APM-6848PA Port Diagram

A port diagram of the APM-6848PA is shown below.



2.4 APM-6848PA Port Functions

Port	Function	Description	Equivalent Circuit for Package
RF In	RF Input	This is the RF input port of the amplifier. It is internally DC blocked and RF matched to 50 Ω.	
VC	Collector Supply	Port VC is the DC voltage supply port for both stages of the 2-stage amplifier. The VC port in the PA module internally connects to both VC1 and VC2 of the IC described in section 2.2 of this datasheet	
VB	Base Supply	Port VB is the DC voltage supply port for current mirrors which controls the collector current supplied to the 2 amplifier stages. Larger voltages result in a higher current draw through port VC, effectively functioning as a gain control pin. The VB port in the PA module internally connects to both VB1 and VB2 of the IC described in section 2.2 of this datasheet	
RF Out	RF Output	This is the RF output port of the amplifier. It is internally DC blocked and RF matched to 50 Ω. Must have less than 7:1 VSWR when operating with voltage larger than 5V on port VC.	
GND	Ground	Housing or outside of the coaxial cables must be connected to a DC/RF ground potential with high thermal and electrical conductivity.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Collector Positive Bias Voltage (VC, VC1, VC2)	7	V
Positive Bias Current (Ic1) ²	90	mA
Positive Bias Current (Ic2) ²	90	mA
Current Mirror Positive Bias Voltage (VB, VB1, VB2)	7	V
Current Mirror Positive Bias Current (Ib, Ib1+Ib2)	8	mA
RF Input Power	+5	dBm
Output Load VSWR	7:1	-
Operating Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
Thermal Resistance, θ_{JC}	53	°C/W
Max Junction Temperature for MTTF >1E6 Hours:	125	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	APM-6848PA	14.7g

² Maximum positive DC collector current into each collector biasing pin

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications. Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max ³	Units
T _A , Ambient Temperature	-40	+25	+85	°C
Positive DC Voltage (VC1)	+3	+5	+6	V
Positive DC Current (Ic1)	8	21	40	mA
Positive DC Voltage (VC2)	+3	+5	+6	V
Positive DC Current (Ic2)	8	21	40	mA
Positive DC Current Mirror Voltage (VB1)	+3	+5	+6	V
Positive DC Current Mirror Current (Ib1)	0.9	2	2.6	mA
Positive DC Current Mirror Voltage (VB2)	+3	+5	+6	V
Positive DC Current Mirror Current (Ib2)	0.9	2	2.6	mA

3.4 Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.

Amplifier must have an output load connected when operating with a VC, VC1, or VC2 voltage larger than +5V.

³ Maximum recommended operating current conditions without RF input applied. Please see typical performance plots on page 12 for relationship between RF input power and DC current draw.

3.5 Electrical Specifications⁴

The electrical specifications apply at $T_A=+25^{\circ}\text{C}$ in a 50Ω system.

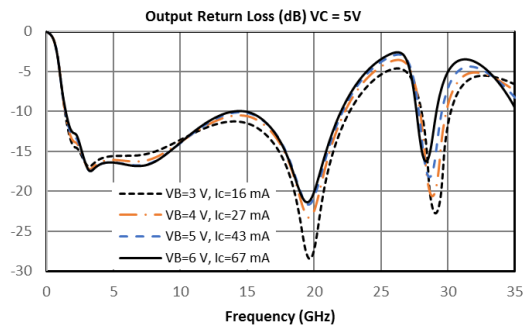
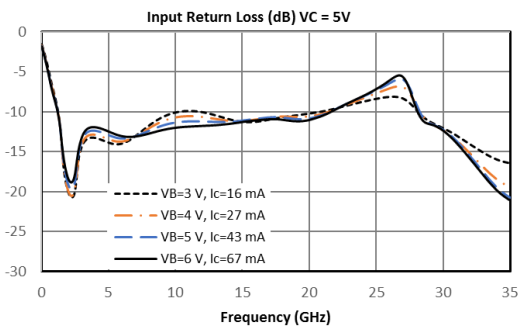
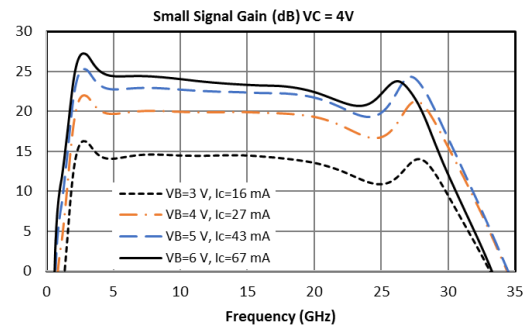
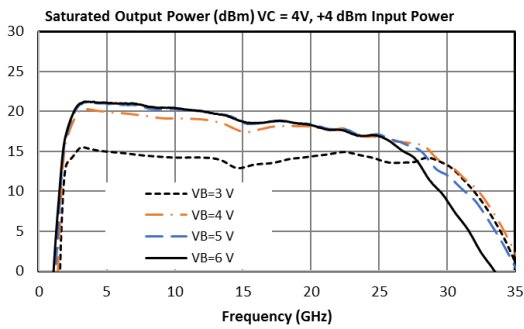
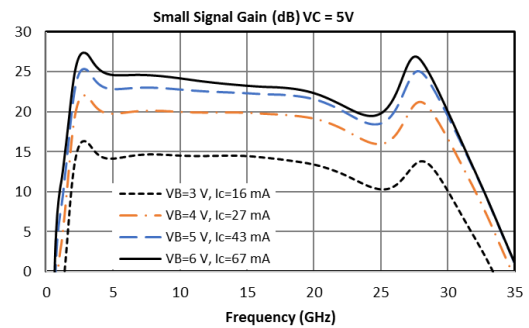
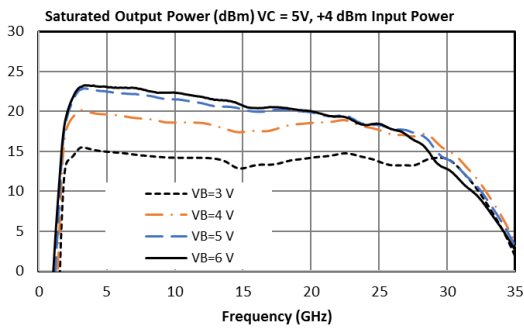
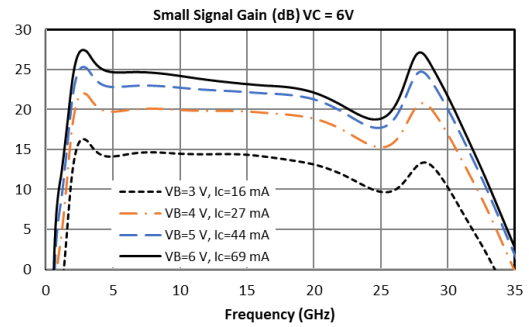
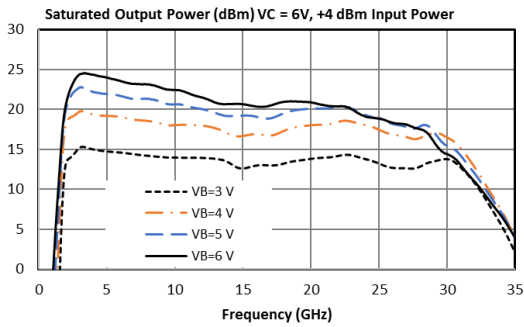
Min and Max limits apply only to our connectorized units and are guaranteed at $T_A=+25^{\circ}\text{C}$. Die are 100% DC tested and RF tested on a per lot basis

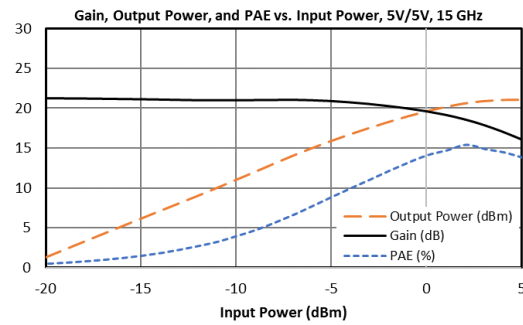
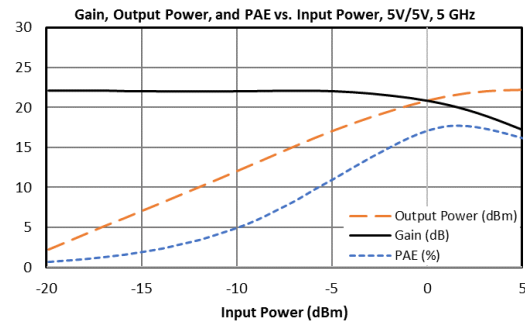
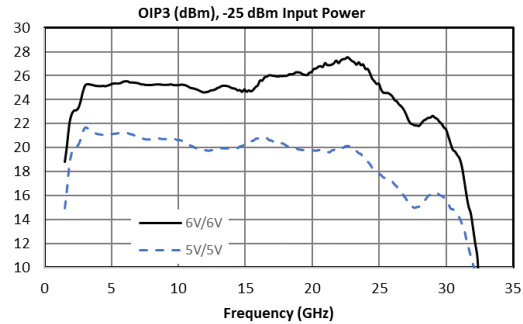
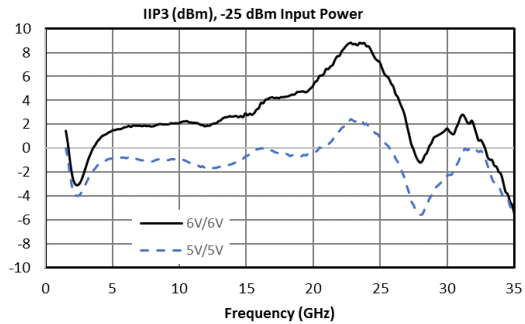
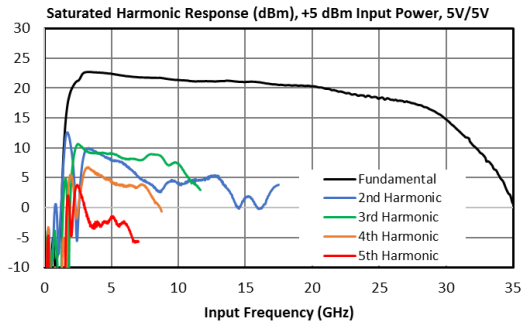
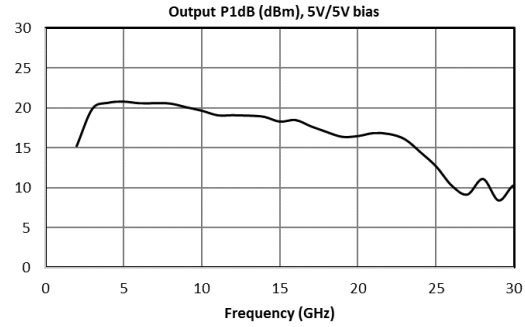
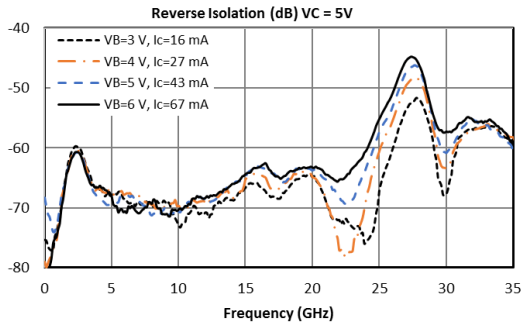
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power	5V/5V bias, +4 dBm Input Power	2 GHz – 20 GHz	+19	+21	dBm
		20 GHz – 29 GHz		+18	
Small Signal Gain	5V/5V bias, -25 dBm Input Power	2 GHz – 20 GHz	19	23	dB
		20 GHz – 29 GHz		21	
Input Return Loss		2 GHz – 20 GHz		11	
		20 GHz – 29 GHz		9	
Output Return Loss		2 GHz – 20 GHz		15	
		20 GHz – 29 GHz		7	
Noise Figure		2 GHz – 26.5 GHz		6	
Reverse Isolation	2 GHz-29 GHz		65		
Collector Current ⁵ , I_c	5V/4V	-		27	mA
	5V/5V	-		43	
	5V/6V	-		67	
Current Mirror Current, I_b	5V/4V	-		2.9	
	5V/5V	-		4	
	5V/6V	-		5.2	
Input IP3 (IIP3)	5V/5V bias, -25 dBm Input Power	2 GHz – 29 GHz		+0.5	dBm
Output IP3 (OIP3)		2 GHz – 29 GHz		+21	
Output P_{1dB}	5V/5V bias	2 GHz – 20 GHz		+19	
		20 GHz – 29 GHz		+13	
Input Power for Saturation	5V/5V bias	2 GHz – 29 GHz		+4	dBm
Phase Noise @ 10 kHz Offset	5V/5V bias, +9 dBm Input power	4 GHz		-165	dBc/Hz

⁴ All Specifications and performance shown with VC1 = VC2 and VB1 = VB2

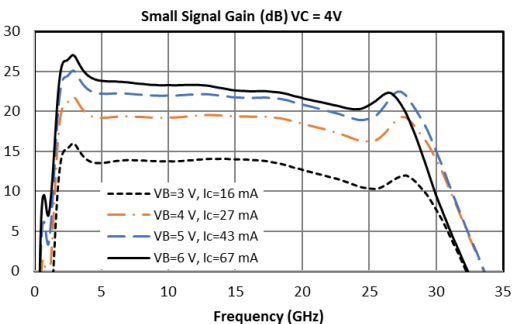
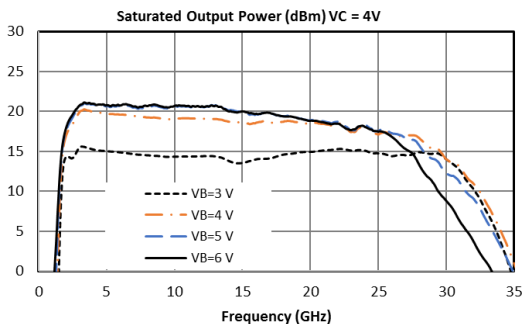
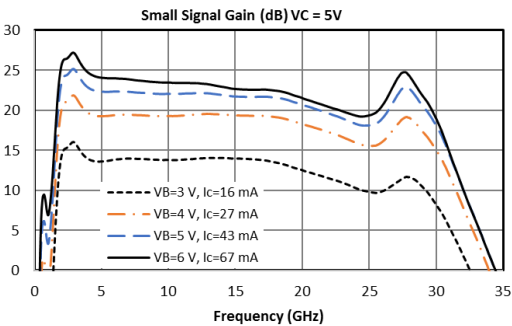
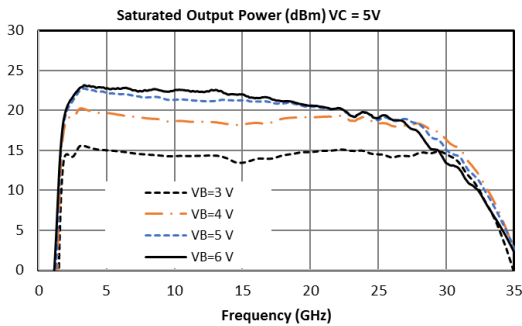
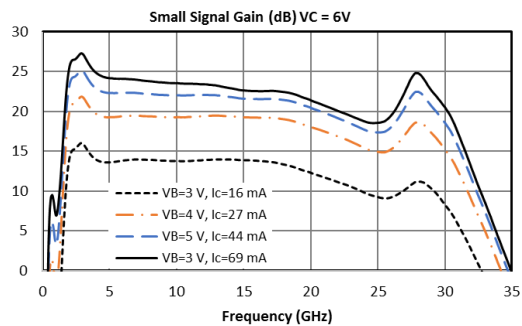
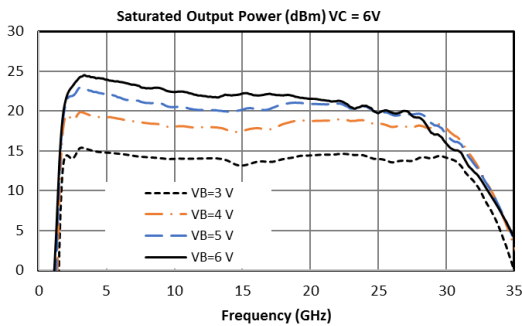
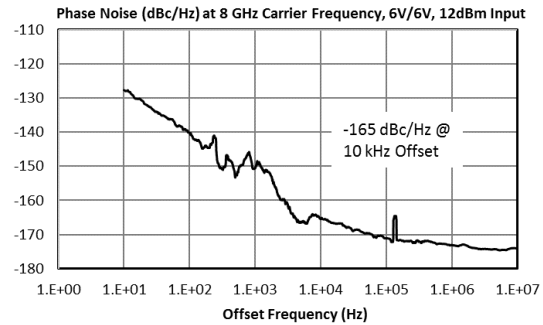
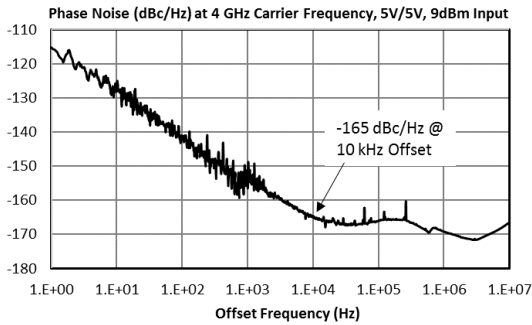
⁵ Bias conditions for I_c and I_b tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as VC/VB.

3.6 APM-6848CH Typical Performance Plots

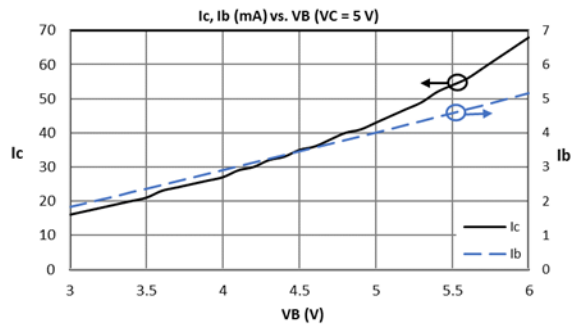
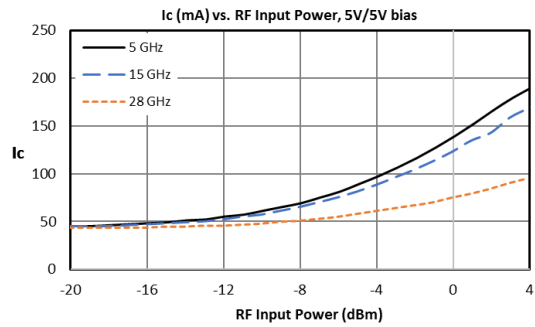
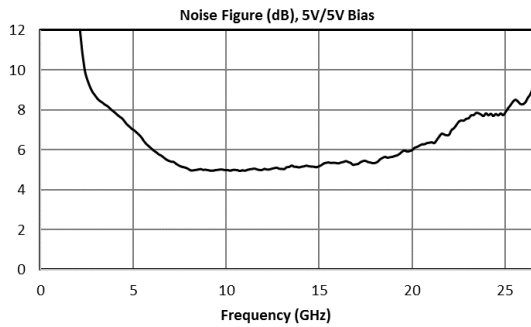
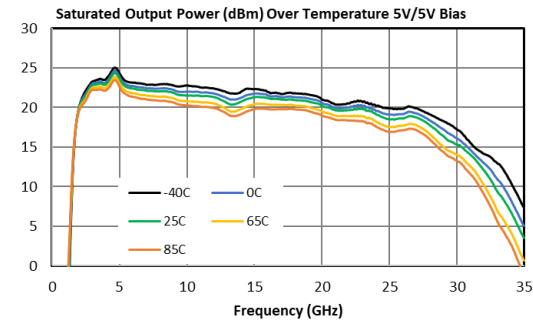
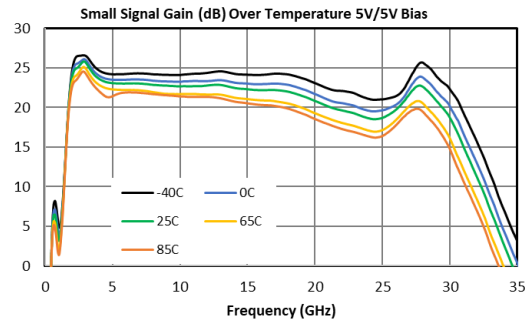
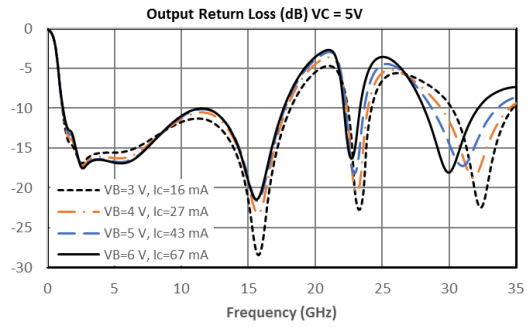
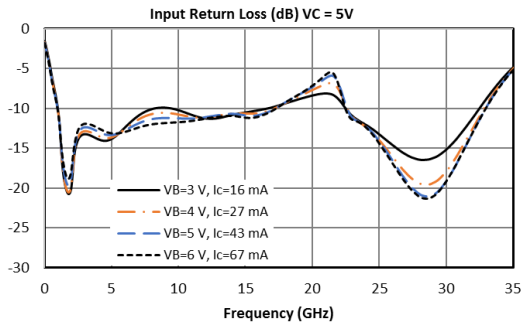




3.7 APM-6848PA Typical Performance Plots⁶

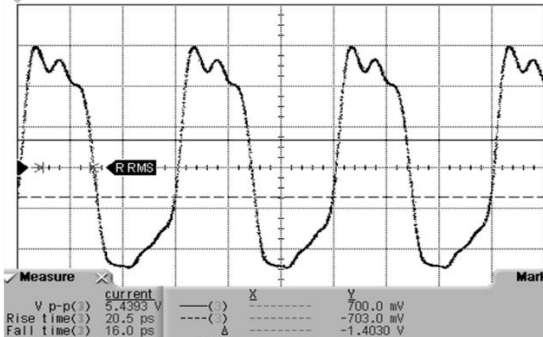


⁶ Phase Noise Plots taken above maximum recommended input power for MTF >1E6 hours. Input powers greater than +5 dBm can result in MTF <1E6 hours.

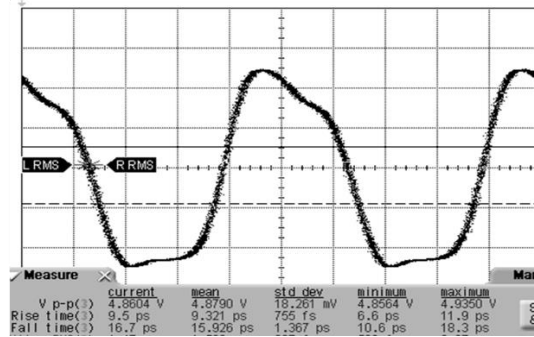


3.9 Time Domain Plots⁷

5 GHz, +5 dBm In, 5V/5V bias



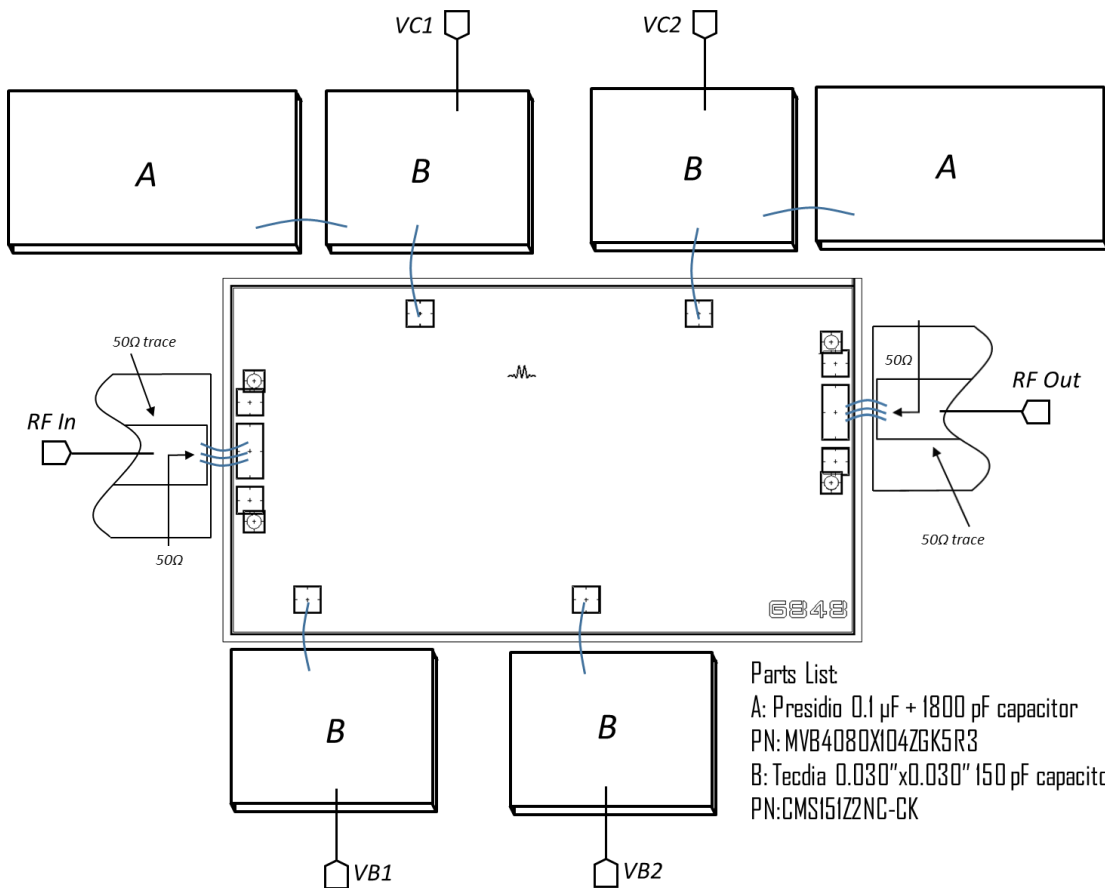
10 GHz, +5 dBm In, 5V/5V bias



4. Application Information

4.1 APM-6848CH Application Circuit

Below is the recommended application circuit for the APM-6848CH.



⁷ Fast rise time is desirable for linear T3 mixer operation.

4.2 Gain and Power Control

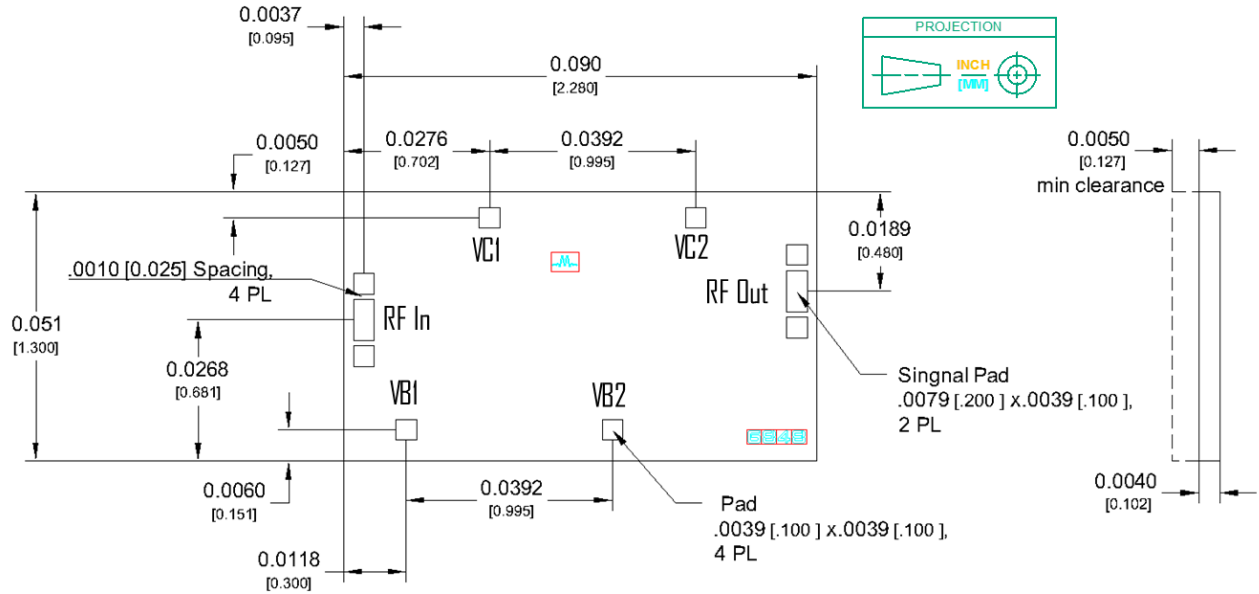
The APM-6848 is a 2-stage amplifier integrated on a single IC. In the APM-6848PA module, VB1 & VB2 and VC1 & VC2 are connected internally for user convenience. However, in the APM-6848CH bare die, the user has some freedom to operate the 2 amplifier stages independently for their application-specific needs. Please refer to section 2.2 to see the function of each pad on the APM-6848CH, and refer to the gain and Psat plots in sections 3.6 and 3.7 to see how bandwidth, saturated output power, and gain profile change for various bias conditions.

Generally, the gain of the first stage and second stage of the amplifier can be controlled by adjusting VB1 and VB2 respectively. Increasing the voltage applied to a VB pad increases the current drawn into the corresponding amplifier stage, which strongly correlates to the gain of that stage, and some difference to the output power of that stage. Increasing the voltage on a VC pad generally increases the linearity, maximum output power, and DC power consumption of the corresponding amplifier stage.

In the case where a user wants to drive the LO port of a mixer from an initial LO power of +5 dBm at 10 GHz, the user could apply 5V at all 4 DC ports and see an output power of +21.5 dBm and an overall power consumption of about 1 watt (the amplifier stages pull more DC current as the gain compresses in a high input power condition). Alternatively, the user could apply 3.5 V – 4 V to VB1 and VC1, and 6V to VB2 and VC2 and see an output power of 22.5 dBm with very little difference in the overall power consumption. For applications with a strict power budget and performance requirements, optimizing the bias conditions of the amplifier can be a useful tool for the system designer.

5. Mechanical Data

5.1 APM-6848CH Outline Drawing



5.2 APM-6848PA Package Outline Drawing

