ISO164x-Q1 Robust-EMC Bidirectional I2C Digital Isolators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - VDA320 Compliant
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Isolated Bidirectional, I^2C Compatible, Communication
  - ISO1640-Q1: Bidirectional SDA and SCL
- Supports up to 1.7 MHz Operation
- Robust isolation barrier:
  - >100-year projected lifetime at 500 V_{RMS} working voltage
  - Up to 3000 V_{RMS} isolation rating
  - Up to 5 kV surge capability
  - ±100 kV/μs typical CMTI
- Supply range: 3 V to 5.5 V (Side 1) and 2.25 V to 5.5 V (Side 2)
- Open-Drain Outputs With 3.5-mA Side 1 and 50-mA Side 2 Sink Current Capability
- Max capacitive load: 80 pF (Side 1) and 400 pF (Side 2)
- 8-SOIC (D-8) Package Options
- –40°C to +125°C Operating Temperature
- ±8 kV IEC-ESD 61000-4-2 contact discharge protection across isolation barrier
- Safety-Related Certifications (planned):
  - UL 1577 Component Recognition Program
  - DIN V VDE V 0884-11
  - IEC 60950-1, IEC62368-1, IEC 61010-1, IEC 60601-1 and GB4943.1-2011 certifications

2 Applications

- Electric and Hybrid-Electric Vehicles
- Isolated I^2C Buses
- SMBus and PMBus Interfaces
- Power Over Ethernet (PoE)
- Motor Control Systems
- Battery Management

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3 Description

The ISO1640-Q1 (ISO164x-Q1) device is a hot swappable, low-power, bidirectional isolator that is compatible with I^2C interfaces. This digital isolator supports UL 1577 isolation ratings of 3000 V_{RMS} in the 8-D package. Each isolation channel in this low emissions device has a logic input and open drain output separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. This family includes devices certified by VDE, UL, CSA, TUV and CQC. The ISO1640-Q1 has two isolated bidirectional channels for clock and data lines. ISO1640-Q1 integrates logic required to support bidirectional channels, providing a much simpler design and smaller footprint when compared to optocoupler-based solutions.

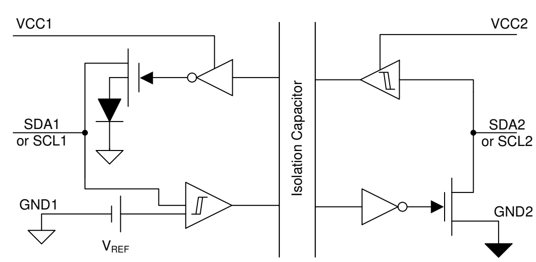
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1640-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Reinforced, Basic, and Functional Isolation Options

PART NUMBER	ISO164xBD-Q1
Protection Level	Basic
Surge Test Voltage	5000 V_{PK}
Isolation Rating	3000 V_{RMS}
Working Voltage	450 V_{RMS} / 637 V_{PK}



Simplified Isolated Bidirectional Data Channel Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2020	*	Initial release.

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5 Pin Configuration and Functions

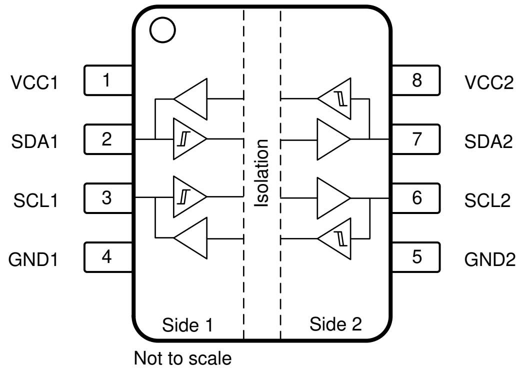

Figure 5-1. ISO1640BD-Q1 Package 8-Pin SOIC Top View

Table 5-1. Pin Functions—ISO1640BD-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground, side 1
GND2	5	—	Ground, side 2
SCL1	3	I/O	Serial clock input / output, side 1
SCL2	6	I/O	Serial clock input / output, side 2
SDA1	2	I/O	Serial data input / output, side 1
SDA2	7	I/O	Serial data input / output, side 2
VCC1	1	—	Supply voltage, side 1
VCC2	8	—	Supply voltage, side 2

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply Voltage	V_{CC1}, V_{CC2}	–0.5	6	V
Input/Output Voltage	SDA1, SCL1	–0.5	V_{CCX} + 0.5(3)	V
	SDA2, SCL2	–0.5	V_{CCX} + 0.5(3)	
Input/Output Current	SDA1, SCL1	–20	20	mA
	SDA2, SCL2	–100	100	
Temperature	Maximum junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
(3) The maximum voltage must not be greater than 6 V.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±6000	V
			Bus pins	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	V
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)		±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC1(UVLO+)}$	UVLO threshold when supply voltage is rising on Side 1		2.7	2.9	V
$V_{CC1(UVLO-)}$	UVLO threshold when supply voltage is falling on Side 1	2.3	2.6		V
$V_{CC2(UVLO+)}$	UVLO threshold when supply voltage is rising on Side 2		2	2.25	V
$V_{CC2(UVLO-)}$	UVLO threshold when supply voltage is falling on Side 2	1.7	1.8		V
$V_{HYS1(UVLO)}$	Supply voltage UVLO hysteresis, Side 1	100	150		mV
$V_{HYS2(UVLO)}$	Supply voltage UVLO hysteresis, Side 2	100	150		mV
V_{CC1}	Supply voltage, Side 1	3.0		5.5	V
V_{CC2}	Supply voltage, Side 2	2.25		5.5	V
V_{SDA1}, V_{SCL1}	Input and output signal voltages, Side 1	0		V_{CC1}	V
V_{SDA2}, V_{SCL2}	Input and output signal voltages, Side 2	0		V_{CC2}	V
V_{IL1}	Low-level input voltage, Side 1	0		480	mV
V_{IH1}	High-level input voltage, Side 1	0.7 × V_{CC1}		V_{CC1}	V
V_{IL2}	Low-level input voltage, Side 2	0		0.3 × V_{CC2}	V
V_{IH2}	High-level input voltage, Side 2	0.5 × V_{CC2}		V_{CC2}	V
I_{OL1}	I2C Output current, Side 1	0.5		3.5	mA

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		MIN	NOM	MAX	UNIT
I_{OL2}	I2C Output current, Side 2	0.5		50	mA
C1	Capacitive load, Side 1			80	pF
C2	Capacitive load, Side 2			400	pF
f_{MAX}	I2C Operating frequency[(1)]			1.7	MHz
T_A	Ambient temperature	–40	25	125	°C
T_{SD}	Thermal shutdown	141		196	°C

(1) Maximum frequency is a function of the RC time constant on the bus. If the system has less bus capacitance, then higher frequencies can be achieved.

6.4 Thermal Information

THERMAL METRIC[(1)]		ISO164x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1640						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2}$ = 5.5 V, T_J = 150°C, C1 = 20 pF, C2 = 400 pF, R1 = 1.4 kΩ, R2 = 94 Ω, Input a 1.7-MHz 50% duty-cycle clock signal			96	mW
P_{D1}	Maximum power dissipation (side-1)				43	mW
P_{D2}	Maximum power dissipation (side-2)				53	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			D	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	4	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	n/a	
DIN V VDE V 0884-11:2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	450	V_{RMS}
		DC voltage	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	5000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/A1:2019, EN 60950- 1:2006/A2:2013 and EN 62368-1:2014
Maximum transient isolation voltage, 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage 637 V_{PK} (D-8); Maximum surge isolation 5000 V_{PK} (D-8)	D-8: 400 V_{RMS} basic insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014, (pollution degree 2, material group 2)	D-8: Single protection, 3000 V_{RMS}	D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	3000 V_{RMS} (D-8) Reinforced insulation per EN 61010-1:2010/A1:2019 up to working voltage 300 V_{RMS} (D-8) 3000 V_{RMS} (D-8) Reinforced insulation per EN 60950-1:2006/A2:2013 and EN 62368-1:2014 up to working voltage of 400 V_{RMS} (D-8)
Certification planned	Certification planned	Certification planned	Certification planned	Certification planned

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D-8 PACKAGE						
I_S	Safety input, output, or supply current(1)	$R_{θJA}$ = 106.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see TBD			214	mA
		$R_{θJA}$ = 106.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see TBD			327	
P_S	Safety input, output, or total power(1)	$R_{θJA}$ = 106.3 °C/W, T_J = 150°C, T_A = 25°C			1176	mW
T_S	Safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{θJA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{θJA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{θJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDE 1						
V_{ILT1}	Voltage input threshold low (SDA1 and SCL1)		480		550	mV
V_{IHT1}	Voltage input threshold high (SDA1 and SCL1)		535		610	mV
V_{HYST1}	Voltage input hysteresis	$V_{IHT1} – V_{ILT1}$	50	60		mV
V_{OL1}	Low-level output voltage(1) (SDA1 and SCL1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	570	650	710	mV
ΔV_{OIT1}	Low-level output voltage to highlevel input voltage threshold difference, SDA1 and SCL1(2) (3)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	50			mV
SIDE 2						
V_{ILT2}	Voltage input threshold low (SDA2 and SCL2)		0.3 × V_{CC2}		0.4 × V_{CC2}	V
V_{IHT2}	Voltage input threshold high (SDA2 and SCL2)		0.4 × V_{CC2}		0.5 × V_{CC2}	V
V_{HYST2}	Voltage input hysteresis	$V_{IHT2} – V_{ILT2}$	0.05 × V_{CC2}			V
V_{OL2}	Low-level output voltage (SDA2 and SCL2)	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 50 mA			0.4	V
BOTH SIDES						
$\|I_I\|$	Input leakage currents (SDA1, SCL1, SDA2, and SCL2)	V_{SDA1}, V_{SCL1} = V_{CC1}, V_{SDA2}, V_{SCL2} = V_{CC2}		0.01	10	µA
C_I	Input capacitance to local ground (SDA1, SCL1, SDA2, and SCL2)	V_I = 0.4 × sin(2e6*πt) + V_{DD}x / 2		10		pF
CMTI	Common-mode transient immunity	V_{CM} = 1000 V, see Common-Mode Transient Immunity Test Circuit	50	75		kV/µs

(1) This parameter does not apply to the SCL1 line of the ISO1641 device because it is unidirectional.

(2) $\Delta V_{OIT1} = V_{OL1} – V_{IHT1}$. This value represents the minimum difference between a threshold for the low-level output voltage and a threshold for the high-level input voltage to prevent a permanent latch condition that would otherwise occur with bidirectional communication.

(3) Any supply voltages on either side that are less than the minimum value make sure that the device does a lockout. Both supply voltages that are greater than the maximum value keep the device from a lockout.

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6.10 Supply Current Characteristics

over recommended operating conditions, unless otherwise noted. See Test Diagram for more information.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.25 V ≤ V_{CC2} ≤ 2.75 V							
I_{CC2}	Supply current, Side 2	ISO1640	V_{SDA1}, V_{SCL1} = GND1, V_{SDA2}, V_{SCL2} = GND2, R1 and R2 = Open, C1 and C2 = Open		4.9	6.6	mA
			V_{SDA1}, V_{SCL1} = VCC1, V_{SDA2}, V_{SCL2} = VCC2, R1 and R2 = Open, C1 and C2 = Open		2.7	3.5	mA
3 V ≤ V_{CC1}, V_{CC2} ≤ 3.6 V							
I_{CC1}	Supply current, Side 1	ISO1640	V_{SDA1}, V_{SCL1} = GND1, V_{SDA2}, V_{SCL2} = GND2, R1 and R2 = Open, C1 and C2 = Open		5.2	7.1	mA
			V_{SDA1}, V_{SCL1} = VCC1, V_{SDA2}, V_{SCL2} = VCC2, R1 and R2 = Open, C1 and C2 = Open		3	4	mA
I_{CC2}	Supply current, Side 2	ISO1640	V_{SDA1}, V_{SCL1} = GND1, V_{SDA2}, V_{SCL2} = GND2, R1 and R2 = Open, C1 and C2 = Open		4.9	6.7	mA
			V_{SDA1}, V_{SCL1} = VCC1, V_{SDA2}, V_{SCL2} = VCC2, R1 and R2 = Open, C1 and C2 = Open		2.8	3.5	mA
4.5 V ≤ V_{CC1}, V_{CC2} ≤ 5.5 V							
I_{CC1}	Supply current, Side 1	ISO1640	V_{SDA1}, V_{SCL1} = GND1, V_{SDA2}, V_{SCL2} = GND2, R1,R2 = Open, C1,C2 = Open		5.3	7.2	mA
			V_{SDA1}, V_{SCL1} = VCC1, V_{SDA2}, V_{SCL2} = VCC2, R1 and R2 = Open, C1 and C2 = Open		3	4.1	mA
I_{CC2}	Supply current, Side 2	ISO1640	V_{SDA1}, V_{SCL1} = GND1, V_{SDA2}, V_{SCL2} = GND2, R1 and R2 = Open, C1 and C2 = Open		5	6.8	mA
			V_{SDA1}, V_{SCL1} = VCC1, V_{SDA2}, V_{SCL2} = VCC2, R1 and R2 = Open, C1 and C2 = Open		2.8	3.6	mA

6.11 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{UVLO}	Time to recover from UVLO	VCC1 > $V_{CC1(UVLO+)}$ or VCC2 > $V_{CC2(UVLO+)}$, I2C bus Idle. see t_{UVLO} Test Circuit and Timing Diagrams	36	95	151	µs

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6.12 Switching Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.25 V ≤ V_{CC2} ≤ 2.75 V, 3 V ≤ V_{CC1} ≤ 3.6 V						
t_{f2}	Output signal fall time (SDA2 and SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 72 Ω, C2 = 400 pF, see Test Diagram	16	26.5	40	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400 mV, R2 = 72Ω, C2 = 400 pF, see Test Diagram	38	53.3	78	
$t_{pLH1\text{-}2}$	Low-to-high propagation delay, side 1 to side 2	V_I = 535 mV, V_O = 0.7 × V_{CC2}, R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V, see Test Diagram		20	30	ns
$t_{pHL1\text{-}2}$	High-to-low propagation delay, side 1 to side 2	V_I = 550 mV, V_O = 0.3 × V_{CC2}, R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V, see Test Diagram		80	130	ns
$t_{pLH2\text{-}1}$	Low-to-high propagation delay, side 2 to side 1[(1)]	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V, see Test Diagram		40	48	ns
$t_{pHL2\text{-}1}$	High-to-low propagation delay, side 2 to side 1[(1)]	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V, see Test Diagram		70	100	ns
$PWD_{1\text{-}2}$	Pulse width distortion $\lvert t_{pHL1\text{-}2} - t_{pLH1\text{-}2}\rvert$	R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V see Test Diagram		60	104	ns
$PWD_{2\text{-}1}$	Pulse width distortion[(1)] $\lvert t_{pHL2\text{-}1} - t_{pLH2\text{-}1}\rvert$	R1 = 953 Ω, R2 = 72 Ω, C1 and C2 = 10 pF, V_{CC1} = 3.3 V see Test Diagram		25	55	ns
t_{LOOP1}	Round-trip propagation delay on side 1[(1)]	0.4 V ≤ V_I ≤ 0.3 × V_{CC1}, R1 = 953 Ω, C1 = 40 pF, R2 = 72 Ω, C2 = 400 pF, see Test Diagram		62	74	ns
3 V ≤ V_{CC1}, V_{CC2} ≤ 3.6 V						
t_{f1}	Output signal fall time (SDA1 and SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 953 Ω, C1 = 40 pF, R2 = 95.3 Ω, C2 = 400 pF, see Test Diagram	8	17	29	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900 mV, R1 = 953 Ω, C1 = 40 pF, see Test Diagram	15	25	48	
t_{f2}	Output signal fall time (SDA2 and SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 95.3 Ω, C2 = 400 pF, see Test Diagram	14	23	47	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400 mV, R2 = 95.3 Ω, C2 = 400 pF, see Test Diagram	30	50	100	
$t_{pLH1\text{-}2}$	Low-to-high propagation delay, side 1 to side 2	V_I = 535 mV, V_O = 0.7 × V_{CC2}, R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		21	29	ns
$t_{pHL1\text{-}2}$	High-to-low propagation delay, side 1 to side 2	V_I = 550 mV, V_O = 0.3 × V_{CC2}, R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		59	88	ns
$t_{pLH2\text{-}1}$	Low-to-high propagation delay, side 2 to side 1[(1)]	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		40	47	ns
$t_{pHL2\text{-}1}$	High-to-low propagation delay, side 2 to side 1[(1)]	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		70	100	ns
$PWD_{1\text{-}2}$	Pulse width distortion $\lvert t_{pHL1\text{-}2} - t_{pLH1\text{-}2}\rvert$	R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		39	61	ns
$PWD_{2\text{-}1}$	Pulse width distortion[(1)] $\lvert t_{pHL2\text{-}1} - t_{pLH2\text{-}1}\rvert$	R1 = 953 Ω, R2 = 95.3 Ω, C1 and C2 = 10 pF, see Test Diagram		25	48	ns
t_{LOOP1}	Round-trip propagation delay on side 1[(1)]	0.4 V ≤ V_I ≤ 0.3 × V_{CC1}, R1 = 953 Ω, C1 = 40 pF, R2 = 95.3 Ω, C2 = 400 pF, see Test Diagram		65	78	ns

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over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.5 V ≤ V_{CC1}, V_{CC2} ≤ 5.5 V						
t_{f1}	Output signal fall time (SDA1 and SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 1430 Ω, C1 = 40 pF, R2 = 95.3 Ω, C2 = 400 pF, see Test Diagram	6	16	22	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900 mV, R1 = 1430 Ω, C1 = 40 pF, see Test Diagram	13	32	48	
t_{f2}	Output signal fall time (SDA2 and SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 143 Ω, C2 = 400 pF, see Test Diagram	10	24	30	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400 mV, R2 = 143 Ω, C2 = 400 pF, see Test Diagram	28	48	76	
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	V_I = 535 mV, V_O = 0.7 × V_{CC2}, R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		21	28	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	V_I = 550 mV, V_O = 0.3 × V_{CC2}, R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		51	70	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1(1)	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		51	57	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1(1)	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		60	88	ns
PWD_{1-2}	Pulse width distortion $\|t_{pHL1-2} – t_{pLH1-2}\|$	R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		30	45	ns
PWD_{2-1}	Pulse width distortion(1) $\|t_{pHL2-1} – t_{pLH2-1}\|$	R1 = 1430 Ω, R2 = 143 Ω, C1 and C2 = 10 pF, see Test Diagram		10	34	ns
t_{LOOP1}	Round-trip propagation delay on side 1(1)	0.4 V ≤ V_I ≤ 0.3 × V_{CCI}, R1 = 1430 Ω, C1 = 40 pF, R2 = 143 Ω, C2 = 400 pF, see Test Diagram		84	96	ns

(1) This parameter does not apply to the SCL1 line of the ISO1641 device because it is unidirectional.

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7 Parameter Measurement Information

7.1 Parameter Measurement Information

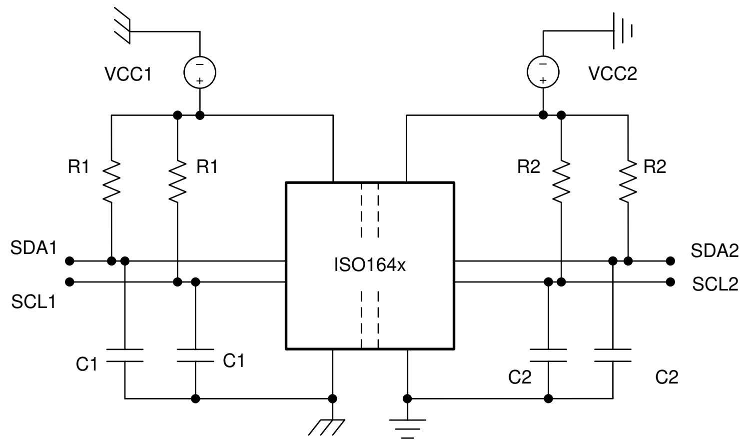

Figure 7-1. Test Diagram

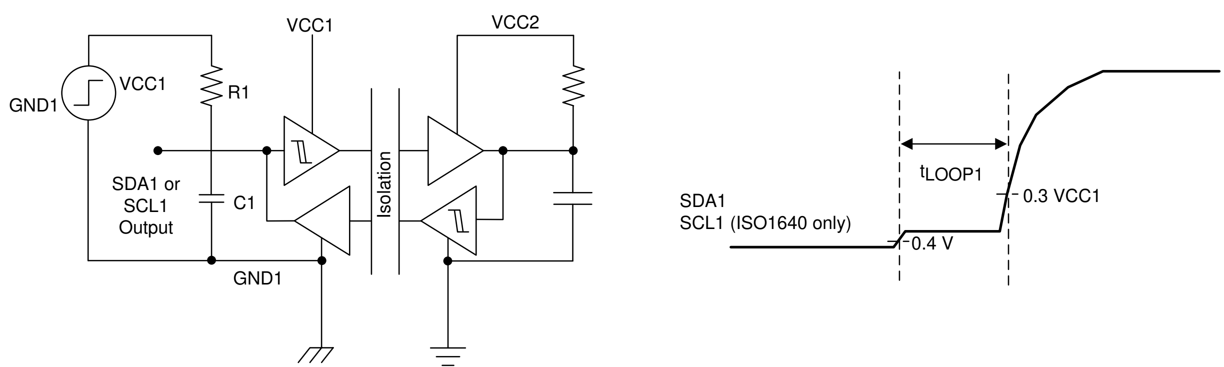

Figure 7-2. t_{Loop1} Setup and Timing Diagram

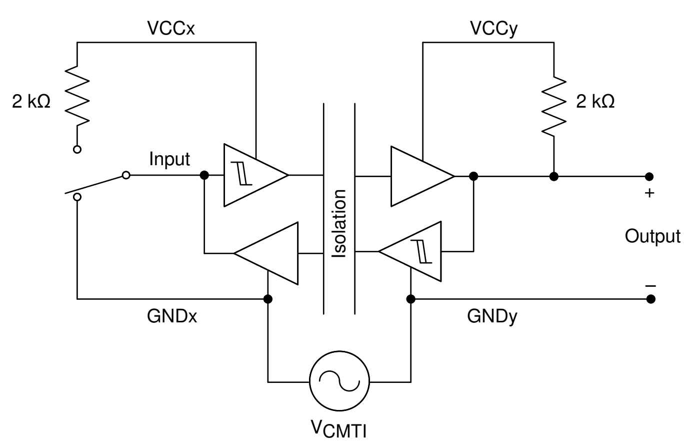

Figure 7-3. Common-Mode Transient Immunity Test Circuit

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Side x, Side y	VCCx,VCCy	Ry
1, 2	3.3 V, 3.3 V	95.3 Ω
2, 1	3.3 V, 3.3 V	953 Ω

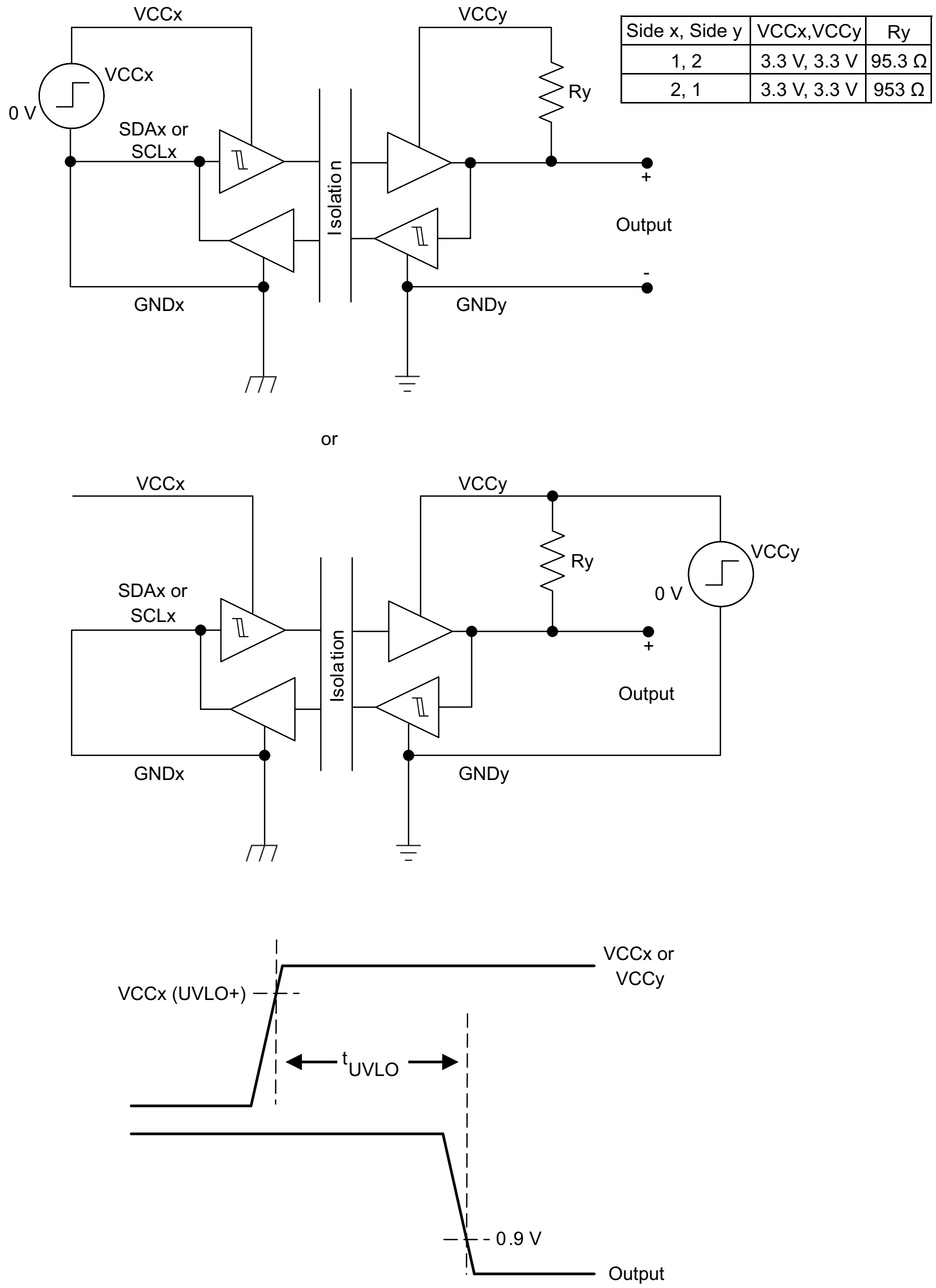

Figure 7-4. t_{UVLO} Test Circuit and Timing Diagrams

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8 Detailed Description

8.1 Overview

The I^{2}C bus consists of a two-wire communication bus that supports bidirectional data transfer between a master device and several slave devices. The master, or processor, controls the bus, specifically the serial clock (SCL) line. Data is transferred between the master and slave through a serial data (SDA) line. This data can be transferred in four speeds: standard mode (0 to 100 kbps), fast mode (0 to 400 kbps), fast-mode plus (0 to 1 Mbps), and high-speed mode (0 to 3.4 Mbps).

The I^{2}C bus operates in bidirectional, half-duplex mode, using open collector outputs to allow for multiple devices to share the bus. When a specific device is ready to communicate on the bus, it can take control pulling the lines low accordingly in order to transmit data. A standard digital isolator or optocoupler is designed to transfer data in a single direction. In order to support an I^{2}C bus, external circuitry is required to separates the bidirectional bus into two unidirectional signal paths. The ISO164x-Q1 devices internally handles the separation and partitioning of the transmit and receive signals, integrating the external circuitry needed and provide the open collector signals. They provide high electromagnetic immunity and low emissions at low power consumption. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

8.2 Functional Block Diagrams

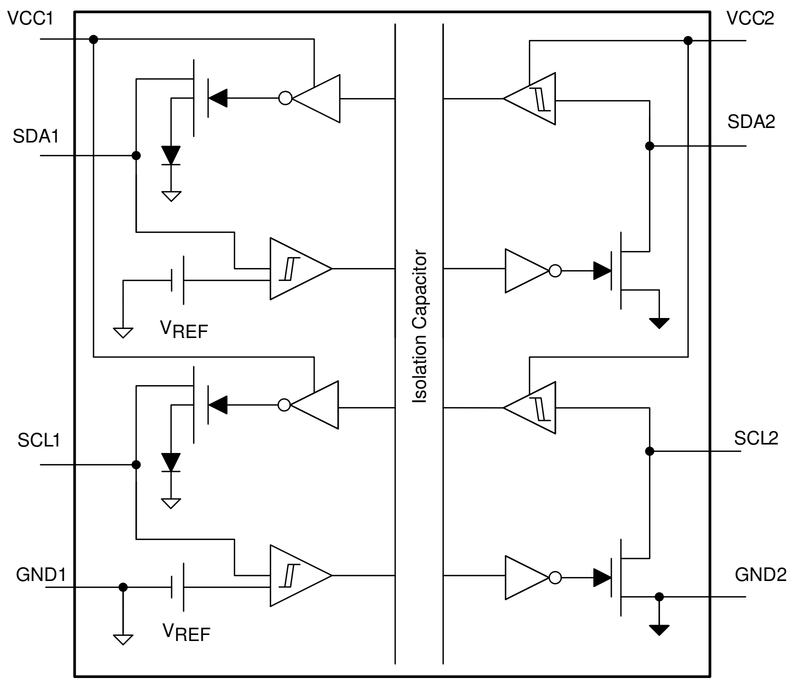

Figure 8-1. ISO1640-Q1 Block Diagram

8.3 Feature Description

The device enables a complete isolated I^{2}C interface to be implemented within a small form factor having the features listed in Table 8-1.

Table 8-1. Features List

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION(1)	MAXIMUM FREQUENCY
ISO1640-Q1	Bidirectional (SCL) Bidirectional (SDA)	3000 V_{RMS} 4242 V_{PK}	1.7 MHz

(1) See for detailed Isolation specifications.

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8.3.1 Hot Swap

The ISO164x-Q1 includes Hot Swap circuitry on Side 2 of the isolator to prevent loading on the I2C bus lines while VCCx is either unpowered or in the process of being powered on. While VCCx is below the UVLO threshold, the ISO164x-Q1 bus lines will not load the bus to avoid disrupting or corrupting an active I2C bus. If the isolator is plugged into a live backplane using a staggered connector, where VCC2 and GND2 make connection first followed by the bus lines, the SDA and SCL lines are pre-charged to VCC2 / 2 to minimize the current required to charge the parasitic capacitance of the device. Once the device is fully powered on, the device bus pins become active providing bidirectional, isolated, SCL and SDA lines.

8.4 Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1640-Q1 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated through a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I^2C. Side 1 of the ISO1640-Q1 connects to a low-capacitance I^2C node (up to 80 pF), while side 2 is designed for connecting to a fully loaded I^2C bus with up to 400 pF of capacitance.

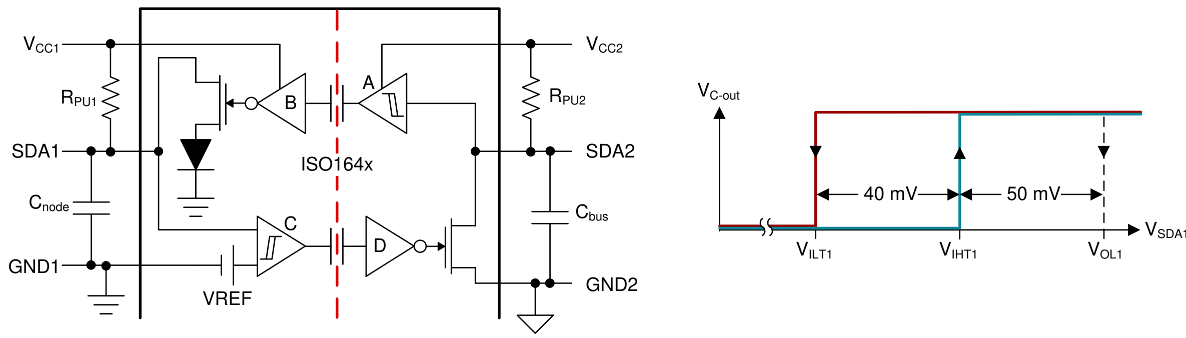

Figure 8-2. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.65 V, and the input buffer (C) that consists of a comparator with defined hysteresis. The comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V (maximum) driven directly by SDA1 and the buffered output low-level of B.

Figure 8-3 demonstrate the switching behavior of the I^2C isolator, ISO164x-Q1, between a master node at SDA1 and a heavy loaded bus at SDA2.

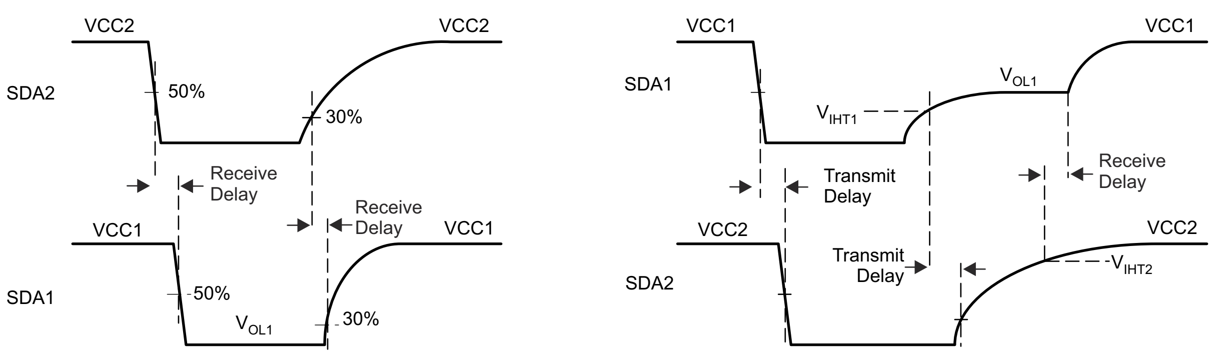

Figure 8-3. SDA Channel Timing in Receive and Transmit Directions

8.4.1 Receive Direction (Left Diagram of Figure 8-3)

When the I^2C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. The output low is the buffered output of V_{OL1} = 0.65 V, which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of V_{IL} = 0.9 V at 3 V supply levels.

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When SDA2 is released, its voltage potential increases towards VCC2 following the time-constant formed by R_{PU2} and C_{bus}. After the receive delay, SDA1 is released and also rises towards VCC1, following the time-constant $R_{PU1} \times C_{node}$. Because of the significant lower time-constant, SDA1 may reach VCC1 before SDA2 reaches VCC2 potential.

8.4.2 Transmit Direction (Right Diagram of Figure 8-3)

When a master drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.65 V level. This level cannot be observed immediately as it is overwritten by the lower low-level of the master.

However, when the master releases SDA1, the voltage potential increases and first must pass the upper input threshold of the comparator, V_{IHT1}, to release SDA2. SDA1 then increases further until it reaches the buffered output level of V_{OL1} = 0.65 V, maintained by the receive path. When comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move toward VCC1 potential.

8.5 Device Functional Modes

Table 8-2 lists the ISO164x-Q1 functional modes.

Table 8-2. Function Table (1)

POWER STATE	INPUT	OUTPUT
VCC1 < 2.3 V or VCC2 < 1.7 V	X	Z
VCC1 > 2.9 V and VCC2 > 2.25 V	L	L
VCC1 > 2.9 V and VCC2 > 2.25 V	H	Z
VCC1 > 2.9 V and VCC2 > 2.25 V	Z(2)	Undetermined

(1) H = High Level; L = Low Level; Z = High Impedance or Float; X = Irrelevant
(2) Invalid input condition as an I^2C system requires that a pullup resistor to VCC is connected.

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Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 I²C Bus Overview

The inter-integrated circuit (I²C) bus is a single-ended, multi-master, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I²C uses open-drain technology, requiring two lines, serial data (SDA) and serial clock (SCL), to be connected to VDD by resistors (see Figure 9-1). Pulling the line to ground is considered a logic zero while letting the line float is a logic one. This logic is used as a channel access method. Transitions of logic states must occur while the SCL pin is low. Transitions while the SCL pin is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are allowed.

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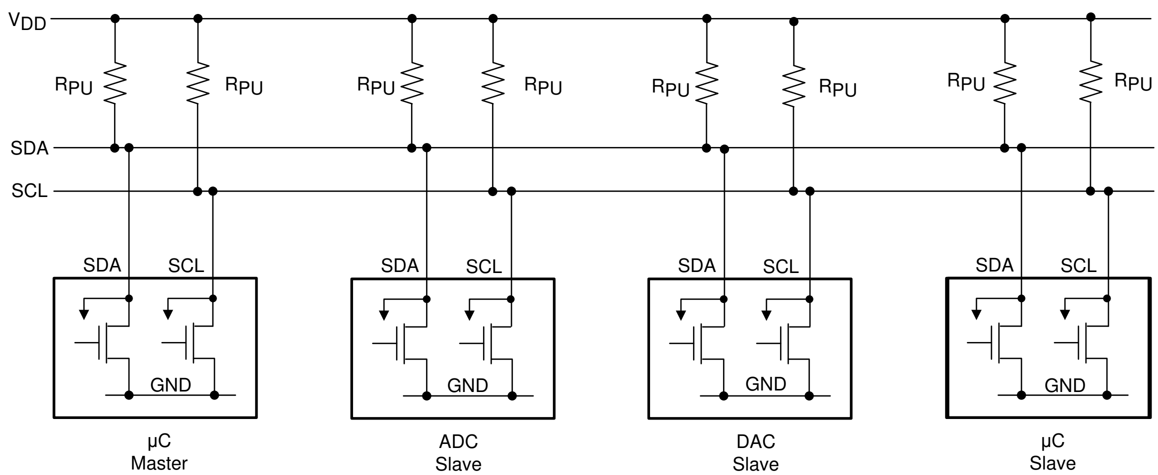

Figure 9-1. I²C Bus

I²C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO164x-Q1 devices are 100 kbps (standard mode), 400 kbps (fast mode), 1.7 Mbps (fast mode plus).

The bus has two roles for nodes: master and slave. A master node issues the clock and slave addresses, and also initiates and ends data transactions. A slave node receives the clock and addresses and responds to requests from the master. Figure 9-2 shows a typical data transfer between master and slave.

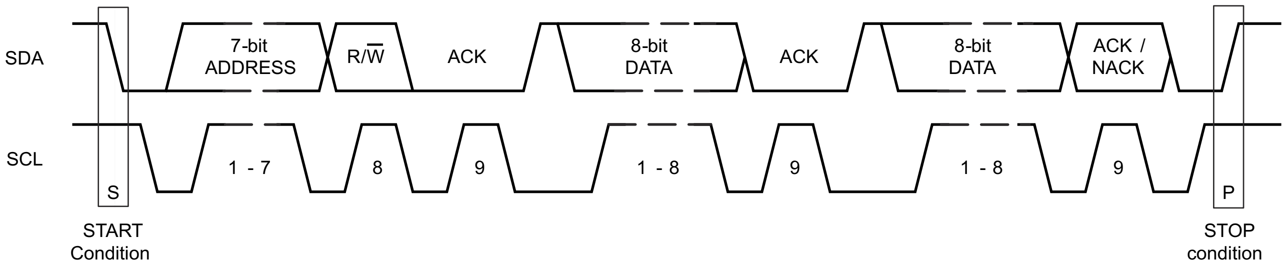

Figure 9-2. Timing Diagram of a Complete Data Transfer

The master initiates a transaction by creating a START condition, following by the 7-bit address of the slave it wishes to communicate with. This is followed by a single read and write (R/W) bit, representing whether the master wishes to write to 0, or to read from 1 the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge bit (ACK) by pulling the SDA pin low during the entire high time of the 9th clock pulse on the SCL signal, after which the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte with the slave sending an ACK bit. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave, while acknowledging (ACK) the receipt of every byte but the last one (see Figure 9-3). In this situation, the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

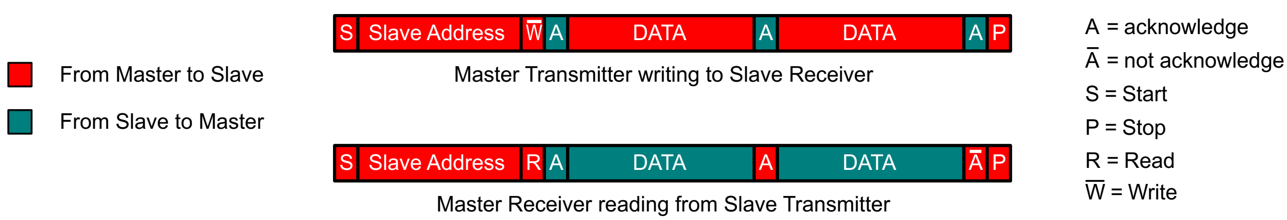

Figure 9-3. Transmit or Receive Mode Changes During a Data Transfer

When writing to a slave, a master mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note

The master ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the slave state machine and allows the master to send the STOP command.

9.2 Typical Application

Figure 9-4 shows isolated I^{2}C data acquisition system built with TI microcontroller, analog-to-digital converter, and I^{2}C isolator, ISO1641-Q1.

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The entire circuit operates from a single 3.3-V supply. A low-power push-pull converter, SN6501-Q1, drives a center-tapped transformer with an output that is rectified and linearly regulated to provide a stable 5-V supply for the data converter.

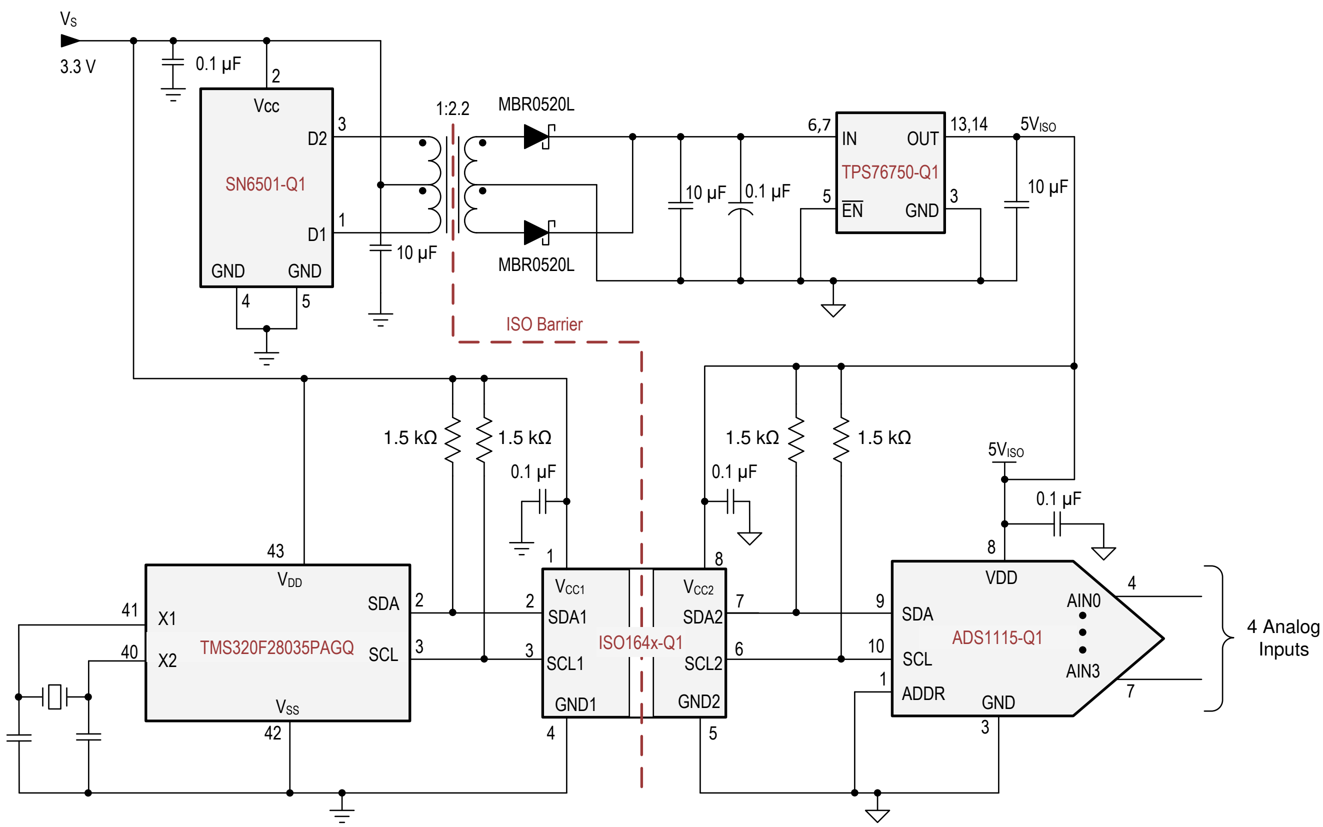

Figure 9-4. Isolated I²C Data Acquisition System

9.2.1 Design Requirements

The recommended power supply voltages must be from 3 V to 5.5 V for VCC1 and 2.25 V to 5.5 V for VCC2. A recommended decoupling capacitor with a value of 0.1 µF is required between both the VCC1 and GND1 pins, and the VCC2 and GND2 pins to support of power supply voltages transient and to ensure reliable operation at all data rates.

9.2.2 Detailed Design Procedure

Although the ISO1640-Q1 features bidirectional data channels, the device performs optimally when side 1 (SDA1 and SCL1) is connected to a single controller or node of an I2C network while side 2 (SDA2 and SCL2) is connected to the I2C bus.

The power-supply capacitor with a value of 0.1-µF must be placed as close to the power supply pins as possible. The recommended placement of the capacitors must be 2-mm maximum from input and output power supply pins (VCC1 and VCC2).

The maximum load permissible on the input lines, SDA1 and SCL1, is ≤ 80 pF and on the output lines, SDA2 and SCL2, is ≤ 400 pF.

The minimum pullup resistors on the input lines, SDA1 and SCL1 to VCC1 must be selected in such a way that input current drawn is ≤ 3.5 mA. The minimum pullup resistors on the input lines, SDA2 and SCL2, to VCC2 must be selected in such a way that output current drawn is ≤ 50 mA. The maximum pullup resistors on the input lines (SDA1 and SCL1) to VCC1 and on output lines (SDA1 and SCL1) to VCC2, depends on the load and rise time requirements on the respective lines to comply with I2C protocols.

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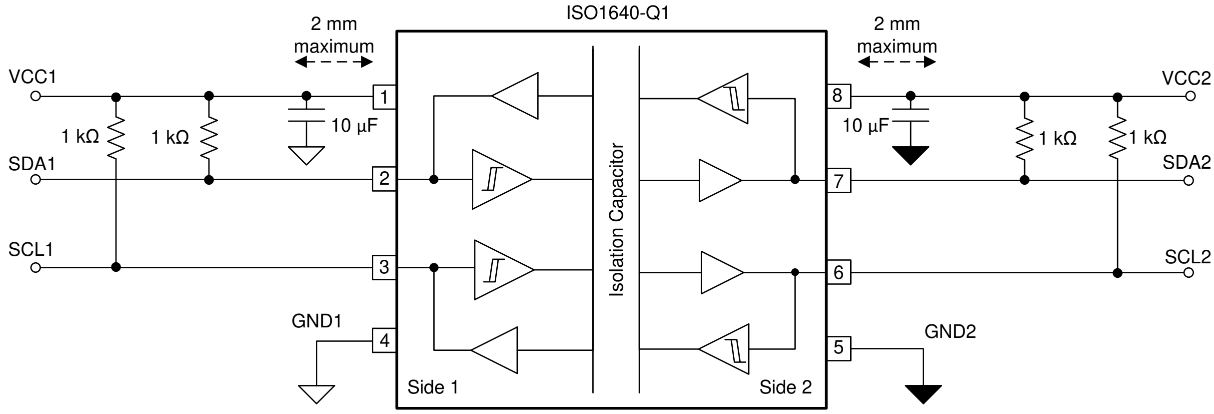

Figure 9-5. Typical ISO1640-Q1 Circuit Hookup

Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, TI recommends connecting a 0.1-µF bypass capacitor at the input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501-Q1 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* (SLLSEF3).

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9 Layout

9.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 9-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284)

9.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

9.2 Layout Example

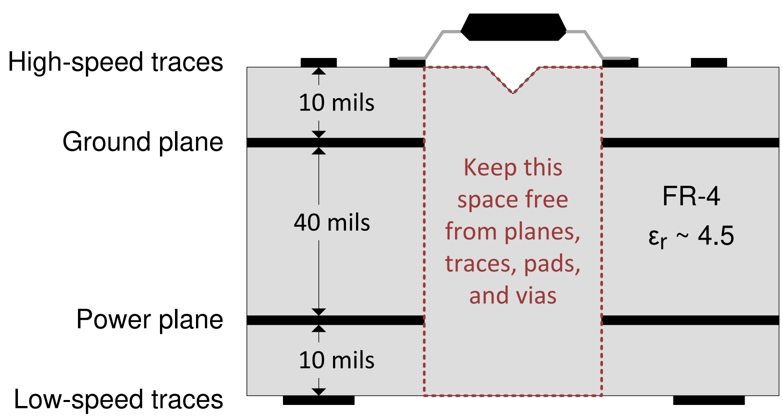

Figure 9-1. Recommended Layer Stack

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems application report*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *What is EMC? 4 questions about EMI, radiated emissions, ESD and EFT in isolated systems*
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505x Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *I2C Bus Pullup Resistor Calculation*
- Texas Instruments, *ISO1640DEVM Evaluation Module Users Guide*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resource

10.4 Trademarks

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XISO1640BQDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XISO1640QDWRQ1	ACTIVE	SOIC	DW	16	2500	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO1640-Q1 :

- Catalog : ISO1640

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

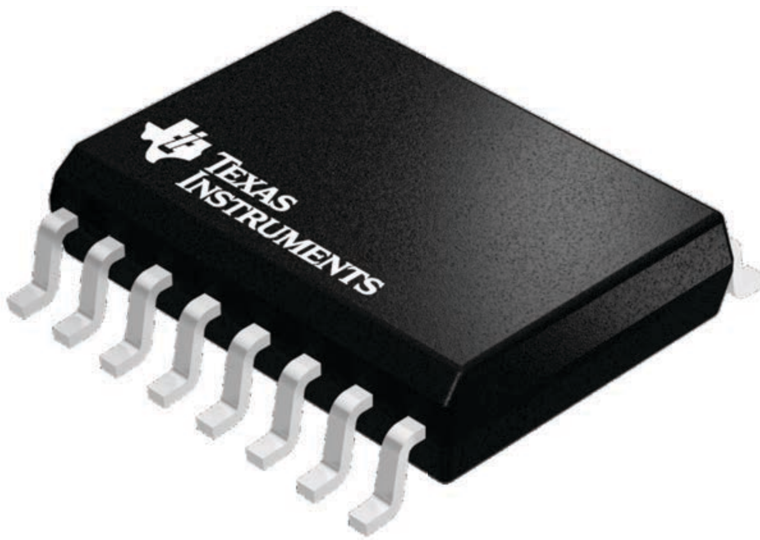
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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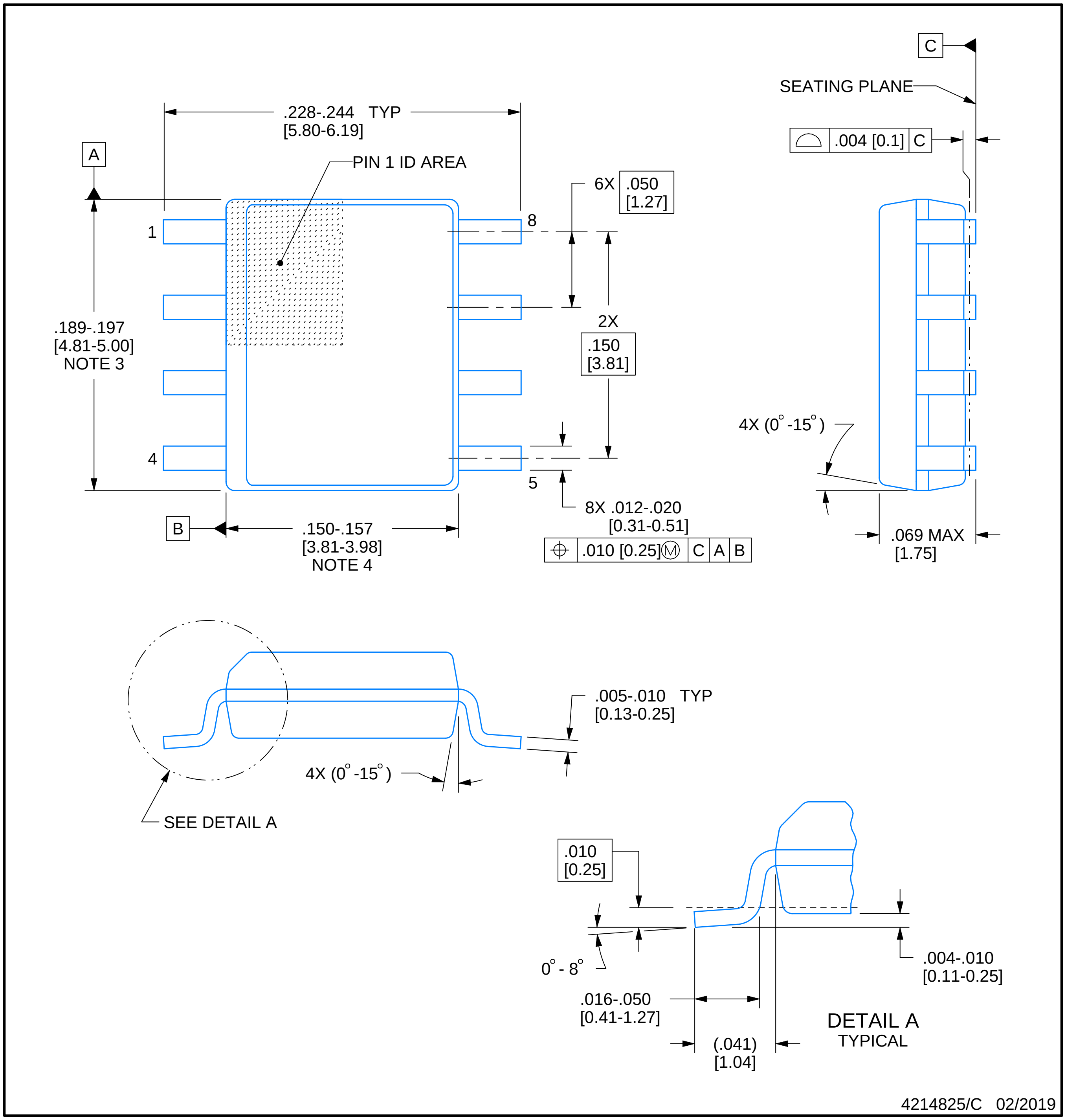

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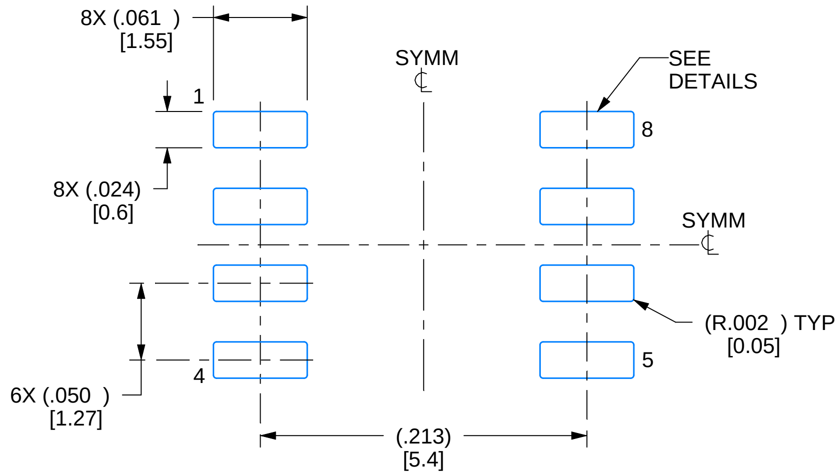
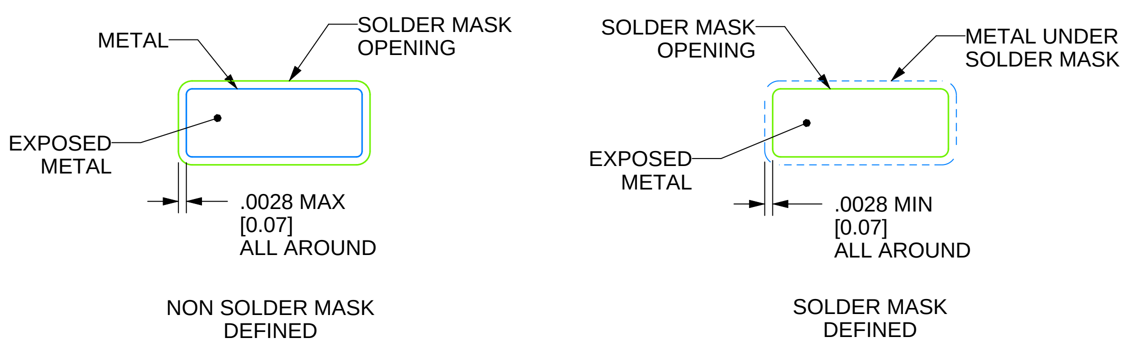
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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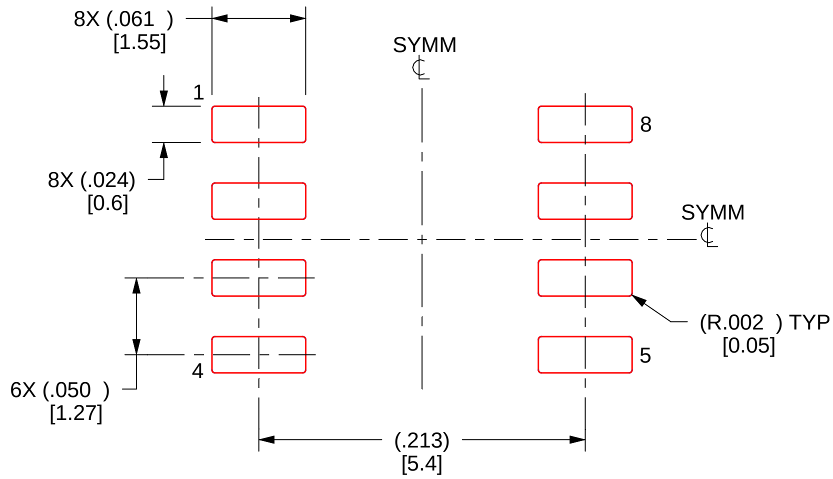
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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