

New Jersey Semi-Conductor Products, Inc.

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3N201, 3N202, 3N203

ELECTRICAL CHARACTERISTICS (continued) ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Common Source Power Gain ($V_{DD} = 18\text{ Vdc}$, $V_{GG} = 7.0\text{ Vdc}$, $f = 200\text{ MHz}$) (Figure 1) ($V_{DD} = 18\text{ Vdc}$, $V_{GG} = 6.0\text{ Vdc}$, $f = 45\text{ MHz}$) (Figure 3) ($V_{DD} = 18\text{ Vdc}$, $f_{LO} = 245\text{ MHz}$, $f_{RF} = 200\text{ MHz}$) (Figure 2)	G_{ps}	15	20	25	dB
Bandwidth ($V_{DD} = 18\text{ Vdc}$, $V_{GG} = 7.0\text{ Vdc}$, $f = 200\text{ MHz}$) (Figure 1) ($V_{DD} = 18\text{ Vdc}$, $f_{LO} = 245\text{ MHz}$, $f_{RF} = 200\text{ MHz}$) (Figure 2) ($V_{DD} = 18\text{ Vdc}$, $V_{GG} = 6.0\text{ Vdc}$, $f = 45\text{ MHz}$) (Figure 3)	BW	5.0	—	9.0	MHz
Gain Control Gate-Supply Voltage(4) ($V_{DD} = 18\text{ Vdc}$, $\Delta G_{ps} = -30\text{ dB}$, $f = 200\text{ MHz}$) (Figure 1) ($V_{DD} = 18\text{ Vdc}$, $\Delta G_{ps} = -30\text{ dB}$, $f = 45\text{ MHz}$) (Figure 3)	$V_{GG}(GC)$	0	-1.0	-3.0	Vdc

) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

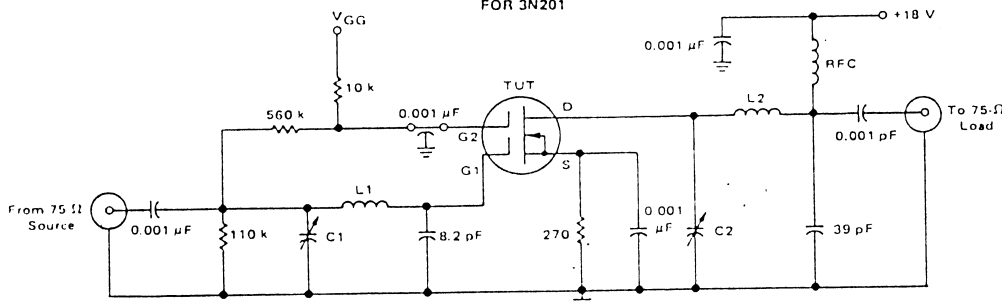
) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

) ΔG_{ps} is defined as the change in G_{ps} from the value at $V_{GG} = 7.0\text{ volts}$ (3N201) and $V_{GG} = 6.0\text{ volts}$ (3N203).

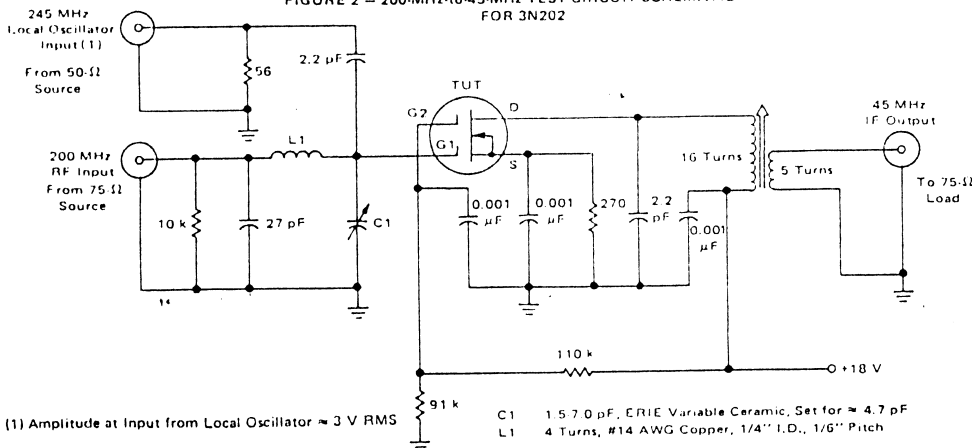
) Power Gain Conversion

FIGURE 1 — 200-MHz TEST CIRCUIT SCHEMATIC FOR 3N201



C1 4.0-30 pF, ERIE Variable Ceramic, Set for $\approx 22\text{ pF}$
C2 4.0-30 pF, ERIE Variable Ceramic, Set for $\approx 10\text{ pF}$
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch
L2 3 Turns, #14 AWG Copper, 1/4" I.D., 1/8" Pitch
RFC DELEVAN No. 153712, 1.0 μH

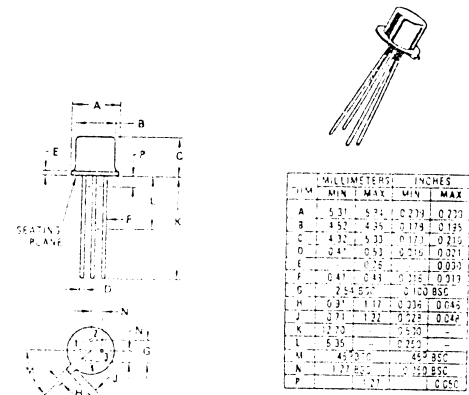
FIGURE 2 — 200-MHz-to-45-MHz TEST CIRCUIT SCHEMATIC FOR 3N202



(1) Amplitude at Input from Local Oscillator $\approx 3\text{ V RMS}$

C1 1.5-7.0 pF, ERIE Variable Ceramic, Set for $\approx 4.7\text{ pF}$
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch

TO-72



ALL JEDEC dimensions and notes apply

CASE 20 STYLES

STYLE 1 PIN 1 SOURCE 2 DRAIN 3 GATE 4 GATE LEAD	STYLE 5 PIN 1 SOURCE 2 DRAIN 3 GATE 4 GATE	STYLE 6 PIN 1 DRAIN 2 SOURCE AND 3 SUBSTRATE AND 4 GATE	STYLE 7 PIN 1 DRAIN 2 SOURCE AND 3 GATE 4 GATE AND SUBSTRATE	STYLE 8 PIN 1 DRAIN 2 SOURCE 3 GATE 4 GATE AND SUBSTRATE	STYLE 9 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 10 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 11 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 12 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 13 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 14 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 15 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 16 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 17 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 18 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 19 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE	STYLE 20 PIN 1 DRAIN 2 GATE 3 GATE 4 GATE AND SUBSTRATE
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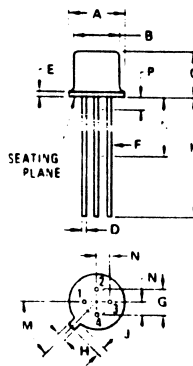


Quality Semi-Conductors

Package Outline Dimensions

Dimensions are in inches unless otherwise noted.

TO-72 (TO-206AF)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.52	4.95	0.178	0.195
B	4.32	5.33	0.170	0.210
C	0.41	0.53	0.016	0.021
D	0.76		0.030	
E	0.41	0.48	0.016	0.019
F	2.54 BSC		0.100 BSC	
G	0.91	1.17	0.036	0.046
H	0.71	1.22	0.028	0.048
J	12.70		0.500	
K	6.35		0.250	
L	35.0 BSC		1.375 BSC	
M	1.27 BSC		0.050 BSC	
N	1.27		0.050	

ALL JEDEC dimensions and notes apply