

Features

- Any frequency between 220.000001 MHz and 725 MHz accurate to 6 decimal places
- Widest pull range options: ± 25 , ± 50 , ± 80 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600 , ± 3200 ppm
- 0.23 ps RMS phase jitter (typ) over 12 kHz to 20 MHz bandwidth
- Wide temperature range support from -40°C to 85°C
Contact [SiTime](#) for other temperature range options
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm
Contact [SiTime](#) for 5.0 x 3.2 mm package
- For frequencies 1 MHz to 220 MHz, refer to [SiT3372](#)

Applications

- Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors, Remote Radio Head (RRH)
- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Optical Transport Network (OTN)

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

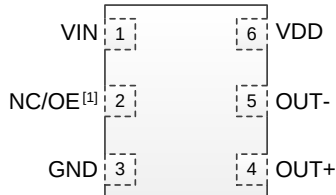
Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	725	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25°C. Contact SiTime for ±15 ppm.
		-20	–	+20	ppm	
		-30	–	+30	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25°C.
		-50	–	+50	ppm	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact SiTime for other temperature range options.
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Voltage Control Characteristics						
Pull Range	PR	±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200ppm			ppm	See the APR (Absolute Pull Range) Table 11 Contact SiTime for custom pull range options.
Upper Control Voltage	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	–	10	–	MΩ	
Control Voltage Input Bandwidth	V_c	–	10	–	kHz	Contact SiTime for other input bandwidth options
Pull Range Linearity	Lin	–	–	1.0	%	
Frequency Change Polarity	–	Positive Slope			–	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 2, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 2, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	μs	

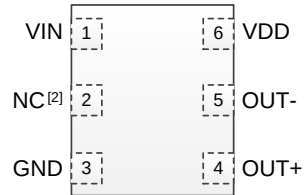
Table 2. Pin Description

Pin	Symbol	Functionality	
1	VIN	Input	Control Voltage
2	NC/OE	No Connect (NC)	No Connect: Leave floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.
		Output Enable (OE)	H ^[1,2] : specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 package. Pin 2 on 3225 package is NC.
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	Vdd	Power	Power supply voltage ^[3]

Top View

Figure 1. Pin Assignments
(7.0 x 5.0 mm package)

Top View

Figure 2. Pin Assignments
(3.2 x 2.5 mm package)

Notes:

1. OE mode is only available in the 7050 package. 3225 package is NC.
2. A pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
3. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance.

Table 3. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	97	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	63	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 3
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 3
Output Differential Voltage Swing	V _{Swing}	1.2	1.6	2.0	V	See Figure 4
Rise/Fall Time	Tr, Tf	–	225	290	ps	20% to 80%, see Figure 3
Jitter						
RMS Phase Jitter (random)	T _{phj}	–	0.225	0.270	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. 7.0 x 5.0 mm package.
		–	0.225	0.275	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdd levels, includes spurs.
RMS Period Jitter ^[4]	T _{jitt}	–	1.0	1.6	ps	f = 322.265625 MHz, Vdd = 3.3V or 2.5V

Table 4. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	89	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	67	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Output Characteristics						
Differential Output Voltage	V _{OD}	250	–	450	mV	See Figure 5
V _{OD} Magnitude Change	ΔV _{OD}	–	–	50	mV	See Figure 5
Offset Voltage	V _{OS}	1.125	–	1.375	V	See Figure 5
V _{OS} Magnitude Change	ΔV _{OS}	–	–	50	mV	See Figure 5
Rise/Fall Time	T _r , T _f	–	370	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 5
Jitter						
RMS Phase Jitter (random)	T _{phj}	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs. 7.0 x 5.0 mm package.
		–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs. 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels, includes spurs.
RMS Period Jitter ^[4]	T _{jitt}	–	0.92	1.6	ps	f = 322.265625 MHz, V _{dd} = 3.3V or 2.5V

Table 5. Electrical Characteristics – HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	102	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	67	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	36	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	V _{OH}	0.6	–	0.90	V	See Figure 3
Output Low Voltage	V _{OL}	-0.05	–	0.08	V	See Figure 3
Output Differential Voltage Swing	V _{Swing}	1.2	1.4	1.8	V	See Figure 4
Rise/Fall Time	T _r , T _f	–	360	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 3
Jitter						
RMS Phase Jitter (random)	T _{phj}	–	0.215	0.270	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs. 7.0 x 5.0 mm package.
		–	0.225	0.275	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs. 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels, includes spurs.
RMS Period Jitter ^[4]	T _{jitt}	–	1.0	1.6	ps	f = 322.265625 MHz, V _{dd} = 3.3V or 2.5V

Notes:

4. Measure according to JESD65B.

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

Table 7. Thermal Considerations^[5]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

Notes:

5. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature^[6]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C

Notes:

6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

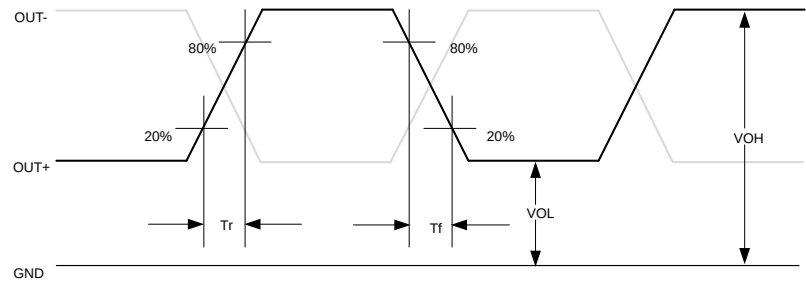


Figure 3. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

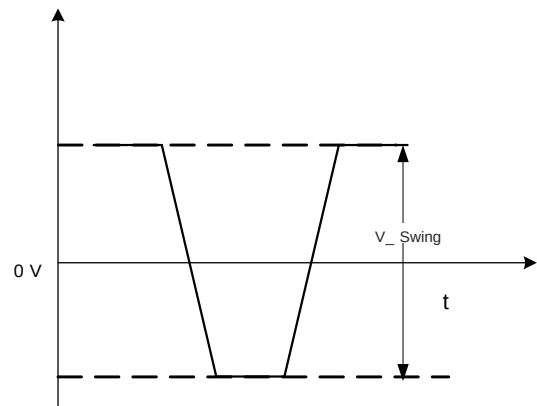


Figure 4. LVPECL/HCSL Voltage Levels across Differential Pair

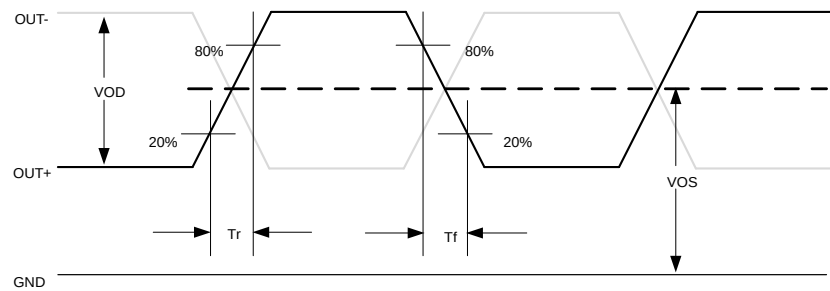


Figure 5. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

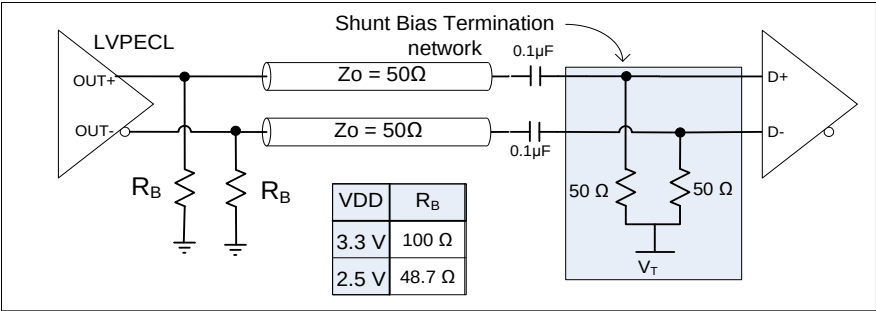


Figure 6. LVPECL with AC-coupled termination

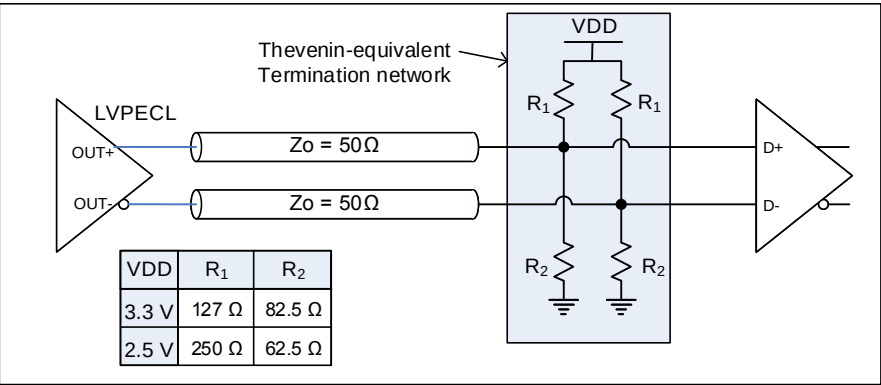


Figure 7. LVPECL DC-coupled load termination with Thevenin equivalent network

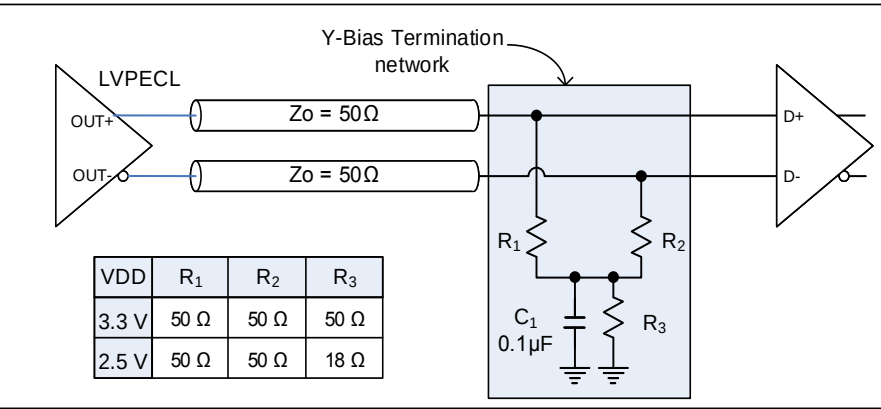


Figure 8. LVPECL with Y-Bias termination

Termination Diagrams (continued)

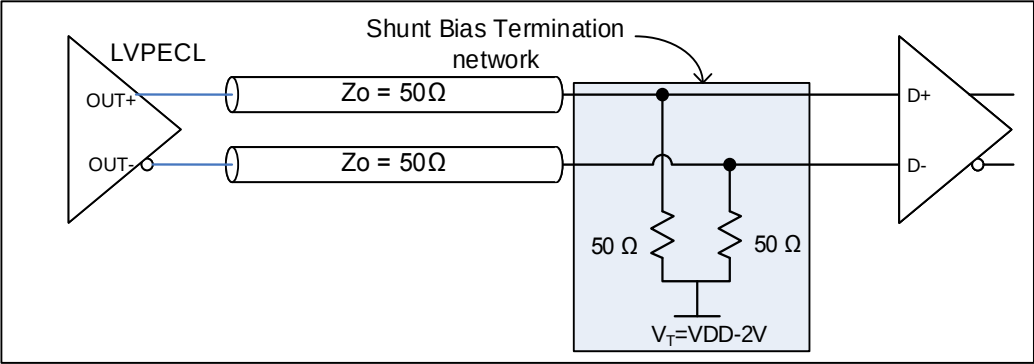


Figure 9. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (continued)

LVDS:

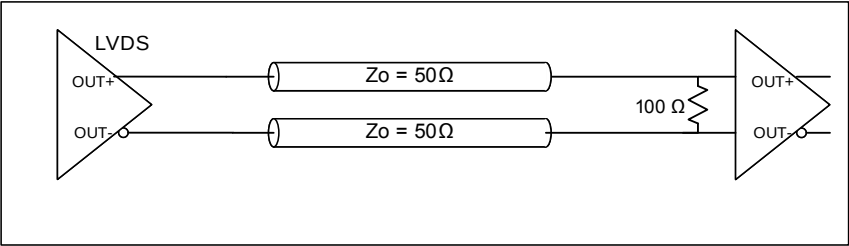


Figure 10. LVDS single DC termination at the load

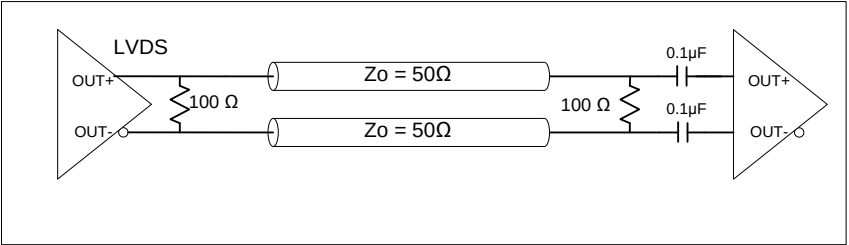


Figure 11. LVDS double AC termination with capacitor close to the load

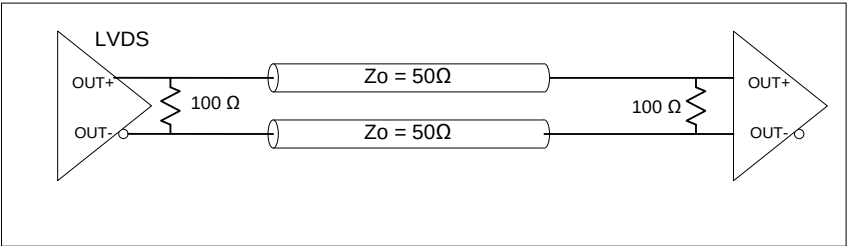


Figure 12. LVDS double DC termination

Termination Diagrams (continued)

HCSL:

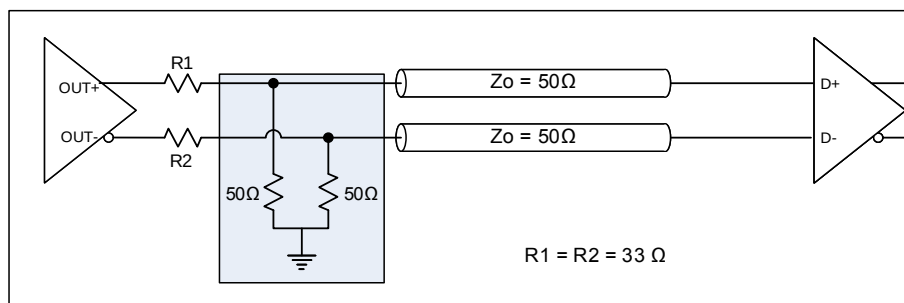


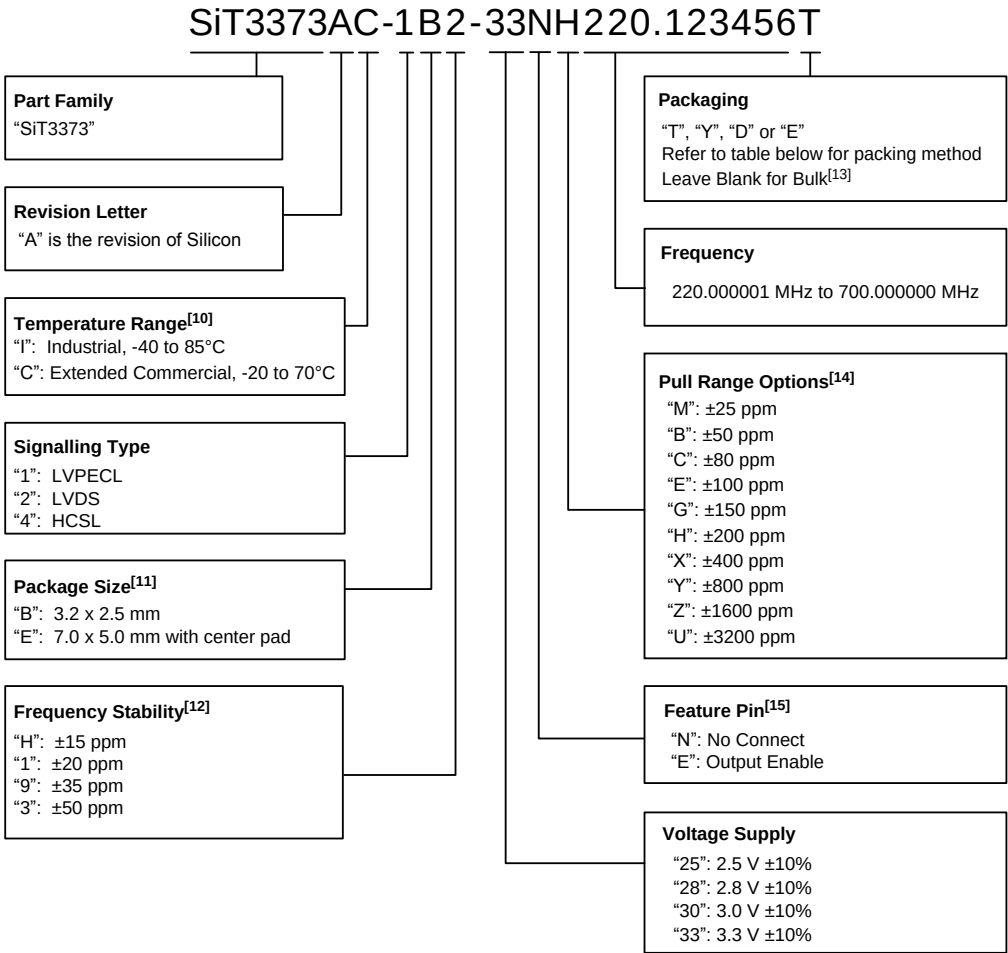
Figure 13. HCSL interface termination

Dimensions and Patterns

Package Size – Dimensions (Unit: mm) ^[7]	Recommended Land Pattern (Unit: mm) ^[8]																																																
3.2 x 2.5 x 0.75 mm Top view: YXXXX, D, E, e, W, J, J Side view: A Land pattern: 2.25, 1.6, 0.65, 1.05, 1.00 <table><tr><th colspan="5">Dimension Table</th></tr><tr><th></th><th>Symbol</th><th>Min</th><th>Nom</th><th>Max</th></tr><tr><td>TOTAL THICKNESS</td><td>A</td><td>0.800</td><td>0.850</td><td>0.900</td></tr><tr><td rowspan="2">BODY SIZE</td><td>X D</td><td>2.400</td><td>2.500</td><td>2.600</td></tr><tr><td>Y E</td><td>3.200</td><td>3.200</td><td>3.300</td></tr><tr><td>LEAD PITCH</td><td>e</td><td colspan="3">1.100 BSC</td></tr><tr><td>LEAD LENGTH</td><td>L</td><td>0.650</td><td>0.700</td><td>0.750</td></tr><tr><td>LEAD WIDTH</td><td>W</td><td>0.550</td><td>0.600</td><td>0.650</td></tr></table> 6L QFN 3.2 x 2.5 x 0.75 mm POD-38 Rev A	Dimension Table						Symbol	Min	Nom	Max	TOTAL THICKNESS	A	0.800	0.850	0.900	BODY SIZE	X D	2.400	2.500	2.600	Y E	3.200	3.200	3.300	LEAD PITCH	e	1.100 BSC			LEAD LENGTH	L	0.650	0.700	0.750	LEAD WIDTH	W	0.550	0.600	0.650	3.2 x 2.5 x 0.75 mm 2.25, 1.6, 0.65, 1.05, 1.00									
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7.0 x 5.0 x 0.90 mm^[9] Top view: YXXXX, D, E, e, W, J, J, K Side view: A Land pattern: 4.15, 1.25, 1.70, 1.00, 1.45, 5.00, 3.90, 3.00, ø 0.30 <table><tr><th colspan="5">Dimension Table</th></tr><tr><th></th><th>Symbol</th><th>Min</th><th>Nom</th><th>Max</th></tr><tr><td>TOTAL THICKNESS</td><td>A</td><td>0.800</td><td>0.850</td><td>0.900</td></tr><tr><td rowspan="2">BODY SIZE</td><td>X D</td><td>4.900</td><td>5.000</td><td>5.100</td></tr><tr><td>Y E</td><td>6.900</td><td>7.000</td><td>7.100</td></tr><tr><td rowspan="2">EP SIZE</td><td>X J</td><td>1.400</td><td>1.500</td><td>1.600</td></tr><tr><td>Y K</td><td>3.400</td><td>3.500</td><td>3.600</td></tr><tr><td>LEAD PITCH</td><td>e</td><td colspan="3">2.540 BSC</td></tr><tr><td>LEAD LENGTH</td><td>L</td><td>0.850</td><td>0.900</td><td>0.950</td></tr><tr><td>LEAD WIDTH</td><td>W</td><td>1.350</td><td>1.400</td><td>1.450</td></tr></table> 6L QFN 7.0 x 5.0 x 0.90 mm POD-37 Rev A	Dimension Table						Symbol	Min	Nom	Max	TOTAL THICKNESS	A	0.800	0.850	0.900	BODY SIZE	X D	4.900	5.000	5.100	Y E	6.900	7.000	7.100	EP SIZE	X J	1.400	1.500	1.600	Y K	3.400	3.500	3.600	LEAD PITCH	e	2.540 BSC			LEAD LENGTH	L	0.850	0.900	0.950	LEAD WIDTH	W	1.350	1.400	1.450	7.0 x 5.0 x 0.90 mm^[9] 4.15, 1.25, 1.70, 1.00, 1.45, 5.00, 3.90, 3.00, ø 0.30 Note: Circles in center pad are thermal vias, recommended to improve thermal performance
Dimension Table																																																	
	Symbol	Min	Nom	Max																																													
TOTAL THICKNESS	A	0.800	0.850	0.900																																													
BODY SIZE	X D	4.900	5.000	5.100																																													
	Y E	6.900	7.000	7.100																																													
EP SIZE	X J	1.400	1.500	1.600																																													
	Y K	3.400	3.500	3.600																																													
LEAD PITCH	e	2.540 BSC																																															
LEAD LENGTH	L	0.850	0.900	0.950																																													
LEAD WIDTH	W	1.350	1.400	1.450																																													

- Notes:
- 7. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
 - 8. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance
 - 9. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information



- Notes:
- 10. Contact [SiTime](#) for higher temperature options
 - 11. Contact [SiTime](#) for 5.0 x 3.2 package
 - 12. Contact [SiTime](#) for ±15 ppm
 - 13. Bulk is available for sampling only
 - 14. Contact [SiTime](#) for custom pull range options
 - 15. "E": Output Enable function is only available in 7.0 x 5.0 mm package

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

Table 11. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab)

Nominal Pull Range	Frequency Stability			
	± 15	± 25	± 35	±50
	APR (ppm)			
± 25	± 5	—	—	—
± 50	± 30	± 20	± 10	—
± 80	± 60	± 50	± 40	± 25
± 100	± 80	± 70	± 60	± 45
± 150	± 130	± 120	± 110	± 95
± 200	± 180	± 170	± 160	± 145
± 400	± 380	± 370	± 360	± 345
± 800	± 780	± 770	± 760	± 745
± 1600	± 1580	± 1570	± 1560	± 1545
± 3200	± 3180	± 3170	± 3160	± 3145

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	http://www.sitime.com/products/field-programmable-oscillators
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/component/docman/doc_download/243-manufacturing-notes-for-sitime-oscillators
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Table 13. Revision History

Revision	Release Date	Change Summary
1.0	09/30/2017	Initial release

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