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NTE2055
Integrated Circuit
CMOS, 3 $^{1}/_{2}$ Digit A/D Converter

Description:

The NTE2055 is a high performance, low power, 3 $^{1}/_{2}$ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. Available in a 24–Lead DIP type package, this device is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The NTE2055 is ratiometric and may be used over a full–scale range from 1.999V to 199.9mV. Systems using this device may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5V supplies. The output drive conforms with standard B–Series CMOS specifications and can drive a low–power Schottky TTL load.

The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the NTE2055 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

Features:

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999V and 199.9mV
- Up to 25 Conversions /s
- Z_{in} > 100MΩ
- Auto–Polarity and Auto–Zero
- Single Positive Voltage Reference
- Standard B–Series CMOS Outputs: Drives One Low Power Schottky Load
- Uses On–Chip System Clock, or External Clock
- Wide Supply Range: e.g., ±4.5V to ±8.0V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count
- Chip Complexity: 1326 FETs

Absolute Maximum Ratings:

DC Supply Voltage, V_{DD} to V_{EE} . . . . . –0.5V to +18V
Voltage, Ant Pin, Referenced to V_{EE}, V . . . . . –0.5V to V_{DD}+0.5V
DC Input Current, Per Pin, I_{in} . . . . . ±10mA
Operating Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Recommended Operating Conditions: (V_{SS} = 0 or V_{EE})

DC Supply Voltage
V_{DD} to Analog GND, V_{DD} . . . . . +5.0 to 8.0V
V_{EE} to Analog GND, V_{EE} . . . . . –2.8 to –8.0V
Clock Frequency, f_{Clk} . . . . . 32 to 400kHz
Zero Offset Correction Capacitor, C_o . . . . . 0.1 ±20%µF

Electrical Characteristics: (C_I = 0.1µF mylar, R_I = 470kΩ @ V_{ref} = 2V, R_I = 27kΩ @ V_{ref} = 200mV, R_C = 300kΩ, T_A = +25°C ; all voltages referenced to Analog GND, Pin1, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Linearity–Output Reading		V_{DD} = 5V, V_{EE} = –5V, Note 2	V_{ref} = 2.000V	–0.05 – Count	±0.05	+0.05 + Count	%rdg
			V_{ref} = 200.0mV	–	±0.05	–	%rdg
Stability – Output Reading		V_{DD} = 5V, V_{EE} = –5V, V_X = 199mV, V_{ref} = 200mV		–	–	3	LSD
Symmetry – Output Reading		V_{DD} = 5V, V_{EE} = –5V, V_{ref} = 2000mV, Note 3		–	–	4	LSD
Zero–Output Reading		V_{DD} = 5V, V_{EE} = –5V, V_X = 0V, V_{ref} = 2V		–	0	0	LSD
Bias Current Analog Input		V_{DD} = 5V, V_{EE} = –5V		–	±20	±100	pA
Reference Input				–	±20	±100	pA
Analog GND				–	±20	±500	pA
Common Mode Rejection		V_{DD} = 5V, V_{EE} = –5V, f_{Clk} = 32kHz, V_X = 1.4V, V_{ref} = 2V		–	65	–	dB
Input Voltage (Pin9, Pin10) "0" Level	V_{IL}	V_{DD} = 5V, V_O = 4.5V or 0.5V, Note 3		–	2.25	1.5	V
		V_{DD} = 10V, V_O = 9V or 1V, Note 3		–	4.50	3.0	V
		V_{DD} = 15V, V_O = 13.5V or 1.5V, Note 3		–	6.75	4.0	V
"1" Level	V_{IH}	V_{DD} = 5V, V_O = 0.5V or 4.5V, Note 3		3.5	2.75	–	V
		V_{DD} = 10V, V_O = 1V or 9V, Note 3		7.0	5.50	–	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V, Note 3		11.0	8.25	–	V
Output Voltage (Pin14 to Pin23) "0" Level	V_{OL}	V_{SS} = 0V	V_{DD} = 5V, V_{EE} = –5V	–	0	0.05	V
		V_{SS} = –5V		–	–5.0	–4.95	V
"1" Level	V_{OH}	V_{SS} = 0V		4.95	–5.0	–	V
		V_{SS} = –5V		4.95	5.0	–	V
Output Current (Pin14 to Pin23) Source	I_{OH}	V_{DD} = 5V, V_{EE} = –5V	V_{SS} = 0V, V_{OH} = 4.6V	–0.2	–0.36	–	mA
			V_{SS} = –5V, V_{OH} = 4.5V	–0.5	–0.9	–	mA
Sink	I_{OL}		V_{SS} = 0V, V_{OL} = 0.4V	0.51	0.88	–	mA
			V_{SS} = –5V, V_{OL} = –4.5V	1.3	2.25	–	mA
Input Current (DU, Pin9)	I_{DU}	V_{DD} = 5V, V_{EE} = –5V		–	±0.00001	±0.3	µA
Quiescent Current	I_Q	V_{DD} to V_{EE}, I_{SS} = 0	V_{DD} = 5V, V_{EE} = –5V	–	0.9	2.0	mA
			V_{DD} = 8V, V_{EE} = –8V	–	1.8	4.0	mA
DC Supply Rejection		V_{DD} = 5V, V_{EE} = –5V, V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2V		–	0.5	–	mV/V

Note 2. Accuracy – The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

Note 3. Symmetry – Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

Note 4. Referenced to V_{SS} for Pin9. Referenced to V_{EE} for Pin10.

Truth Table (DS1 =1)

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
–0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
–0 UR	1	0	1	1	Blank
+1	0	1	0	0	$4 \rightarrow 1$ } Hook up
–1	0	0	0	0	$0 \rightarrow 1$ } only seg b
+1 OR	0	1	1	1	$7 \rightarrow 1$ } and c to
–1 OR	0	0	1	1	$3 \rightarrow 1$ } MSD

Notes for Truth Table:

Q3 – $^1/_2$ digit, low for “1”, high for “0”

Q2 – Polarity: “1” = positive, “0” = negative

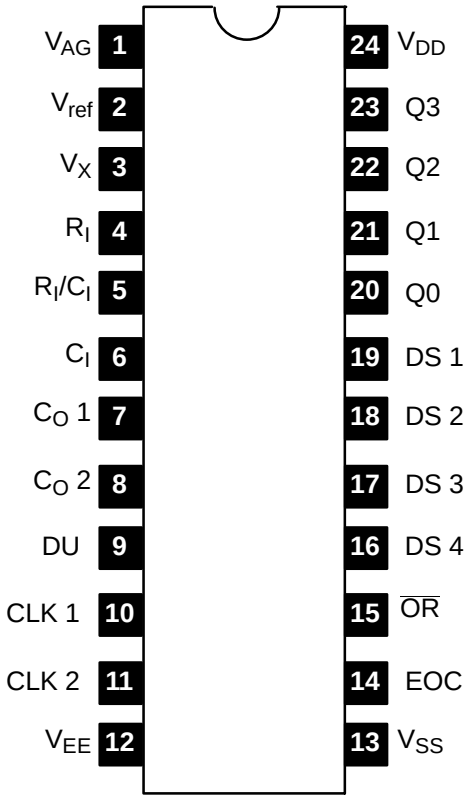
Q0 – Out of range condition exists if Q0 =1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

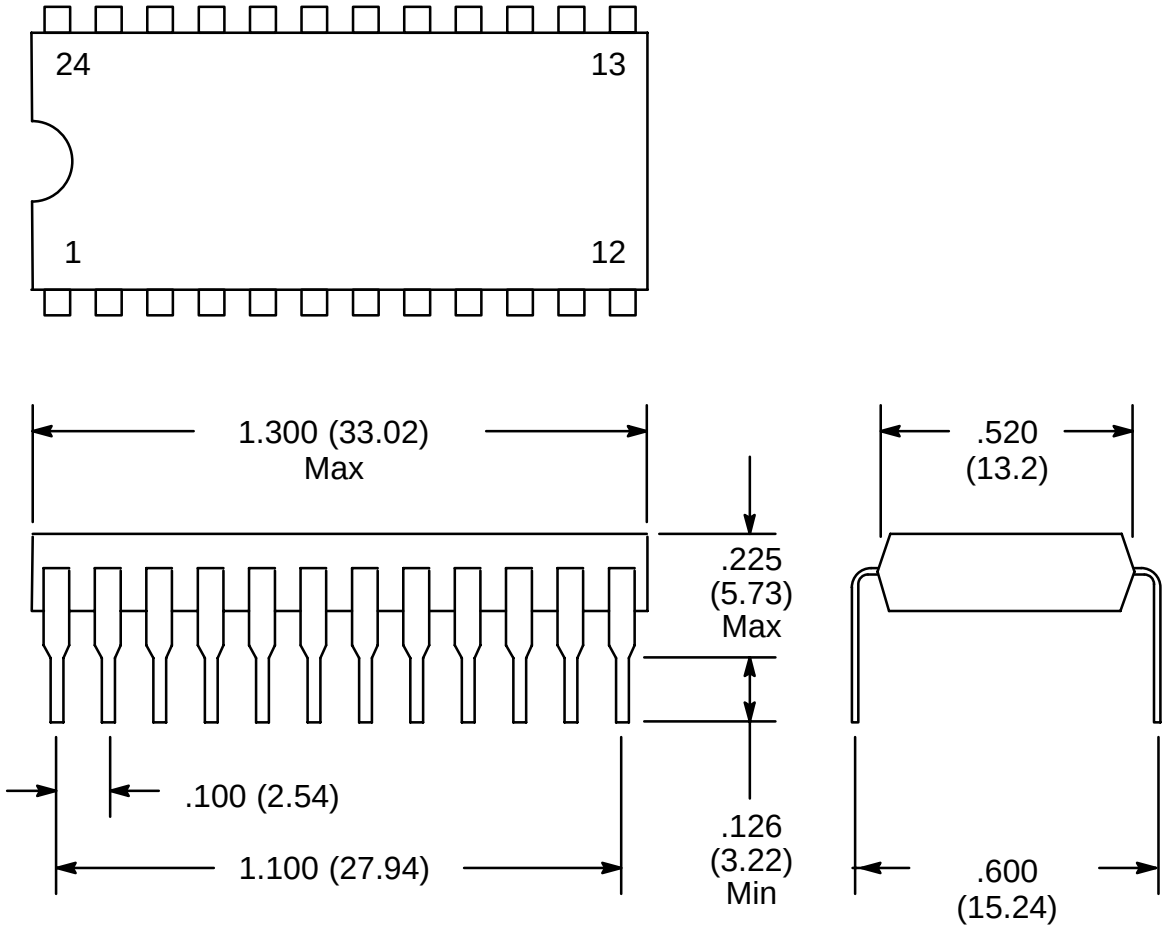
When only segment b and c of the decoder are connected to the $^1/_2$ digit of the display 4, 0, 7, and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999V for a reference of 2V. The underrage indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., o.180V for a reference of 2V.

Caution: If the most significant digit is connected to a display other than a “1” only; such as a full digit display, segments other than b and c must be disconnected. The BCD ti seven decoder must blank on BCD inputs 1010 to 1111.

Pin Connection Diagram




24
13
1
12
1.300 (33.02)
Max
.225
(5.73)
Max
.100 (2.54)
1.100 (27.94)
.126
(3.22)
Min
.520
(13.2)
.600
(15.24)