ALPHA & OMEGA SEMICONDUCTOR

AOC2800

Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

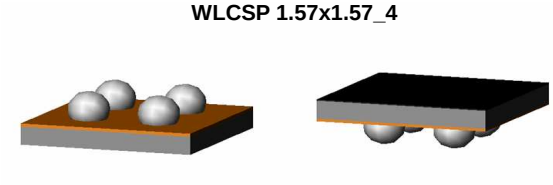
The AOC2800 uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

Product Summary

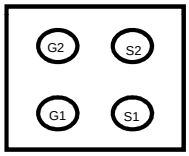
Vss	30V
I_D (at V_{GS}=4.5V)	6A
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 42mΩ
$R_{SS(ON)}$ (at V_{GS}=4.0V)	< 44mΩ
$R_{SS(ON)}$ (at V_{GS}=3.1V)	< 49mΩ
$R_{SS(ON)}$ (at V_{GS}=2.5V)	< 61mΩ

Green Product

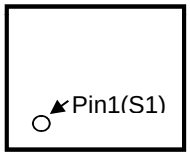
WLCSP 1.57x1.57_4



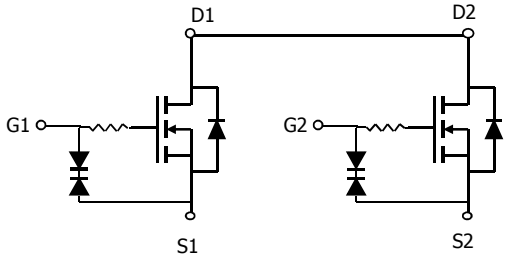
Bottom View



Top View



Equivalent Circuit



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Source-Source Voltage		V_{SS}	**30**	V
Gate-Source Voltage		V_{GS}	**±12**	V
Source Current (DC) Note1	T_A=25°C	I_S	**6**	A
Source Current (Pulse) Note2		I_{SM}	**60**	
Power Dissipation Note1	T_A=25°C	P_D	**1.3**	W
Junction and Storage Temperature Range		T_J, T_{STG}	**-55 to 150**	°C

Note 1. Mounted on minimum pad PCB

Note 2. PW <300 µs pulses, duty cycle 0.5% max

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V, Test Circuit 6	30			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=20V, V_{GS}=0V, Test Circuit 1			1	µA
		T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}= ±10V, Test Circuit 2		1	10	
BV_{GSO}	Gate-Source Breakdown Voltage	V_{SS}=0V, I_G=±250µA, Test Circuit 7	±12			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS} I_S=250µA, Test Circuit 3	0.5	1	1.5	V
$R_{SS(ON)}$	Static Source to Source On-Resistance [Note]	V_{GS}=4.5V, I_S=3A, Test Circuit 4		35	42	mΩ
		T_J=125°C		53	63	
		V_{GS}=4.0V, I_S=3A, Test Circuit 4		37	44	
		V_{GS}=3.1V, I_S=3A, Test Circuit 4		41	49	
		V_{GS}=2.5V, I_S=3A, Test Circuit 4		49	61	
g_{FS}	Forward Transconductance [Note]	V_{SS}=5V, I_S=3A, Test Circuit 3		21		S
V_{FSS}	Diode Forward Voltage [Note]	I_S=1A,V_{GS}=0V, Test Circuit 5		0.7	1	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{SS}=15V, f=1MHz,		984	1180	pF
C_{oss}	Output Capacitance			93		pF
C_{rss}	Reverse Transfer Capacitance			57		pF
R_g	Gate resistance	V_{GS}=0V, V_{SS}=0V, f=1MHz		1.5		kΩ
SWITCHING PARAMETERS						
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{SS}=15V, R_L=2.4Ω, R_{GEN}=6Ω ,		320		ns
t_r	Turn-On Rise Time			800		ns
$t_{D(off)}$	Turn-Off DelayTime			3.8		µs
t_f	Turn-Off Fall Time			3.6		µs
Q_g	Total Gate Charge	V_{G1S1}=4.5V, V_{SS}=15V, I_S=6A		9.1		nC

Note: Pulsed

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

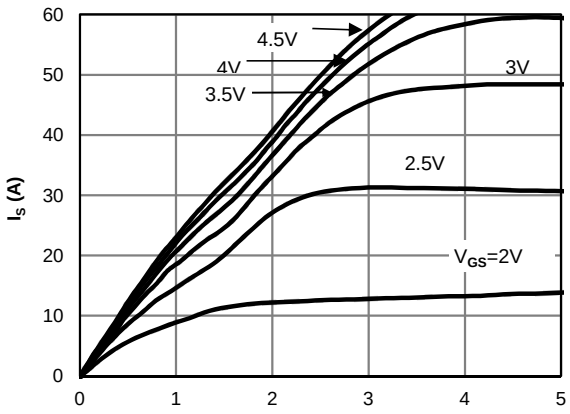
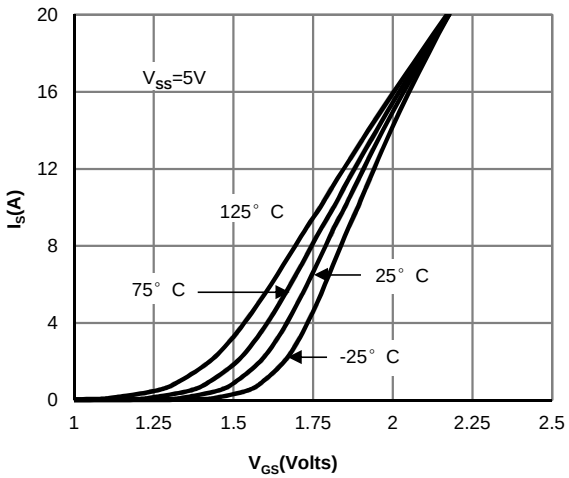


Fig 1: On-Region Characteristics



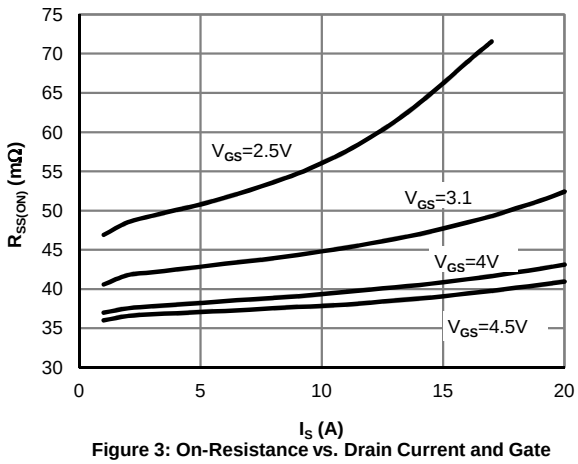


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

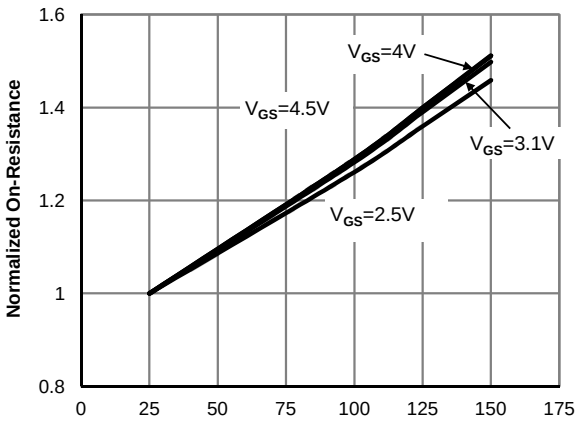


Figure 4: On-Resistance vs. Junction Temperature

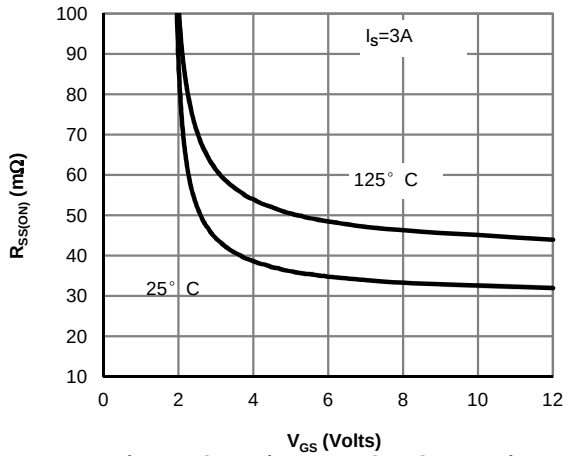


Figure 5: On-Resistance vs. Gate-Source Voltage

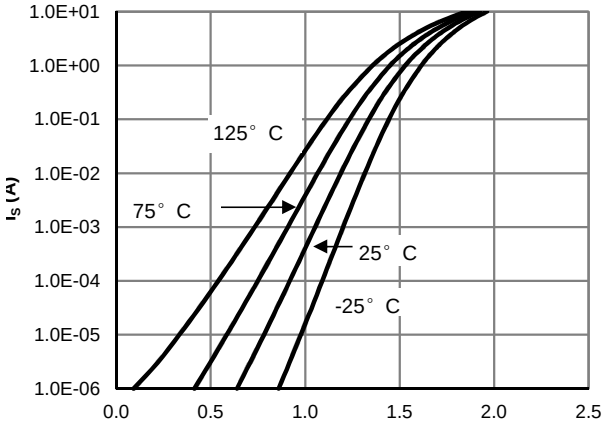


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

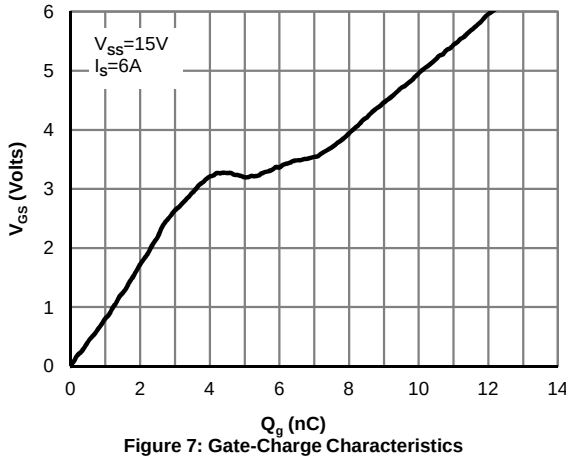


Figure 7: Gate-Charge Characteristics

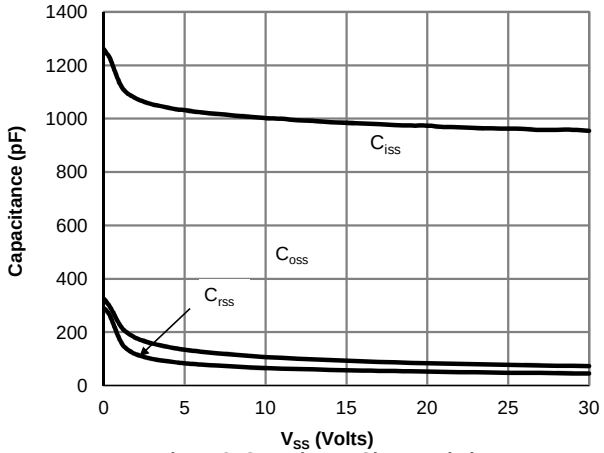


Figure 8: Capacitance Characteristics

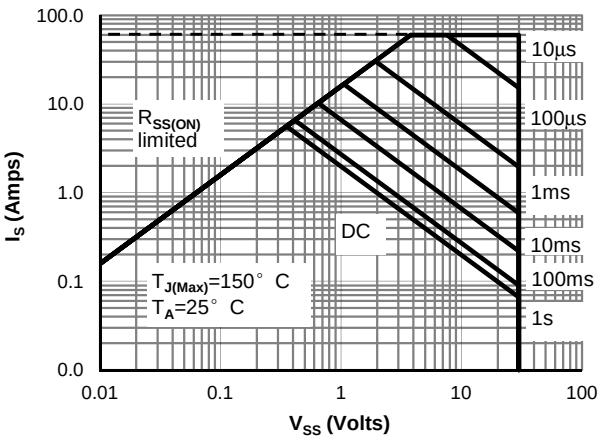


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

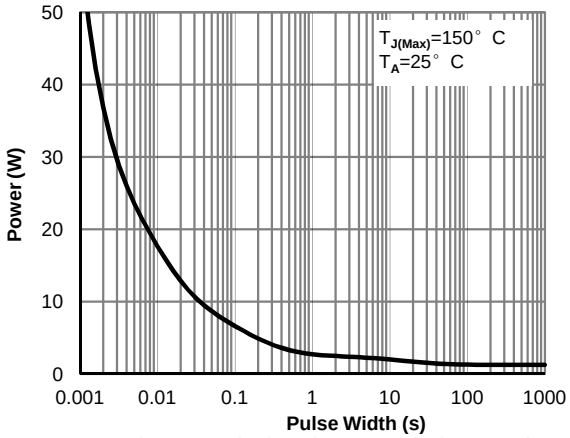


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

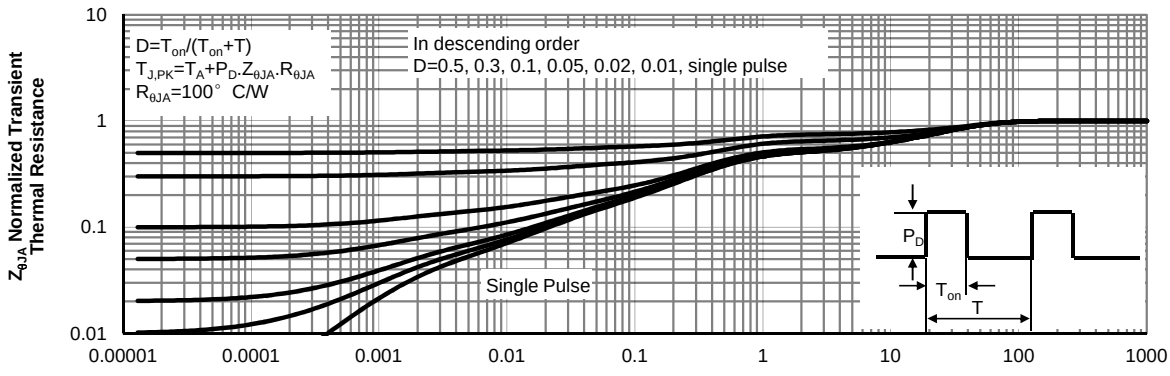
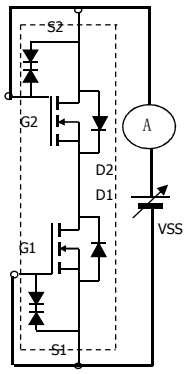


Figure 11: Normalized Maximum Transient Thermal Impedance

TEST CIRCUIT 1 Isss

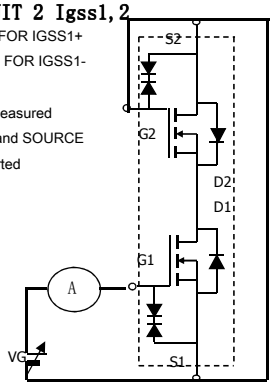
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 2 Igss1, 2

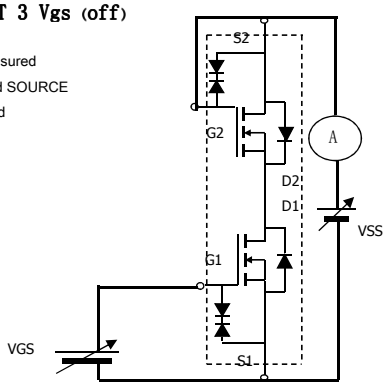
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



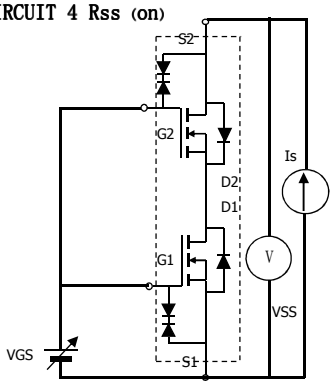
TEST CIRCUIT 3 Vgs (off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 4 Rss (on)

Vss/Is

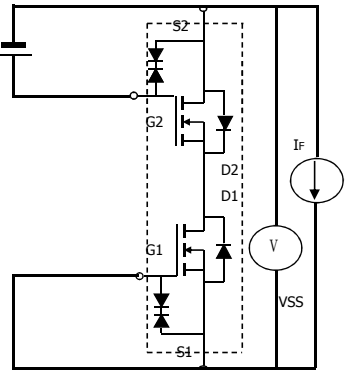


TEST CIRCUIT 5 $V_{F(SS)1,2}$

4.5V

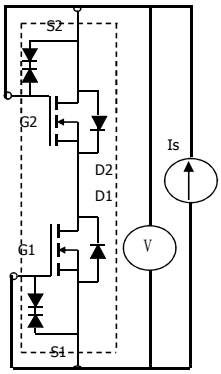
When FET1 measured
FET2 VGS=4.5V

VGS=0



TEST CIRCUIT 6 BV_{DSS}

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 $BV_{GS01,2}$

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted

