Active Clamp Current-Mode PWM Controller

Features

- Peak current-mode PWM Controller
- Two complementary MOSFET drivers
- Programmable deadtime between drivers
- High current gate drivers for main and auxiliary outputs
- Internal high voltage (12V to 250V) start-up regulator
- Programmable V_{IN} undervoltage lockout and hysteresis
- V_{DD} supply operation from 7.8V to 12V
- Fixed frequency PWM operation from 25KHz to 800KHz
- >50% duty cycle operation (up to 95%)
- Programmable slope compensation
- Programmable max duty-cycle/volt-second clamp
- Capacitor programmable soft-start
- Cycle-by-cycle current limiting
- 100ns current sense leading edge blanking
- 2 MHz error amplifier

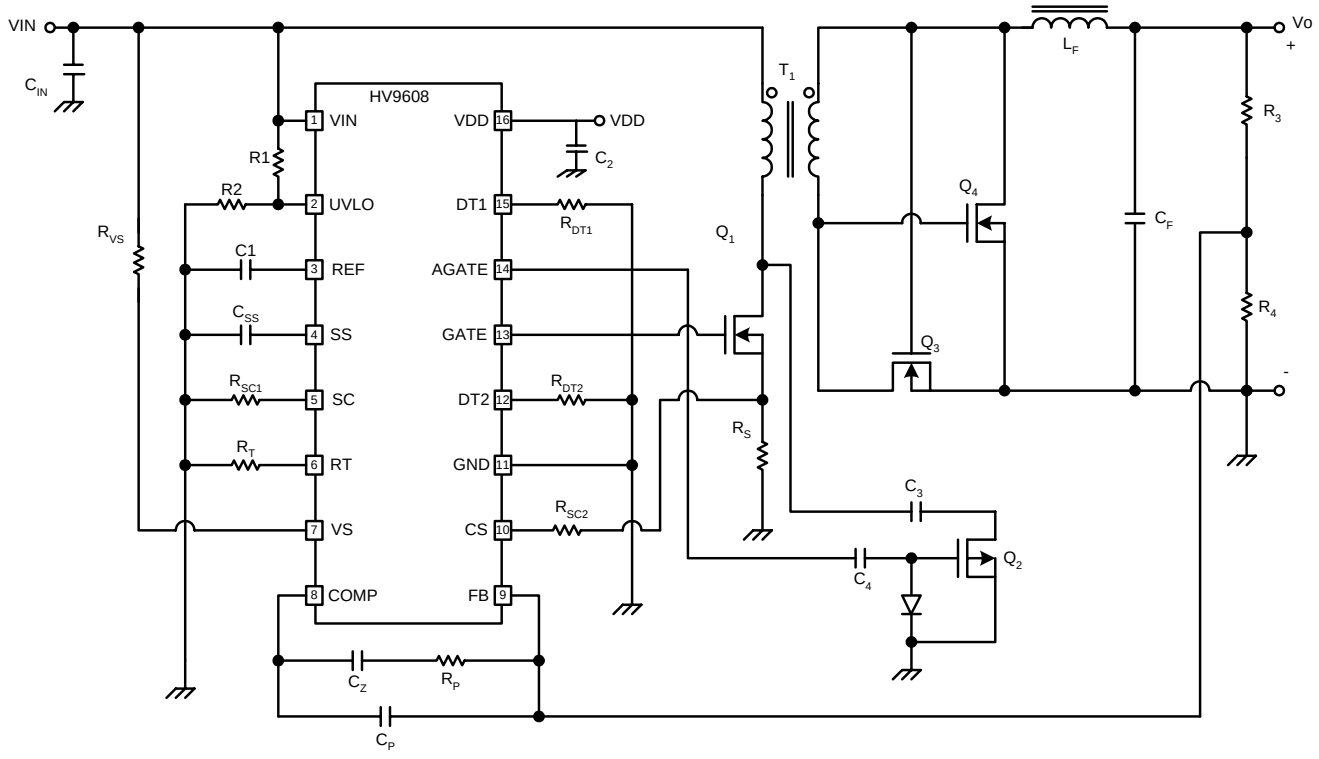
Applications

- Networking
- Telecommunication Systems and Terminals
- IEEE 802.3af PoE PD Devices
- SANS, Servers & Workstations
- High Efficiency Instrumentation Supplies
- High Efficiency Supplies for Portable Equipment

Description

The HV9608 provides a single chip, optimized peak current mode control solution for design of high performance PWM converters using the active-clamp transformer flux reset. Due to its programmable slope compensation feature, the HV9608 allows operation beyond 50% duty cycle. Zero-voltage switching can be accomplished through using the programmable deadtime timers. The switching frequency can be programmed from 25kHz to 800kHz using a single resistor. The internal high voltage startup circuit can ensure start-up from the input voltage from 12V to 250V. It can also maintain the HV9608 in operation when the external "bootstrap" power supply is not available. The startup regulator is disconnected as soon as the HV9608 becomes powered from the bootstrap winding. The HV9608 offers a programmable soft start feature using a single external capacitor. The cycle by cycle current limit feature can protect the converter from overheating and damage by limiting the output over current. The HV9608 will maintain the cycle-by-cycle current limiting mode for a period of time programmed by the soft start capacitor value. The HV9608 includes a single pin UVLO circuit that allows independent accurate setting of both the turn-on and the turn-off threshold voltage. A programmable volt-second clamp reduces voltage stress of the switching devices. The HV9608 is available in a space-saving TSSOP-16 package.

Typical Application Circuit



A122104

Ordering Information

DEVICE	Package Options
	16-Pin TSSOP
HV9608	HV9608TS

Absolute Maximum Ratings*

Input Voltage, V_{IN}	-0.3V to +250V
Supply Voltage, V_{DD}	+13.5V max
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65° to +150°C
Power Dissipation @ 25°C, TSSOP	1000mW

**All voltages referenced to GND pin.*
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics *(The * denotes the specifications which apply over the full operating temperature range of -40°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C, V_{DD} = 10V, unless otherwise noted)*

V_{IN}_Pre-Regulator/Start-up/ V_{DD}_Supply

Symbol	Parameter	Min	Typ.	Max	Units		Conditions
V_{IN}	Regulator input voltage	12		250	V		
$I_{IN,MAX}$	Maximum regulator current	20			mA		V_{IN} = 24V, V_{DD} = 9.2V
$V_{DD,REG}$	Regulator output voltage	9.27	9.46	9.65	V		V_{IN} [12V – 250V]
$V_{DD, MAX}$	Supply voltage range			12	V		To guarantee table parameters
$V_{DD,STOP}$	V_{DD} under voltage threshold	7.58	7.74	7.90	V		V_{DD} falling
$V_{DD,START}$	V_{DD} startup voltage	8.33	8.5	8.67	V		V_{DD} rising
$I_{DD,OFF}$	Supply standby quiescent current		1.25	1.8	mA		R_T = 110 KΩ; R_{DT1}= 80KΩ; R_{DT1}= 80KΩ; UVLO tied to ground;

Under Voltage Lockout (UVLO)

Symbol	Parameter	Min	Typ.	Max	Units		Conditions
$V_{th,UVLO}$	UVLO threshold voltage	1.112	1.135	1.158	V	*	
$I_{HYS,UVLO}$	UVLO hysteresis current		14		μA		*Guaranteed by design*

GATE/AGATE_MOSFET Driver Output

Symbol	Parameter	Min	Typ	Max	Units		Conditions
t_{R1}	Main gate rise time		40	60	nSec		C_{LOAD} = 1nF
t_{F1}	Main gate fall time		20	30	nSec		C_{LOAD} = 1nF
t_{R2}	Auxiliary gate rise time		40	60	nSec		C_{LOAD} = 0.5nF
t_{F2}	Auxiliary gate fall time		20	30	nSec		C_{LOAD} = 0.5nF
R_{DT1}, R_{DT2}	Dead time control resistor range	40		400	KΩ		
d_1	Rising edge delay from AGATE to GATE	80	105	130	nSec		R_{DT1} = 80K
d_2	Falling edge delay from GATE to AGATE	100		400	nSec		R_{DT2} = 80K

Electrical Characteristics *(continued from page 2)* *(The * denotes the specifications which apply over the full operating temperature range of -40°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C, VDD = 10V, unless otherwise noted)*

R_T_Oscillator

Symbol	Parameter	Min	Typ	Max	Units		Conditions
$f_{OSC,MIN}$	Minimum operating frequency		25		KHz		R_T = 1.862MΩ
$f_{OSC,MAX}$	Maximum operating frequency		800		KHz		R_T = 52.3KΩ
f_{OSC}	Frequency variation	220	250	280	KHz	*	R_T = 169KΩ
Δf/f	VDD supply voltage stability of frequency			3	%		R_T = 169KΩ, 7.8V < V_{DD} < 12V

PWM

Symbol	Parameter	Min	Typ	Max	Units		Conditions
D_{MAX}	Maximum GATE duty cycle	95			%	*	f_{OSC} = 100KHz (R_T = 453KΩ)
D_{MAX}	Maximum GATE duty cycle	85			%	*	f_{OSC} = 800KHz (R_T = 52.3KΩ)
D_{MIN}	Minimum GATE duty cycle			0	%		
D_{MIN}	Minimum GATE duty cycle			0	%		

Reference

Symbol	Parameter	Min	Typ	Max	Units		Conditions
V_{REF}	Reference output voltage	1.112	1.135	1.158	V	*	
I_{SRC}	Maximum sourcing current	2			mA		
V_{REF}	Load regulation			5	mV		0 < I_{REF} < 2 mA
V_{REF}	Line regulation			20	mV		7.8V < V_{DD} < 12V

Current Sensing

Symbol	Parameter	Min	Typ	Max	Units		Conditions
V_{CS}	Current limit threshold voltage	0.58	0.6	0.62	V		
t_{BLANK}	Leading edge current sense blanking time		100		nSec		
t_{DELAY}	Current limit delay to output		70	120	nSec		V_{CS} = 0 to 1V step after blanking time

Error Amplifier

Symbol	Parameter	Min	Typ	Max	Units		Conditions
I_{FB}	Input bias current		25	200	nA		V_{FB} = V_{COMP}
V_{FB}	FB input voltage	1.112	1.135	1.158	V		V_{FB} = V_{COMP}
A_{VOL}	Open loop voltage gain	70			dB		
BW	Unity gain bandwidth	2			MHz		
I_{SOURCE}	Maximum output current sourcing	2			mA		
I_{SINK}	Maximum output current sinking	4			mA		
V_{COMP}	Output clamped voltage	3.3	3.45	3.6	V		

Soft Start

Symbol	Parameter	Min	Typ	Max	Units		Conditions
$V_{SS,LOW}$	Soft start low output			0.1	V		
$V_{SS,HI}$	Soft start high output	5.25	5.45	5.65	V		
$I_{SS,HI}$	Soft start output current		7		μA		
t_F	Soft start output fall time			10	μSec		C_{SS} = 0.1μF; V_{FB} = V_{COMP};
$I_{SS,LO}$	Pulse-by-pulse current limit mode sink current		7		μA		

Electrical Characteristics *(continued from page 3)* *(The * denotes the specifications which apply over the full operating temperature range of -40°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C, V_{DD} = 10V, unless otherwise noted)*

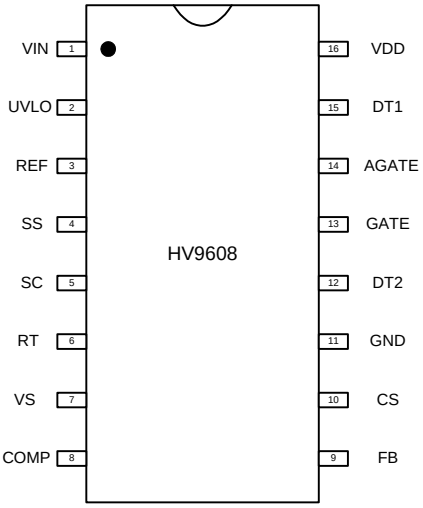
Slope Compensation

Symbol	Parameter	Min	Typ	Max	Units		Conditions
R_{SC}	Slope compensation resistor range	5			kΩ		
$I_{RAMP,PEAK}$	Slope compensation ramp peak current	125	150	175	μA		R_T = 453KΩ; R_{CS} = 500Ω; R_{SC} = 40KΩ; Full duty cycle

Max Duty-Cycle/Voltage-Second Clamp

Symbol	Parameter	Min	Typ	Max	Units		Conditions
I_{in}	VS pin input current range	50μ		3m	A		
D_{VS}	Duty cycle of gate signal	50	55.5	61	%		I_{vs} = 250μA, R_{DT1} = R_{DT2} = 80K; R_T = 169K
D_{VS}	Duty cycle of gate signal	23	25.5	28	%		I_{vs} = 510μA, R_{DT1} = R_{DT2} = 80K; R_T=169K
D_{VS}	Duty cycle of gate signal	21.5	25.5	29	%	*	I_{vs} = 510μA, R_{DT1} = R_{DT2} = 80K; R_T=169K

Pinout



Pin Descriptions

V_{IN} – This is the high voltage linear regulator input. It can accept DC input voltages in the range of 12V to 250V, and supplies a regulated voltage of 9.5V to the V_{DD} pin.

UVLO – This pin can be used for enabling/disabling the HV9608, or as an under voltage lockout input. Both the turn-on and the turn-off thresholds are independently programmable. By selecting appropriate resistor values, a corresponding voltage divider is connected to this pin. When the voltage on this pin falls below a threshold, the high voltage regulator turns-off and the HV9608 becomes disabled.

V_{DD} – This is the power supply pin for the PWM logic and analog circuits. When the input voltage to the V_{IN} pin exceeds the start voltage of 8.5V, the input regulator will bias the voltage at this pin to a nominal of 9.5V. After the PWM has started, an external bootstrap supply can overdrive the output voltage of the regulator disconnecting it from V_{IN}. Bypass this pin to GND using a low impedance high frequency capacitor.

REF – This pin provides a 2% accurate reference voltage that can source up to 2mA of current.

SS – A capacitor connected to this pin determines the soft start time. The soft start capacitor is fully discharged upon detection of the under voltage condition at V_{DD} or UVLO pins.

VS – The resistor connected from this pin to V_{IN} sets the charging current to an internal capacitor, which is matched with the oscillator capacitor. The voltage on the capacitor is compared with a reference voltage of 1.2V, and sets the maximum duty ratio of the PWM controller.

SC – The resistor connected from this pin to GND sets the ramp current sourced from the CS pin for slope compensation.

RT – The resistor connected from this pin to GND programs the frequency of the internal oscillator by setting the charging current for the internal timing capacitor.

GND – Common connection for all Logic and Analog circuits.

AGATE – This push-pull CMOS output is designed to drive the gate of an external P-Channel power MOSFET.

GATE – This push-pull CMOS output is designed to drive the gate of an external N-Channel power MOSFET.

DT2 – This pin is used to set the dead time between the falling edge of GATE signal and AGATE signal.

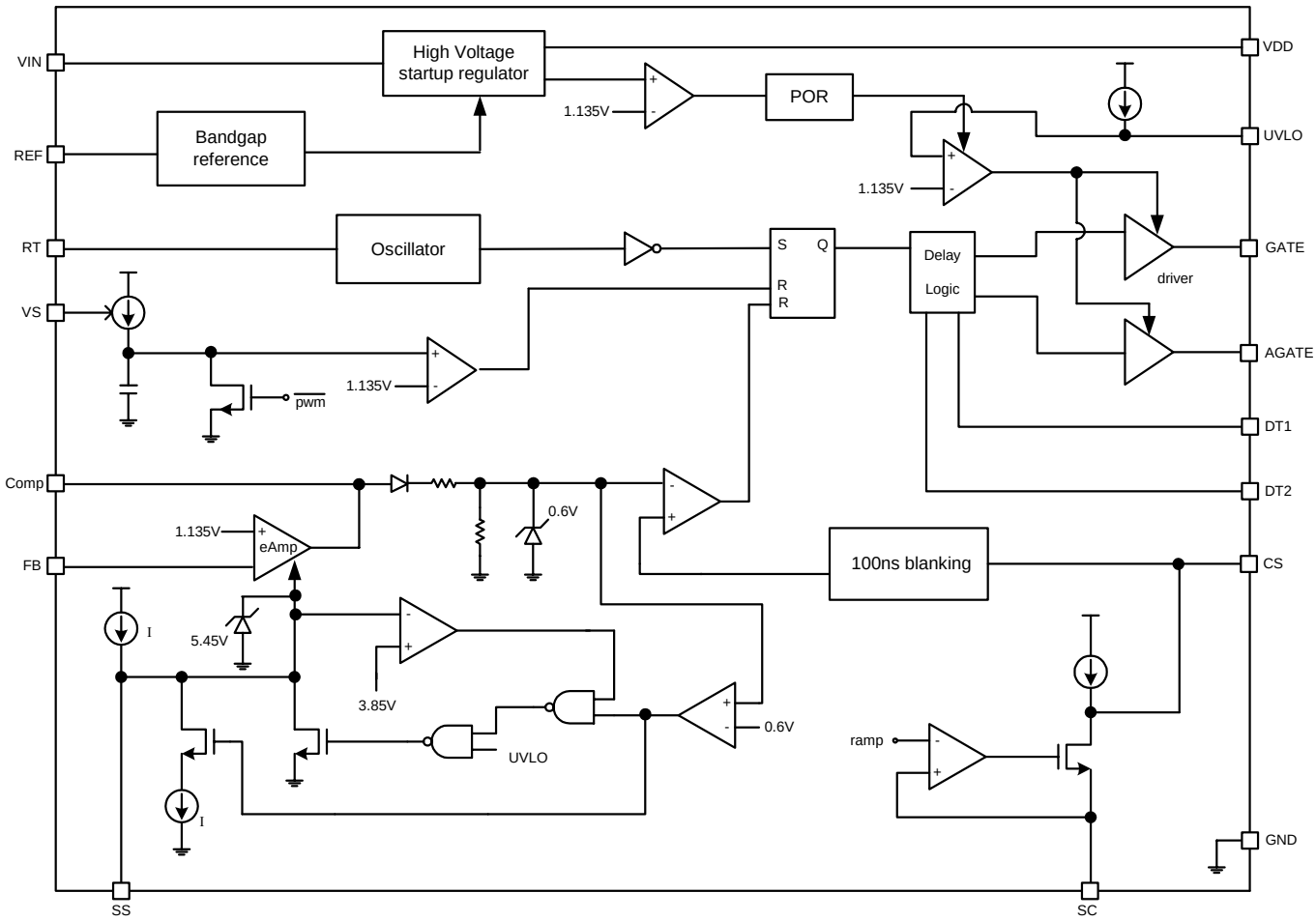
DT1 – This pin is used to set the dead time between the rising edge of AGATE signal and GATE signal.

FB – High impedance inverting input of the error amplifier.

COMP – The output of the error amplifier.

CS – A resistor connected from this pin to a current sense voltage programs the amount of slope compensation ramp and feeds this current sense voltage to the PWM comparator. A leading edge blanking of 100ns is provided. Voltage of 0.6V at this pin triggers the current limit comparator.

Functional Block Diagram



Functional Description

HIGH VOLTAGE REGULATOR

When DC voltage from 12 to 250V is applied to the V_{IN} pin, an internal high voltage linear regulator provides a regulated output voltage of 9.3V at the V_{DD} pin. This voltage can be used to start the DC/DC converter. Applying external voltage to the V_{DD} pin that is higher than its output voltage will disable the regulator. Therefore, the V_{IN} pin will draw negligible current once the DC/DC converter has started, and a "bootstrap" voltage has developed at the V_{DD} pin. Alternatively, the high voltage regulator can continuously supply bias current up to 20mA powering the gate driver and all internal circuits of HV9608. The need for a bootstrap power supply would be eliminated in this case. However, caution must be taken to maintain the HV9608 within its package power dissipation limits.

The output of the linear regulator is equipped with an under voltage protection comparator that disables all internal circuits when the voltage at the V_{DD} pin falls below 7.62V. Hysteresis of 0.76V is provided.

INPUT UNDER VOLTAGE LOCKOUT (UVLO)

The HV9608 provides a programmable under voltage protection input (UVLO pin) that allows independent setting of the turn-on and the turn-off limits for the input voltage of the DC/DC converter.
When the voltage applied to the UVLO pin exceeds 1.135V, the gate driver and the reference voltage at the V_{REF} pin are enabled, and the DC/DC converter starts switching. At the same time, a current of 14µA is sourced from the UVLO pin. This current sets the hysteresis that can be calculated in accordance with the following equation:

$$\Delta V_{UVLO} = 14\mu A \cdot \frac{R_1 \cdot R_2}{R_1 + R_2},$$

where R_1 and R_2 are the input voltage divider resistors.

OSCILLATOR FREQUENCY

The switching frequency of the HV9608 can be programmed using a single resistor connected to the R_T pin:

$$R_T = \frac{\left(\frac{1}{F_{OSC}[Hz]} - 300 \cdot 10^{-9} \right)}{C_T[F]}$$

SOFT START

As soon as the voltage at the V_{DD} pin exceeds the turn-on threshold, a 7µA current is sourced from the SS pin into an external soft-start capacitor C_{SS}. As the voltage across C_{SS} ramps up linearly, the output of the error amplifier (COMP) gradually increases until regulation of the output voltage is achieved. Sizing C_{SS} programs the time duration of the soft start mode. When C_{SS} is sized properly, no overshoot of the output voltage or excessive input inrush current will occur. When the voltage at the V_{DD} pin falls below the under voltage protection threshold, C_{SS} is rapidly discharged to zero.

SLOPE COMPENSATION

The HV9608 PWM controller uses an internal slope compensation scheme that is externally programmable by appropriately selecting two resistors $\mathbf{R_{SC1}}$ and $\mathbf{R_{CS2}}$. The slope compensation ramp generated at the CS pin can be calculated as:

$$\mathbf{m_{SC}}\left[\mathbf{V}/\mu\mathbf{s}\right] = 5.7 \cdot 10^{-6} \cdot \mathbf{F_{OSC}}\left[\mathbf{Hz}\right] \cdot \frac{\mathbf{R_{SC2}}}{\mathbf{R_{SC1}}}$$

$\mathbf{R_{SC1}}$ must be selected greater than 5 kΩ.

When a current sense RC filter is needed at the SC pin, the value of $\mathbf{R_{CS2}}$ will be dictated by the filter capacitor and the corner frequency of the filter. The filter capacitor externally connected to the CS pin is discharged prior to each switching cycle. It is not recommended to use a capacitor larger than 220pF for this reason.

GATE DRIVE OUTPUTS

The HV9608 provides two gate-drive outputs that are configured for driving a low-side clamp DC-DC converter, having a main switching N-channel MOSFET (Q_1) and an auxiliary active clamp P-channel MOSFET (Q_2). The GATE output is designed to drive the main N-channel MOSFET Q_1, while the AGATE output drives Q_2 via a negative output charge pump circuit C_4, D_1, R_5. Delays between the leading and the trailing edges of the gate drive outputs can be programmed using external resistors $\mathbf{R_{DT1}}$ and $\mathbf{R_{DT2}}$ connected to the DT1 and DT2 pins, respectively. The values of $\mathbf{R_{DT1}}$ and $\mathbf{R_{DT2}}$ can be calculated according to the following equations:

$$\mathbf{R_{DT1}} = 8 \times 10^{11} \cdot \mathbf{d_1}\left[\mathbf{s}\right], \qquad \mathbf{R_{DT2}} = 8 \times 10^{11} \cdot \mathbf{d_2}\left[\mathbf{s}\right],$$

where $\mathbf{d_1}$ is the leading edge delay, $\mathbf{d_2}$ is the trailing edge delay. (Refer to Fig. 2.)

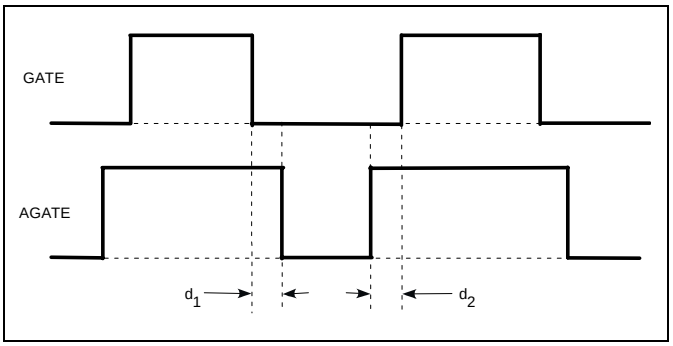


Figure 2. Gate Drive Output timing diagram.

VOLT-SECOND CLAMP

The duty cycle of the active DC-DC converter may become very large during load transients. This condition may cause saturation of the power transformer or excessive voltage stress at the clamp capacitor C_3, potentially damaging for all switching devices. In order to prevent this condition, the HV9608 includes a volt-second clamp circuit that can be programmed to limit the maximum duty cycle of the PWM controller, which is inversely proportional to the input voltage of the DC-DC converter. The maximum duty cycle D_{MAX} is set by merely connecting a single resistor R_{VS} between the positive input terminal of the converter and the VS pin. R_{VS} can be calculated with the following equation.

$$R_{VS} = 1.72 \times 10^{9} \cdot \left(V_{IN}\left[V\right] - 0.7\right) \cdot \left(\frac{D_{MAX}}{F_{OSC}\left[Hz\right]} + d_1\left[s\right] + 2 \times 10^{-8}\right)$$

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