ISL9113

Low Input Voltage and High Efficiency Synchronous Boost Converter with 1.3A Switch

FN8313
Rev 3.00
February 23, 2015

The ISL9113 provides a power supply solution for devices powered by three-cell alkaline, NiCd, NiMH or one-cell Li-Ion/Li-Polymer batteries. It offers either a fixed 5V or an adjustable output option for USB-OTG or portable HDMI applications. The device is guaranteed to supply 500mA from a 3V input and 5V output and has a typical 1.3A peak current limit. High 1.8MHz switching frequency allows for the use of tiny, low-profile inductors and ceramic capacitors to minimize the size of the overall solution.

The ISL9113 is an internally compensated, fully integrated synchronous converter optimized for efficiency with minimal external components. At light load, the device enters skip mode and consumes only 20µA of quiescent current, resulting in higher efficiency at light loads and maximum battery life.

The device is available in an 8 Ld DFN package and a 6 bump WLCSP.

Related Literature

- AN1816, "ISL9113ERAZ-EVZ, ISL9113ER7Z-EVZ Evaluation Board User Guide"

Features

- Up to 95% efficiency at typical operating conditions
- Input voltage range: 0.8V to 4.7V
- Output current: Up to 500mA (V_{BAT} = 3.0V, V_{OUT} = 5.0V)
- Low quiescent current: 20µA (typical)
- Logic control shutdown (I_Q < 1µA)
- Fixed 5V, 5.1V or adjustable output
- 1.2V EN high logic
- Output disconnect during shutdown
- Skip mode under light load condition
- Undervoltage lockout
- Fault protection: OVP (ADJ version only), OTP, short circuit
- 8 Ld 2mmx2mm DFN package and 6 bump 0.8mmx1.36mm WLCSP

Applications

- Products including portable HDMI and USB-OTG
- Smartphones
- Tablet and mobile internet devices

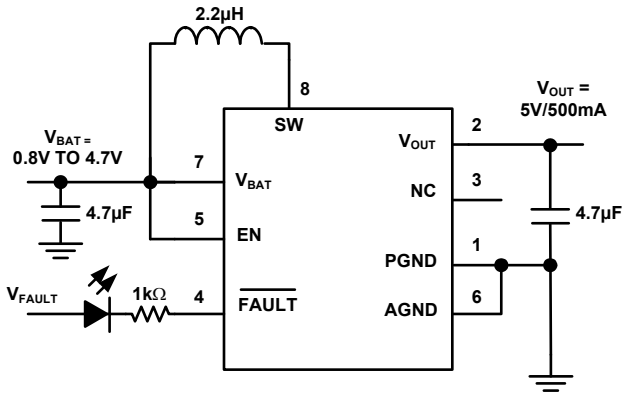


FIGURE 1. TYPICAL APPLICATION (ISL9113ER7Z)

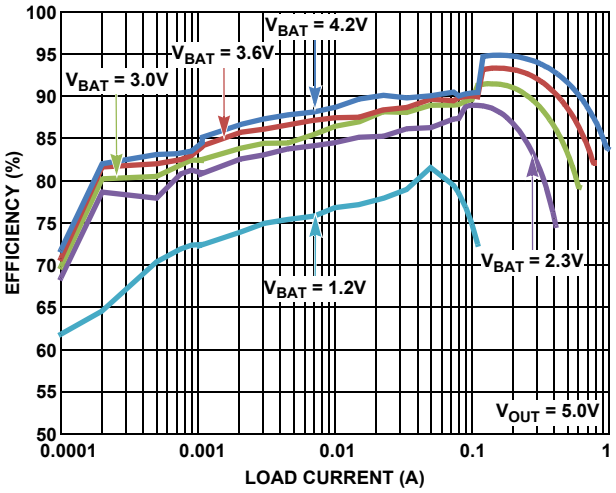
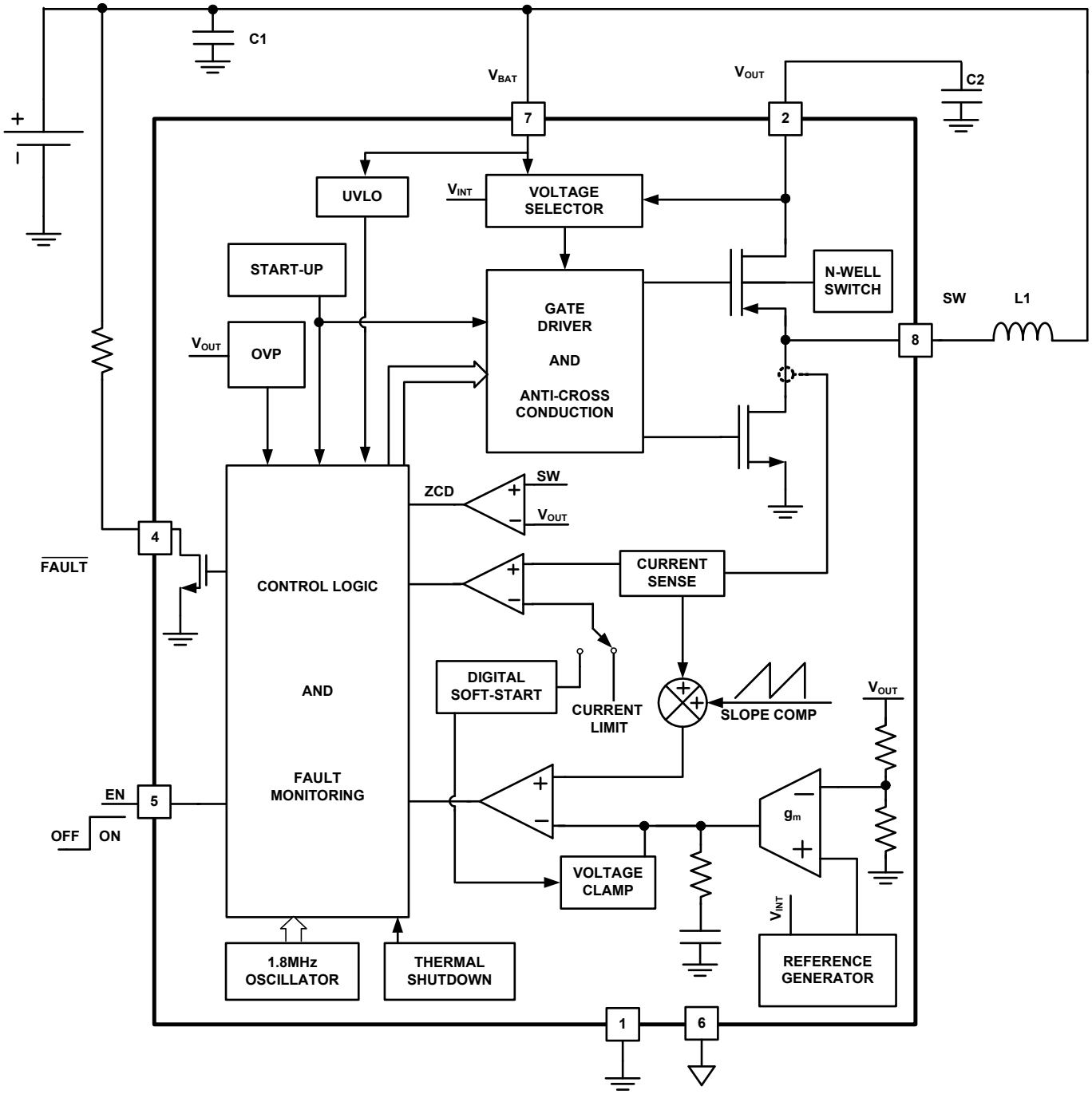


FIGURE 2. FIXED 5V EFFICIENCY (ISL9113ER7Z)

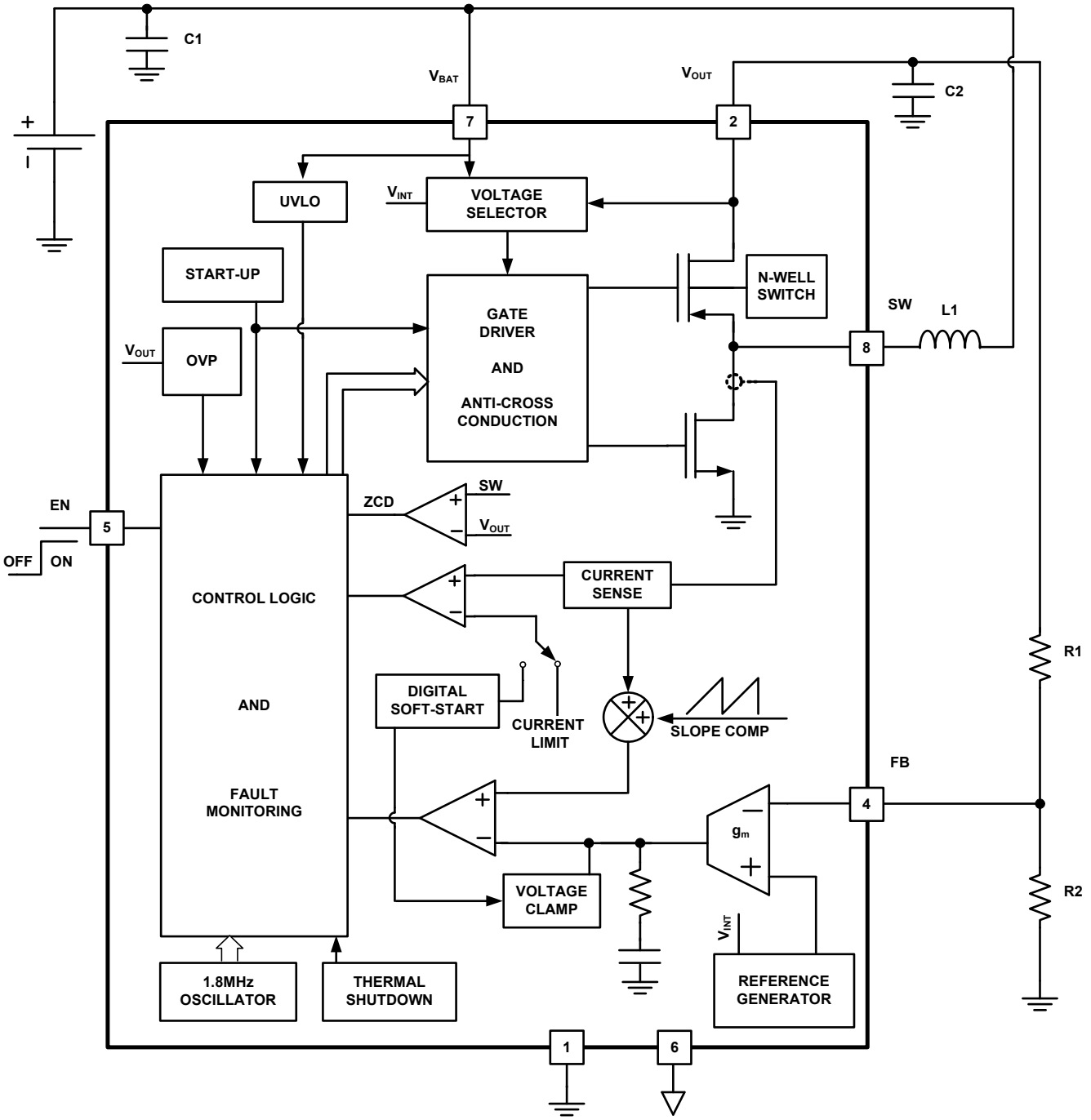
Block Diagrams

ISL9113ER7Z



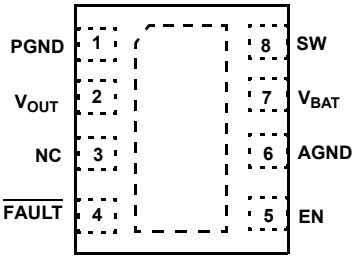
Block Diagrams (Continued)

ISL9113ERAZ

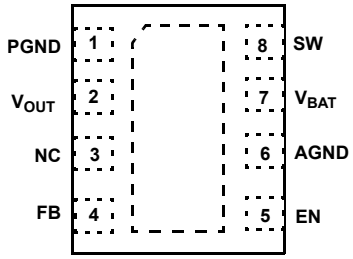


Pin Configurations

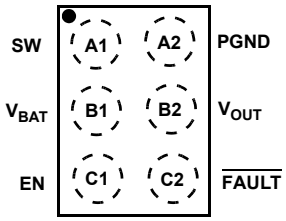
FIXED OUTPUT
(8 LD DFN)
TOP VIEW



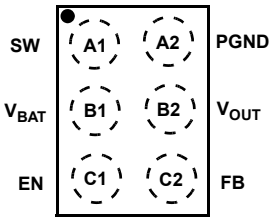
ADJUSTABLE OUTPUT
(8 LD DFN)
TOP VIEW



FIXED OUTPUT
(6 BUMP WLCSP)
TOP VIEW



ADJUSTABLE OUTPUT
(6 BUMP WLCSP)
TOP VIEW



Pin Descriptions

8 LD DFN PIN NUMBERS		6 BUMP WLCSP PIN NUMBERS		SYMBOL	PIN DESCRIPTIONS
FIXED OUTPUT	ADJUSTABLE OUTPUT	FIXED OUTPUT	ADJUSTABLE OUTPUT		
1	1	A2	A2	PGND	Power ground
2	2	B2	B2	V_{OUT}	Device output
3	3	-	-	NC	No connection
4	-	C2	-	$\overline{FAULT}$	Fault output; outputs logic LOW under a number of fault conditions (see Table 1 on page 9).
-	4	-	C2	FB	Feedback pin of the converter. Connect voltage divider resistors between V_{OUT}, FB and GND for desired output.
5	5	C1	C1	EN	The EN pin is an active-HIGH logic input for enabling the device. When asserted HIGH, the boost function begins. When asserted LOW, the device is completely disabled, and current is blocked from flowing from the SW pin to the output and vice versa. This pin should be tied either HIGH to enable the device, or LOW to disable the device.
6	6	-	-	AGND	Analog ground
7	7	B1	B1	V_{BAT}	Device input supply from a battery. Connect a 4.7µF ceramic capacitor to the power ground.
8	8	A1	A1	SW	The SW pin is the switching node of the power converter. Connect one terminal of the inductor to the SW pin and the other to power input.
		-	-	EPAD	The exposed pad (available only in the 8 Ld DFN package) must be connected to PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the system GND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 4)	PART MARKING	V_{OUT} (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL9113ER7Z-T (Note 2)	137	5.0	-20 to +85	8 Ld DFN	L8.2x2D
ISL9113ERAZ-T (Note 2)	13A	Adjustable	-20 to +85	8 Ld DFN	L8.2x2D
ISL9113EI9Z-T (Note 3)	139	5.1	-20 to +85	6 Bump WLCSP	W3x2.6
ISL9113EIAZ-T (Note 3)	13A	Adjustable	-20 to +85	6 Bump WLCSP	W3x2.6
ISL9113ER7Z-EVZ	Evaluation Board for ISL9113ER7Z				
ISL9113ERAZ-EVZ	Evaluation Board for ISL9113ERAZ				
ISL9113EI9Z-EVZ	Evaluation Board for ISL9113EI9Z				
ISL9113EIAZ-EVZ	Evaluation Board for ISL9113EIAZ				

NOTES:

1. Please refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL9113. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

V_{BAT}, EN, $\overline{FAULT}$, V_{OUT}, FB . . . . . -0.3V to 6.5V
SW Voltage
DC . . . . . -0.5V to 6.5V
Pulse < 10ns . . . . . -0.5V to 8.0V
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 3kV
*Other ESD Spec should meet Level 1 requirement
Latch-up (Tested per JESD78; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 5, 6)	80	15
6 Bump WLCSP (Note 5)	116	-

Junction Temperature Range . . . . . -20°C to +125°C
Operating Temperature Range . . . . . -20°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{BAT} (After Start-up) . . . . . 0.8V to 4.7V
V_{OUT} . . . . . (V_{BAT} + 0.2V) to 5.2V
Ambient Temperature Range . . . . . -20°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC} the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{BAT} = 3.0V, V_{OUT} = 5.0V, T_A = +25°C (see "Typical Application Circuit" on page 7). **Boldface limits apply across the operating temperature range, -20°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Start-up Voltage	V_{MIN}	V_{EN} = 1.2V, R_{LOAD} = 50Ω	**2.8**	3.0		V
Input Undervoltage Lockout	V_{UVLO}	V_{EN} = V_{BAT}, R_{LOAD} = 50Ω, DFN versions only	**0.68**	0.70	**0.76**	V
Feedback Voltage	V_{FB}	ADJ version only	**784**	800	**816**	mV
Output Voltage	V_{OUT}	V_{BAT} = 2.8V, ADJ version only	**3.0**		**5.2**	V
		I_{LOAD} = 50mA, 5V DFN Fixed version	**4.9**	5	**5.1**	V
		I_{LOAD} = 1mA or 50mA, 5.1V WLCSP Fixed version	**4.96**	5.1	**5.2**	V
Feedback Pin Input Current		V_{FB} = 0.8V, ADJ version only			**100**	nA
Quiescent Current from V_{OUT}	I_{Q1}	V_{BAT} = V_{EN} = 1.2V, No Load (Note 8)		20	**45**	µA
Shutdown Current from V_{BAT}	I_{SD}	V_{EN} = 0V, V_{BAT} = 1.2V, V_O = 0		0.5	2	µA
Leakage Current at SW Pin		V_{EN} = 0V, V_{BAT} = 4.7V, V_O = 0			1	µA
N-Channel MOSFET ON-resistance				0.20		Ω
P-Channel MOSFET ON-resistance				0.35		Ω
N-Channel MOSFET Peak Current Limit	I_{PK}		**1.1**	1.3	**1.5**	A
Maximum Duty Cycle	D_{MAX}		**85**	87.5		%
PWM Switching Frequency	F_{OSC}	DFN version	**1.5**	1.8	**2.0**	MHz
		WLCSP version	**1.7**	1.8	**2.2**	MHz
EN Logic High		2.5V < V_{BAT} < 4.7V	**1.2**			V
		V_{BAT} < 2.5V	**0.48*V_{BAT}**			V
EN Logic Low		2.5V < V_{BAT} < 4.7V			**0.35**	V
		V_{BAT} < 2.5V			**0.14*V_{BAT}**	V
Soft-Start-Up Time		C_{OUT} = 4.7µF, L = 2.2µH		0.2	1	ms

Electrical Specifications V_{BAT} = 3.0V, V_{OUT} = 5.0V, T_A = +25°C (see "Typical Application Circuit" on page 7). **Boldface limits apply across the operating temperature range, -20°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
$\overline{FAULT}$ Pin Leakage Current when High		V_{FAULT} = V_{OUT}			**100**	nA
$\overline{FAULT}$ Pin Sink Current when Low		V_{FAULT} = 0.5V	**10**			mA
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	I_{LOAD} = 0 to 100mA, DFN versions	**-1.5**		**+1.5**	%
		I_{LOAD} = 0 to 100mA, WLCSP versions		±1.5		%
Line Regulation		V_{BAT} = 3.0V to 3.6V, I_{LOAD} = 1mA	**-1.0**		**+1.0**	%
Output Overvoltage Protection Threshold		ADJ version only		5.9		V
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. I_{Q1} is measured at V_{OUT} and multiplied by V_{OUT}/V_{BAT}; thus, the equivalent input quiescent current is calculated.

Typical Application Circuit

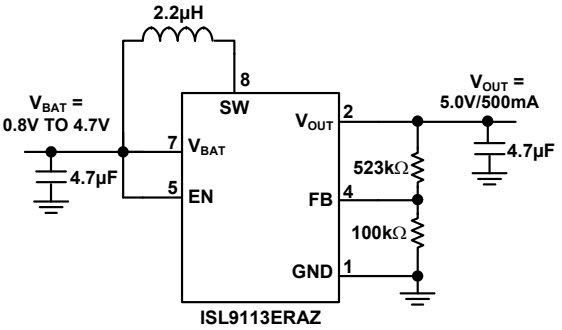


FIGURE 3. POWER SUPPLY SOLUTION FOR V_{OUT} = 5V

Detailed Description

Current Mode PWM Operation

The control scheme of the device is based on the peak current mode control and the control loop is compensated internally. The peak current of the N-channel MOSFET switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical current limit is set to 1.3A.

The control circuit includes a ramp generator, slope compensator, error amplifier and a PWM comparator (see "Block Diagrams" on pages 2 and 3). The ramp signal is derived from the inductor current. This ramp signal is then compared to the error amplifier output to generate the PWM gating signals for driving both N-channel and P-channel MOSFETs. The PWM operation is initialized by the clock from the internal oscillator (typical 1.8MHz). The N-channel MOSFET is turned ON at the beginning of a PWM cycle, the P-channel MOSFET remains OFF and the current starts ramping up. When the sum of the ramp and the slope compensator output reaches the error amplifier output voltage, the PWM comparator outputs a signal to turn OFF the N-channel MOSFET. Here, both MOSFETs remain OFF during the dead-time interval. Next, the P-channel MOSFET is turned ON and remains ON until the end of this PWM cycle. During this time, the inductor current ramps down until the next clock. At this point, following a short dead time, the N-channel MOSFET is again turned ON, repeating as previously described.

Skip Mode Operation

The boost converter is capable of operating in two different modes. When the inductor current is sensed to cross zero for eight consecutive times, the converter enters skip mode. In skip mode, each pulse cycle is still synchronized by the PWM clock. The N-channel MOSFET is turned ON at the rising edge of the clock and turned OFF when the inductor peak current reaches typically 25% of the current limit. Then, the P-channel MOSFET is turned ON, and it stays ON until its current goes to zero. Subsequently, both N-channel and P-channel MOSFETs are turned OFF until the next clock cycle starts, at which time the N-channel MOSFET is turned ON again. When V_{OUT} is 1.5% higher than the nominal output voltage, the N-channel MOSFET is immediately turned OFF and the P-channel MOSFET is turned ON until the inductor current goes to zero. The N-channel MOSFET resumes operation when V_{FB} falls back to its nominal value, repeating the previous operation. The converter returns to 1.8MHz PWM mode operation when V_{FB} drops 1.5% below its nominal voltage.

Given the skip mode algorithm incorporated in the ISL9113, the average value of the output voltage is approximately 0.75% higher than the nominal output voltage under PWM operation. This positive offset improves the load transient response when switching from skip mode to PWM mode operation. The ripple on the output voltage is typically 1.5%*V_{OUT} (nominal) when input voltage is sufficiently lower than output voltage, and it increases as the input voltage approaches the output voltage.

Synchronous Rectifier

The ISL9113 integrates one N-channel MOSFET and one P-channel MOSFET to realize a synchronous boost converter. Because the commonly used discrete Schottky rectifier is replaced with the low $r_{DS(ON)}$ P-channel MOSFET, the power conversion efficiency reaches a value above 90%. Since a typical step-up converter has a conduction path from the input to the

output via the body diode of the P-channel MOSFET, a special circuit (see “Block Diagrams” on pages 2 and 3) is used to reverse the polarity of the P-channel body diode when the device is shut down. Thus, this configuration completely disconnects the load from the input during shutdown of the converter. The benefit of this feature is that the battery will not be completely depleted during shutdown of the converter. No additional components are needed to disconnect the battery from the output of the converter.

Soft-Start

The soft start-up duration is the time between the device being enabled and V_{OUT} rising to within 3% of target voltage. When the device is enabled, the start-up cycle starts with a linear phase. During the linear phase, the rectifying switch is turned ON in a current limited configuration, delivering about 350mA, until the output capacitor is charged to approximately 90% of the input voltage. At this point, PWM operation begins in boost mode. If the output voltage is below 2.3V, PWM switching is done at a fixed duty-cycle of 75% until the output voltage reaches 2.3V. When the output voltage exceeds 2.3V, the closed-loop current mode PWM loop overrides the duty cycle until the output voltage is regulated. Peak inductor current is ramped to the final value (typically 1.3A) during the soft-start period to limit inrush current from the input source. Fault monitoring begins approximately 2ms after the device is enabled.

Over-temperature Protection (OTP)

The device offers over-temperature protection. A temperature sensor circuit is integrated and monitors the internal IC temperature. Once the temperature exceeds the preset threshold (typically +150°C), the IC shuts down immediately. The OTP has a typical hysteresis of +25°C. When the device temperature decreases by this, the device starts operating.

Fault Monitoring and Reporting

Fault monitoring starts 2ms after start-up. Table 1 shows the response to different detected faults. Any fault condition shown in Table 1 causes the $\overline{FAULT}$ pin to be taken LOW. The $\overline{FAULT}$ pin will not release until V_{BAT} and V_{OUT} fully collapse or until the fault condition is removed.

Printed Circuit Board Layout Recommendations

The ISL9113 is a high frequency switching boost converter. Accordingly, the converter has fast voltage change and high switching current that may cause EMI and stability issues if the layout is not done properly. Therefore, careful layout is critical to minimize the trace inductance and reduce the area of the power loop.

Power components, such as input capacitor, inductor and output capacitor, should be placed close to the device. Board traces that carry high switching current should be routed wide and short. A solid power ground plane is important for EMI suppression.

The switching node (SW pin) of the converter and the traces connected to this pin are very noisy. Noise sensitive traces, such as the FB trace, should be kept away from SW node. The voltage divider should be placed close to the FB pin to prevent noise pickup. Figures 4 and 5 show the recommended PCB layout.

In the 8 Ld DFN package, the heat generated in the device is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. It is recommended to add at least 4 vias within the pad to the GND plane for the best thermal relief.

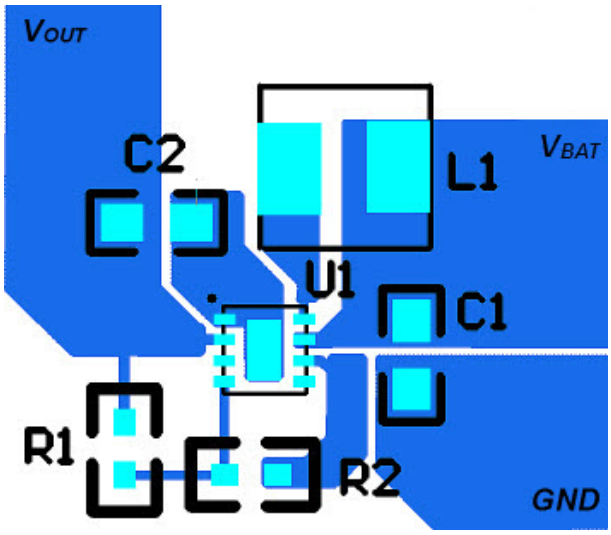


FIGURE 4. RECOMMENDED PCB LAYOUT (DFN VERSION)

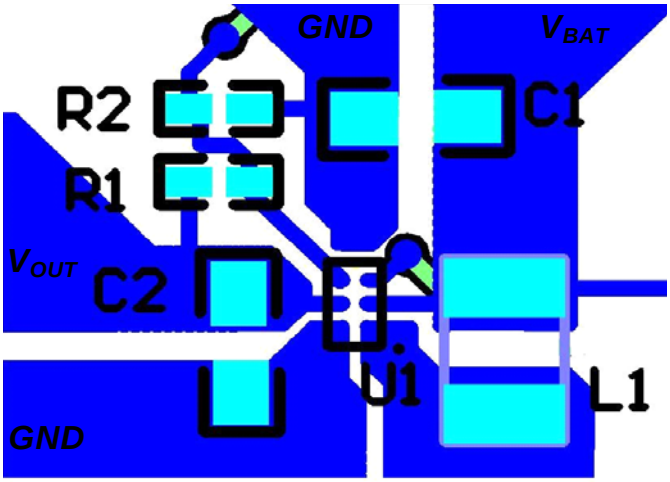


FIGURE 5. RECOMMENDED PCB LAYOUT (WLCSP VERSION)

Fixed and Adjustable Output Voltage

ISL9113 offers options for fixed output voltage of 5V, 5.1V or an adjustable output voltage.

For the fixed output voltage version (ISL9113ER7Z, ISL9113EI9Z-T), an internal voltage divider is used (see “Block Diagrams”, “ISL9113ER7Z” on page 2). For the adjustable output voltage version (ISL9113ERAZ), the output voltage is programmed by connecting two external voltage divider resistors between V_{OUT}, FB and GND (see “Block Diagrams”, “ISL9113ERAZ” on page 3).

TABLE 1. FAULT DETECTION AND RESPONSE

FAULT CONDITION	DETECTION DETAILS	ACTION
Low Battery Voltage	V_{BAT} < 0.7V	Shut down until V_{EN} or V_{BAT} is cycled.
V_{OUT} out of Regulation	V_{OUT} is 10% below the target output voltage	Shut down only if V_{BAT} and V_{OUT} fall below 2.1V. Device automatically restarts after 200ms. $\overline{FAULT}$ signal switches ON and OFF when V_{OUT} drops out of regulation due to overload condition.
Short Circuit	V_{OUT} falls below V_{BAT}	Shut down immediately. Device automatically restarts after 200ms.
Over-temperature Protection	Die temperature is > +150°C	Switching stops. Device automatically restarts when temperature decreases to +125°C.
Output Overvoltage Protection (ADJ version only)	V_{OUT} > 5.9V	Switching stops until EN pin is toggled or power is cycled.

Output Voltage Setting Resistor Selection

For the ISL9113 adjustable output version, resistors R_1 and R_2, shown in the Block Diagram "ISL9113ERAZ" on page 3, set the desired output voltage values. The output voltage can be calculated using Equation 1:

$$V_{OUT} = V_{FB} \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

where V_{FB} is the internal FB reference voltage (0.8V typical). The current flowing through the divider resistors is calculated as $V_{OUT}/(R_1 + R_2)$. Large resistance is recommended to minimize current into the divider and thus improve the total efficiency of the converter. R_1 and R_2 should be placed close to the FB pin of the device to prevent noise pickup.

Inductor Selection

An inductor with core material suitable for high frequency applications (e.g., ferrite) is desirable to minimize core loss and improve efficiency. The inductor should have a low ESR to reduce copper loss. Moreover, the inductor saturation current should be higher than the maximum peak current of the device; i.e., 1.5A.

The device is designed to operate with an inductor value of 2.2µH to provide stable operation across the range of load, input and output voltages. Stable mode switching between PWM and skip mode operation is guaranteed at this inductor value. Table 2 shows recommended inductors.

TABLE 2. INDUCTOR VENDOR INFORMATION

MANUFACTURER	PART NUMBER	DIMENSIONS- W x L x H (mm)
Murata	LQH32PN2R2NN0L	3.2 x 2.5 x 1.7(max)
Toko	1239AS-H-2R2M	2.5 x 2.0 x 1.2(max)
	1286AS-H-2R2M	2.0 x 1.6 x 1.2(max)
TDK	TFM201610A-2R2M	2.0 x 1.6 x 1.0(max)
Cyntec	PSE25201B-2R2MS	2.0 x 1.6 x 1.2(max)

Capacitor Selection

INPUT CAPACITOR

A minimum of a 4.7µF ceramic capacitor is recommended to provide stable operation under typical operating conditions. For input voltage less than 1.0V application, an additional 4.7µF ceramic capacitor is recommended for better noise filtering and EMI suppression. The input capacitor should be placed close to the input pin, GND pin and the non-switching terminal of the inductor.

OUTPUT CAPACITOR

For the output capacitor, a ceramic capacitor with small ESR is recommended to minimize output voltage ripple. A typical 4.7µF should be used to provide stable operation at different typical operating conditions. The output capacitor should be placed close to the output pin and GND pin of the device. Table 3 shows the recommended capacitors.

TABLE 3. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Typical Characteristics

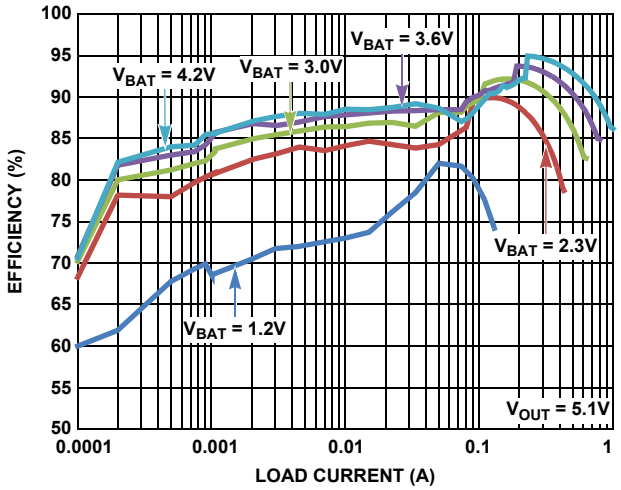


FIGURE 6. FIXED 5.1V EFFICIENCY (ISL9113EI9Z)

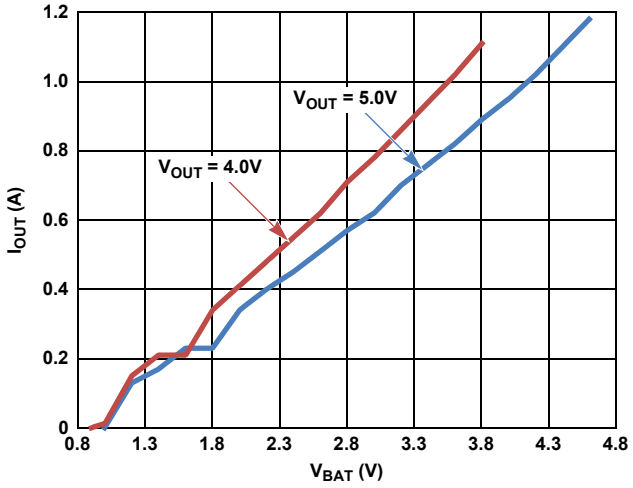


FIGURE 7. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE (ISL9113ERAZ)

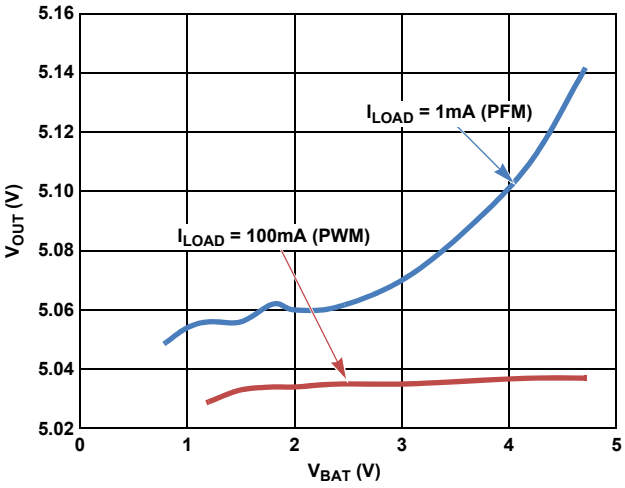


FIGURE 8. LINE REGULATION, V_{OUT} = 5V (ISL9113ER7Z)

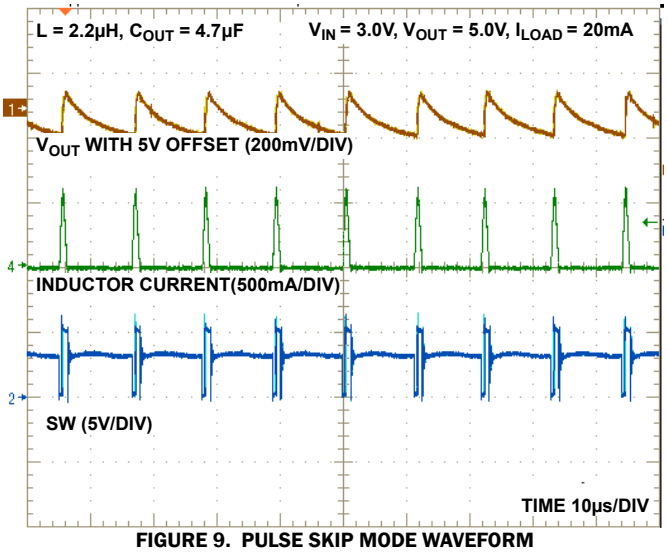


FIGURE 9. PULSE SKIP MODE WAVEFORM

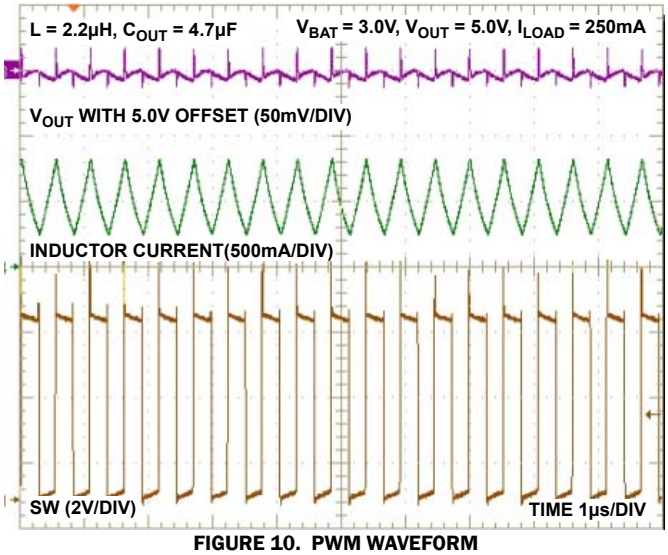


FIGURE 10. PWM WAVEFORM

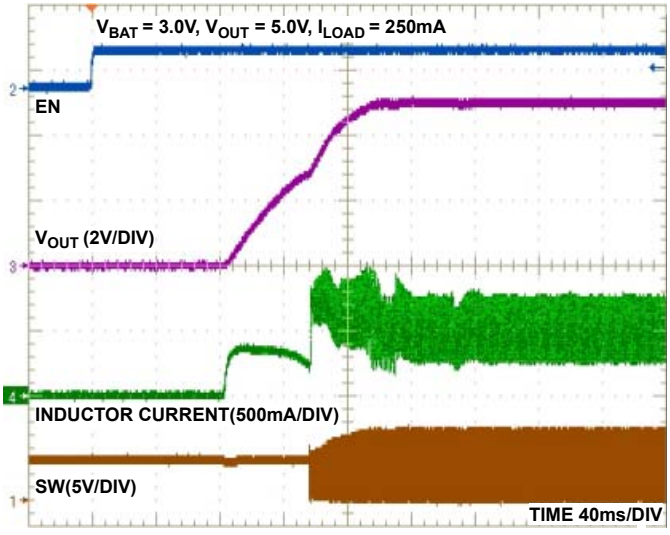


FIGURE 11. START-UP AFTER ENABLE (I_{LOAD} = 250mA)

Typical Characteristics (Continued)

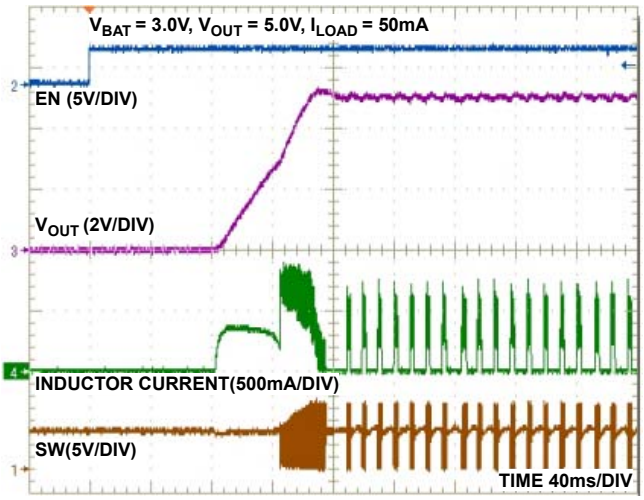


FIGURE 12. START-UP AFTER ENABLE (I_{LOAD} = 50mA)

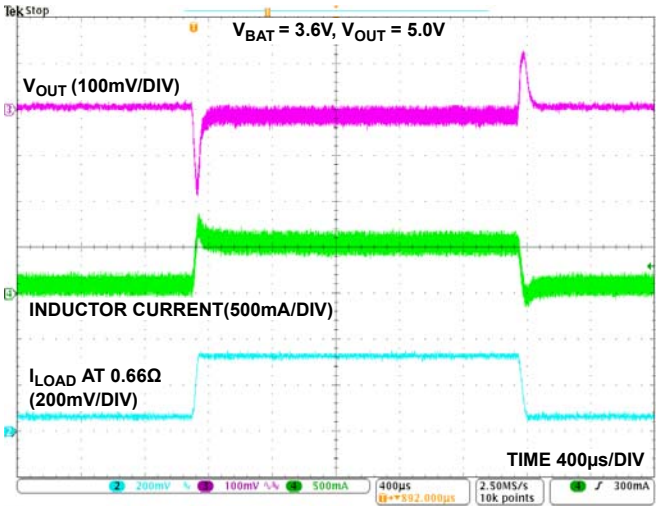


FIGURE 13. LOAD TRANSIENT RESPONSE (100mA TO 500mA)

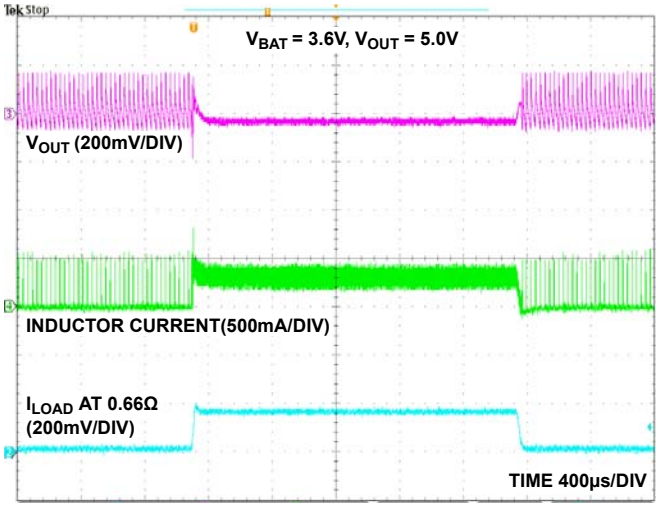


FIGURE 14. LOAD TRANSIENT RESPONSE (20mA TO 250mA)

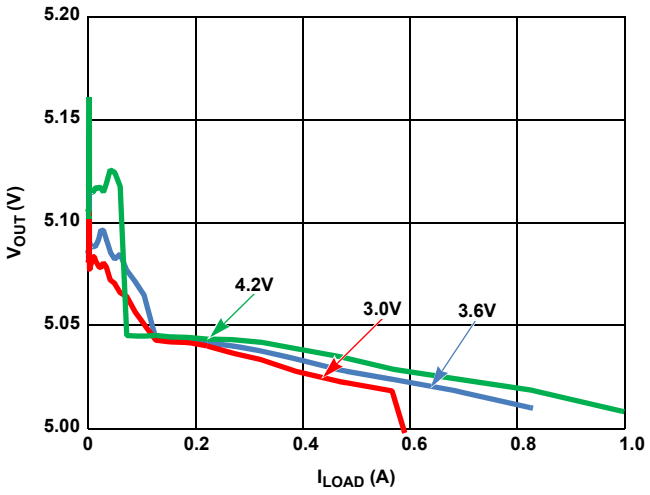


FIGURE 15. LOAD REGULATION (ISL9113ER7Z)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 23, 2015	FN8313.3	Updated Datasheet with Intersil new standards. On page 6, under the“Absolute Maximum Ratings” section added “FB” to the first line. Replaced Figure 9 on page 10. Updated the About Intersil verbiage.
February 18, 2013	FN8313.2	Page 1: Added 5.1V or Adjustable Output options to “Features” Removed "Coming Soon" from WLCSP package references Updated Figure 2. Changed y axis scale Page 5: Added information for WLCSP package option. Page 6: Removed Machine Model from “ESD Ratings”. Added “Thermal Information” for WLCSP. “Electrical Specifications” on page 6: “Input Undervoltage Lockout”, aded "DFN versions only" to test conditions. Changed parameter name from “Output Voltage Accuracy” to “Output Voltage”. Added "5V DFN Fixed version" to test conditions where I_{LOAD} = 50mA. Changed MIN/MAX from -100/+100 mV to 4.9/5.1 V. Added TYP. Added lines for ADJ version only and WLCSP Fixed version. Added "ADJ version only" to test conditions for “Feedback Voltage”. Added test conditions for “Feedback Pin Input Current”. Added WLCSP specs for “PWM Switching Frequency”. “Electrical Specifications” on page 7: Added "DFN versions" to test conditions for “Load Regulation” where I_{LOAD} = 0 to 100mA. Added line for WLCSP versions. Added test conditions for “Output Overvoltage Protection Threshold”. Page 8: Added Figure 5 “RECOMMENDED PCB LAYOUT (WLCSP VERSION)”. Changed “Fixed and Adjustable Output Voltage” from: “ISL9113 offers options for fixed output voltage of 5V or an adjustable output voltage. For fixed output voltage version (ISL9113ER7Z)..” to: “ISL9113 offers options for fixed output voltage of 5V, 5.1V, or an adjustable output voltage. For fixed output voltage version (ISL9113ER7Z, ISL9113EI9Z-T)..” Revised Table 2. Added dimensions. Revised Manufacturers and Part Numbers. Added new efficiency plot, Figure 6. Added “W3x2.6” on page 15.
January 16, 2013	FN8313.1	Updated Related Literature on page 1. Changed ESD Ratings in “Absolute Maximum Ratings” on page 6 as follows: HBM from 2.5kV to 3kV MM from 250V to 300V
July 12, 2012	FN8313.0	Initial Release.

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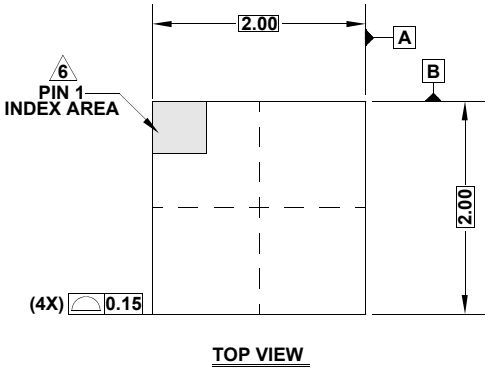
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

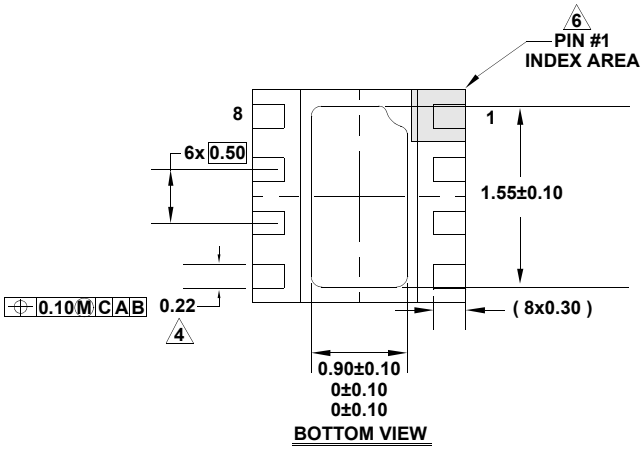
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

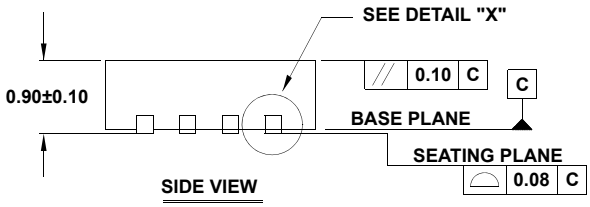
Rev 0, 3/11



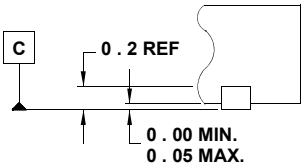
TOP VIEW



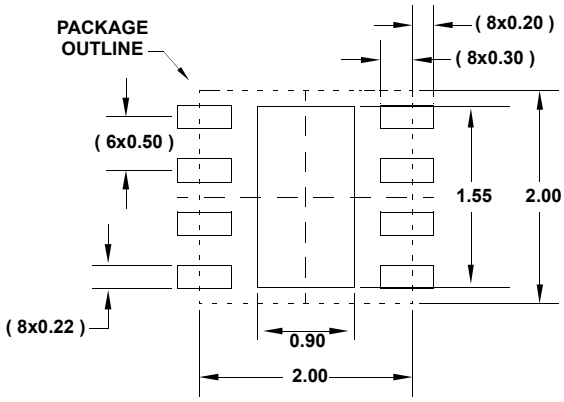
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

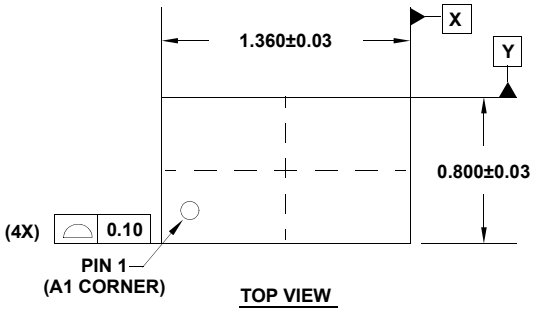
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

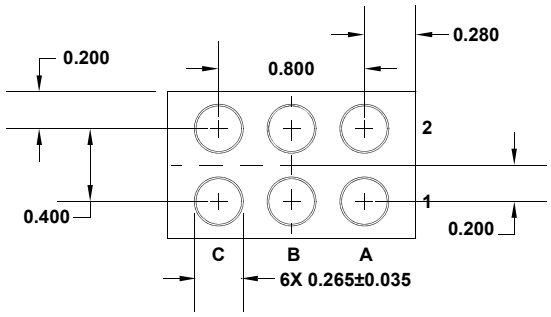
W3x2.6

3X2 ARRAY 6 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLSCP 0.4MM PITCH)

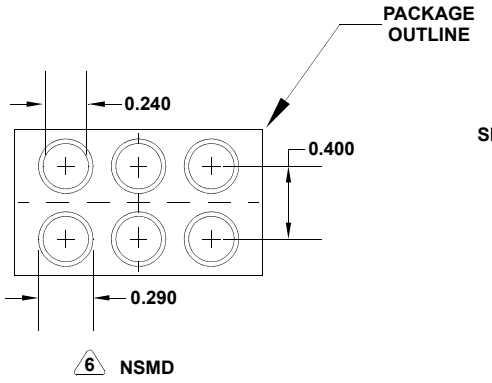
Rev 3, 1/13



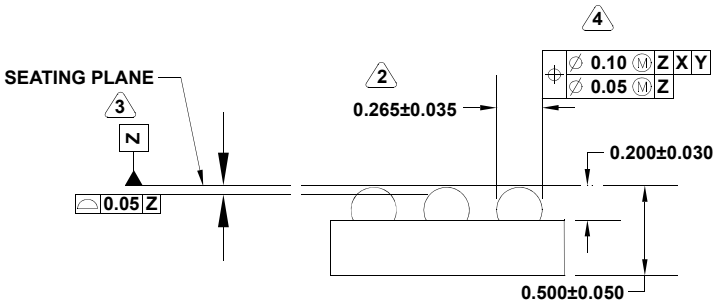
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. All dimensions are in millimeters.
6. NSMD refers to non-solder mask defined pad design per Intersil Tech Brief www.intersil.com/data/tb/tb451.pdf
7. Ball height and post saw device size can vary by ±10µm depending on final selection of assembly vendor.