FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13748-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90860E Series

MB90867E(S), MB90F867E(S), MB90V340E-101/102

■ DESCRIPTION

MB90860E-series with Flash ROM is especially designed for automotive and other industrial applications. With the new 0.35 µm CMOS technology, Fujitsu now offers on-chip Flash ROM program memory up to 512 Kbytes.

The power supply (3 V) is supplied to the internal MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features an 8 channel Output Compare Unit and 8 channel Input Capture Unit with 2 separate 16-bit free running timers. 4 UARTs constitute additional functionality for communication purposes.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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FUJITSU

■ FEATURES

- **CPU**
  - Instruction system best suited to controller
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes(23 types)
  - Enhanced multiply-divide instructions and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
  - Instruction system compatible with high-level language (C language) and multitask
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
  - Increased processing speed
  - 4-byte instruction queue
- **Serial interface**
  - UART (LIN/SCI) : up to 4 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
  - I^2C interface* : up to 2 channels
  - Up to 400 Kbits/s transfer rate
- **Interrupt controller**
  - Powerful interrupt function
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 16 external interrupts are supported
  - Automatic data transfer function independent of CPU
  - Expanded intelligent I/O service function (EI^2OS) : up to 16 channels
- **I/O port**
  - General-purpose input/output port (CMOS output)
    - 80 ports (devices without S-suffix)
    - 82 ports (devices with S-suffix)
- **8/10-bit A/D converter**
  - 8/10-bit A/D converter : 24 channels
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time : 3 μs (at 24-MHz machine clock, including sampling time)
  - Program patch function
- **Timer**
  - Time-base timer, clock timer, watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 16 channels, or 16-bit × 8 channels
  - 16-bit reload timer : 4 channels
  - 16-bit input/output timer
    - 16-bit free run timer : 2 channel
    (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
    - 16-bit input capture: (ICU) : 8 channels
    - 16-bit output compare : (OCU) : 8 channels

- **Variety of mode**
  - Low power consumption (standby) mode
  - Sleep mode (a mode that halts CPU operating clock)
  - Main timer mode (time-base timer mode that is transferred from main clock mode)
  - PLL timer mode (time-base timer mode that is transferred from PLL clock mode)
  - Watch mode (a mode that operates sub clock and clock timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode
- **Technology**
  - 0.35 μm CMOS technology

* : I²C license :
Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

Part Number / Parameter	MB90867E(S)	MB90F867E(S)	MB90V340E-101/102
CPU	F²MC-16LX CPU		
Type	MASK ROM product	Flash memory product	Evaluation product
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	MASK ROM 128 Kbytes	Flash memory 128 Kbytes	External
RAM	6 Kbytes	6 Kbytes	30 Kbytes
Emulator-specific power supply*1	—		Yes
Technology	0.35 µm CMOS with on-chip voltage regulator for internal power supply	0.35 µm CMOS with on-chip voltage regulator for internal power supply + Flash memory with on-chip charge pump for programming voltage	0.35 µm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus		5 V ± 10%
Temperature range	−40 °C to +105 °C		—
Package	QFP-100, LQFP-100		PGA-299
UART	4 channels		5 channels
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I²C (400 kbps)	2 channels		
8/10-bit A/D converter	24 channels		
	10-bit or 8-bit resolution Conversion time : Min 3 µs include sample time (per one channel)		
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function		
16-bit I/O timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (ch.0, ch.4) Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit output compare (8 channels)	Signals an interrupt when 16-bit I/O Timer match output compare registers. A pair of compare registers can be used to generate an output signal.		
16-bit input capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Signals an interrupt upon external event		

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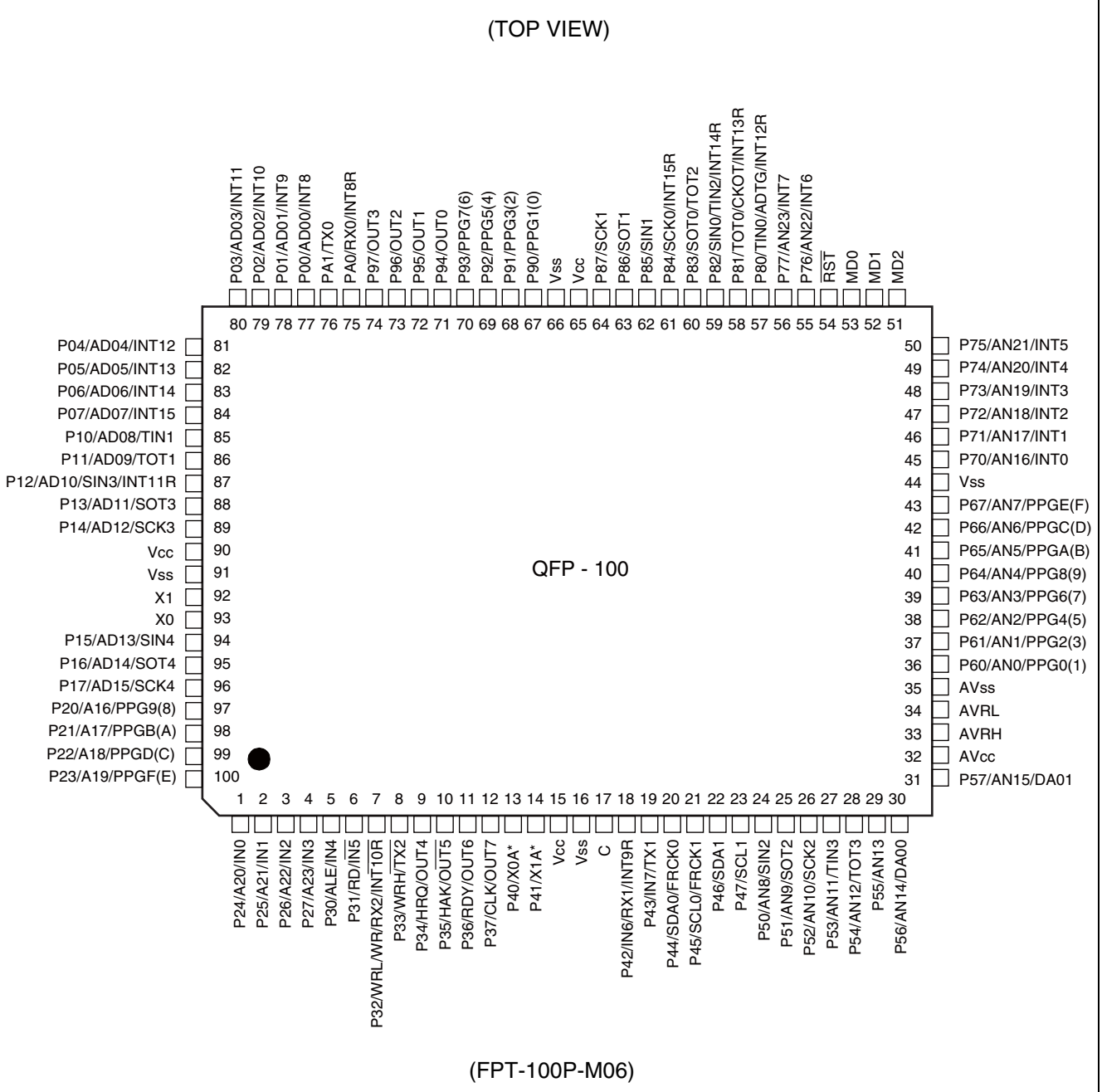
Part Number / Parameter	MB90867E(S)	MB90F867E(S)	MB90V340E-101/102
8/16-bit programmable pulse generator (8 channels)	Supports 8-bit and 16-bit operation modes Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)		
CAN interface	—		3 channels
External interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI^{2}OS) and DMA		
D/A converter	—		2 channels
Up to 100 kHz sub clock for low power operation	Devices without ‘S’-suffix		Only for MB90V340E-102
I/O ports	Virtually all external pins can be used as general purpose I/O port All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable in pin-wise of 8 as CMOS schmitt trigger/automotive inputs (default) TTL input level settable for external bus (32-pin only for external bus)		
Flash memory	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash		—

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the Emulator hardware manual about details.

*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PIN ASSIGNMENTS

- MB90V340E-101/102

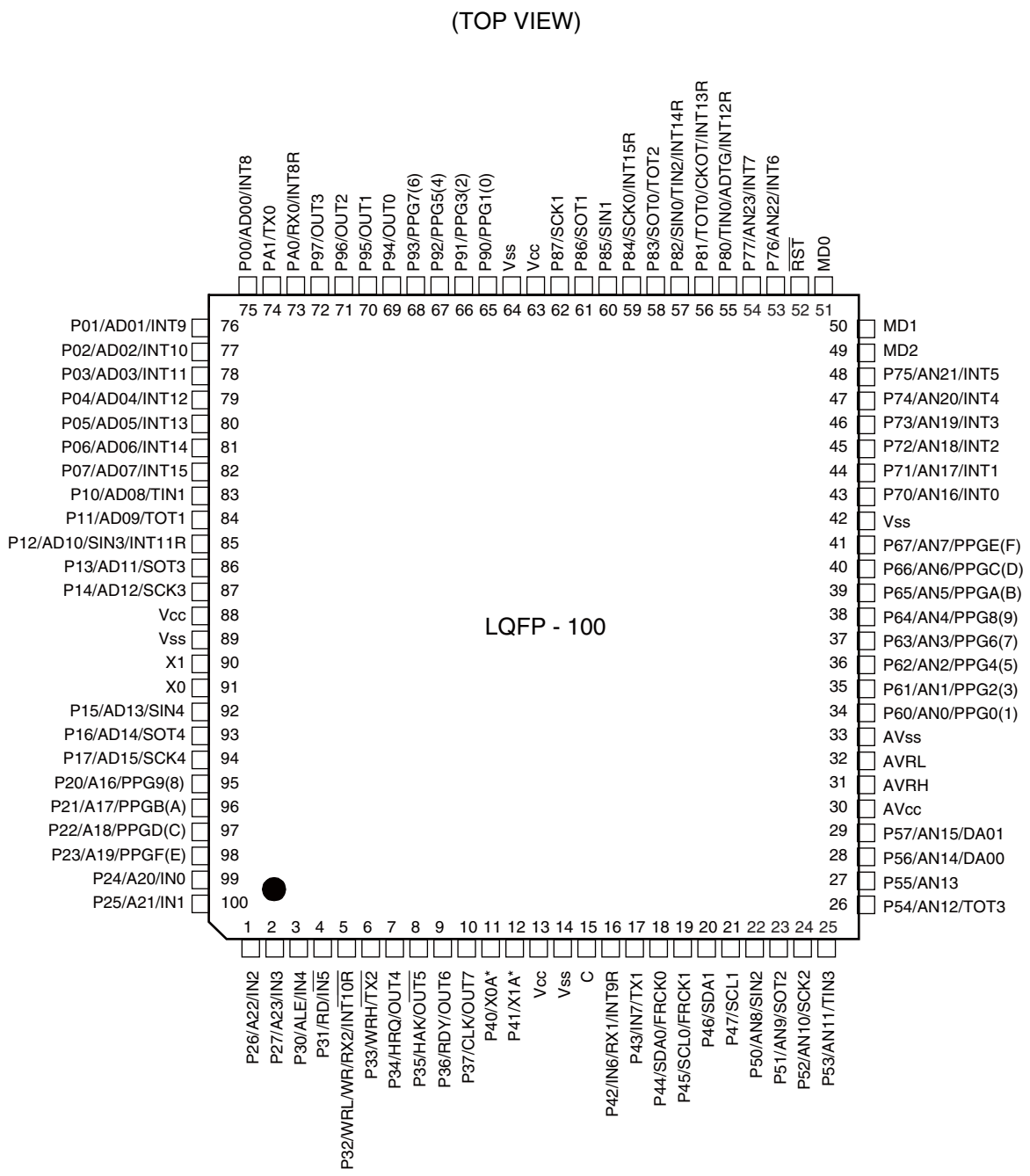


(FPT-100P-M06)

* : X0A, X1A : MB90V340E-102
P40, P41 : MB90V340E-101

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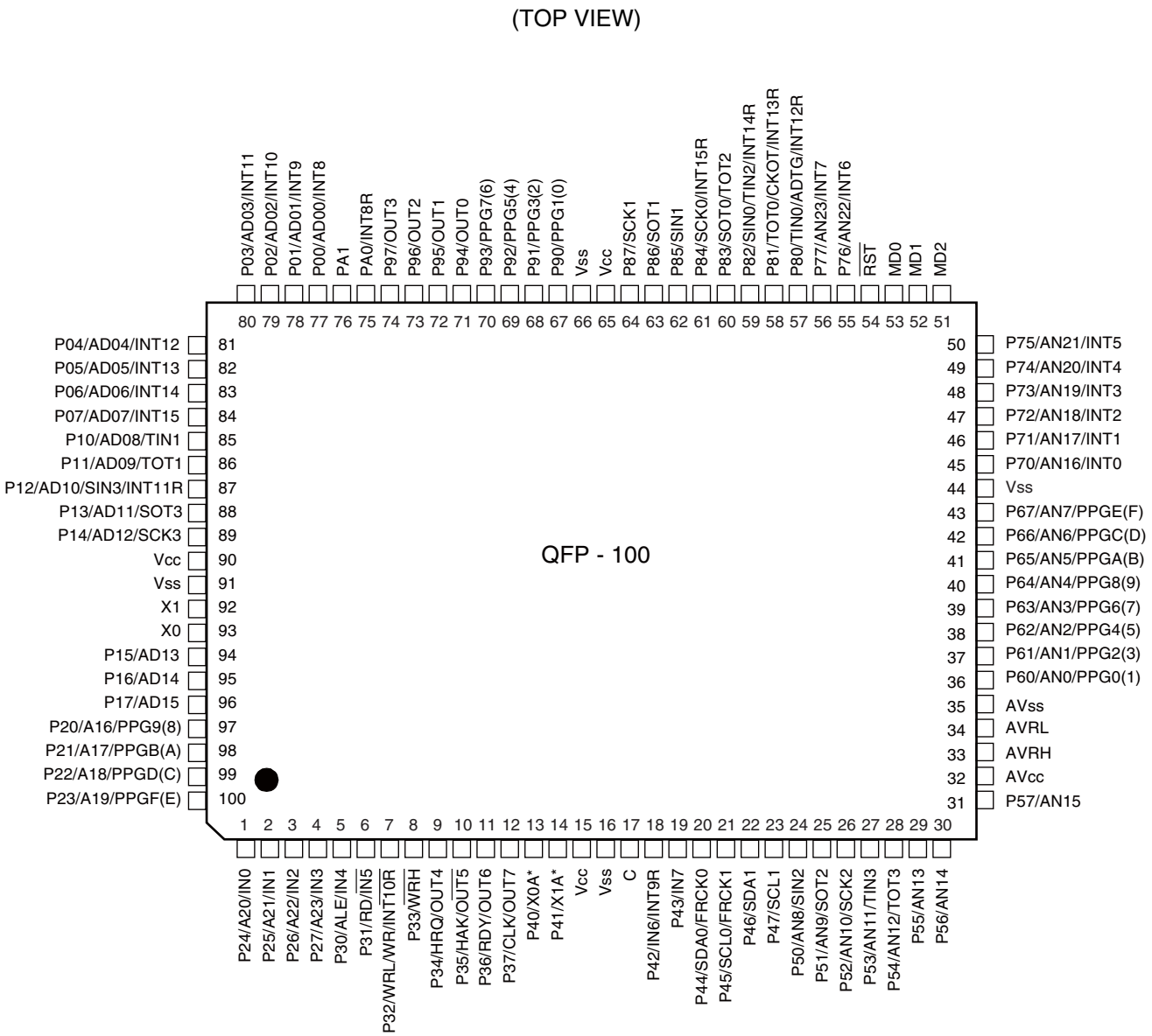
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(FPT-100P-M05)

* : X0A, X1A : MB90V340E-102
P40, P41 : MB90V340E-101

- MB90867E(S)/MB90F867E(S)



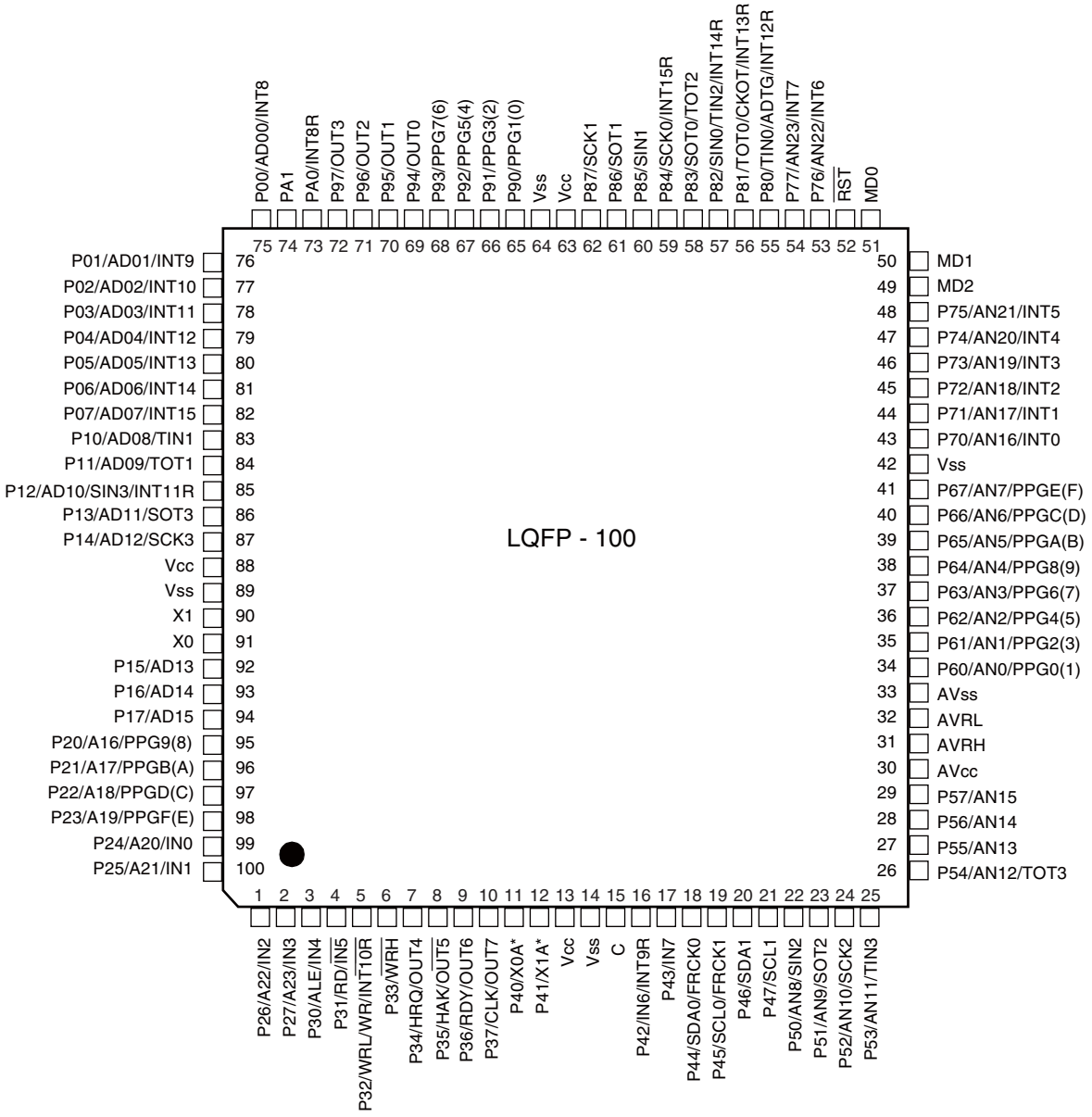
(FPT-100P-M06)

* : X0A, X1A : MB90867E, MB90F867E
P40, P41 : MB90867ES/MB90F867ES

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(TOP VIEW)



(FPT-100P-M05)

* : X0A, X1A : MB90867E, MB90F867E
P40, P41 : MB90867ES, MB90F867ES

■ PIN DESCRIPTION

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures 0 to 3.
5	3	P30	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor.This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture 4.
6	4	P31	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor.This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture 5.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled.
		$\overline{WR}$ / $\overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin (sub) .
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or with the $\overline{WRH}$ pin output disabled.
		$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare 4.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare 5.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare 6.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the clock output disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare 7.
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with S-suffix)
		X0A , X1A	B	Input pins for sub-clock (devices without S-suffix)
15	13	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V_{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 µF ceramic capacitor.
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture 6.
		INT9R		External interrupt request input pin (sub)

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture 7.
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I²C 0
		FRCK0		Input pin for the 16-bit I/O Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I²C 0
		FRCK1		Input pin for the 16-bit I/O Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I²C 1
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I²C 1
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer 3
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pin for the A/D converter
32	30	AV_{CC}	K	Power input pin for the A/D Converter analog

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AVCC.
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AVSS	K	GND pin for the A/D Converter analog
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	VSS	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	$\overline{RST}$	E	Reset input
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer 0
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin (sub)
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer 0
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin (sub)
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer 2
		INT14R		External interrupt request input pin (sub)
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer 2
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin (sub)

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V_{CC}	—	Power (3.5 V to 5.5 V) input pins
66	64	V_{SS}	—	GND pins
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pin
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pin
		OUT0 to OUT3		Waveform output pins for output compares 0 to 3. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		INT8R		External interrupt request input pin (sub)
76	74	PA1	F	General purpose I/O pin.
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer 1
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin (sub)
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V_{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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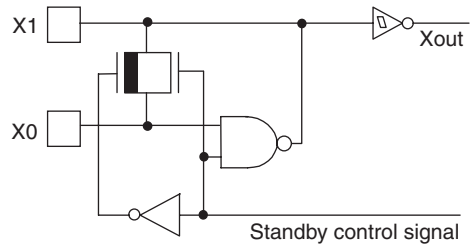
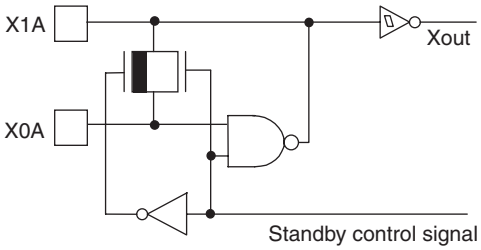
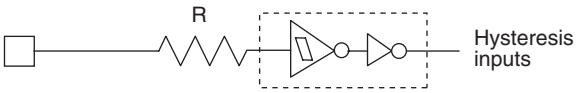
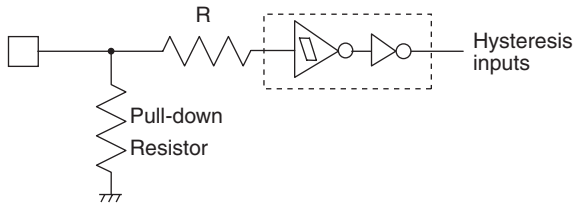
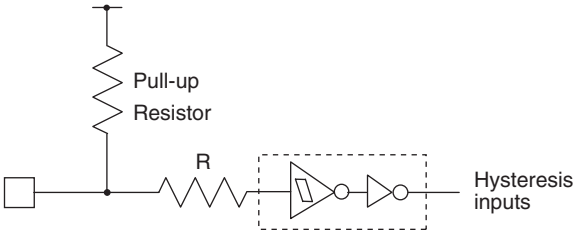
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9,PPGB, PPGD,PPGF		Output pins for PPGs

*1 : FPT-100P-M06

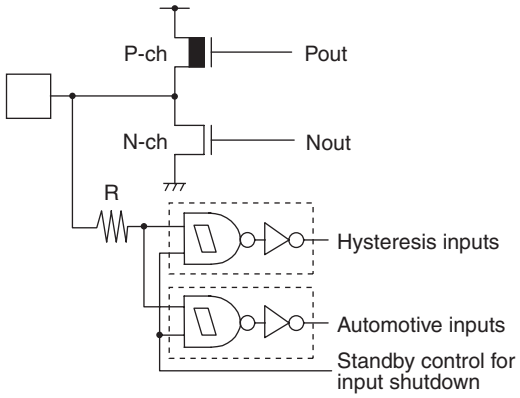
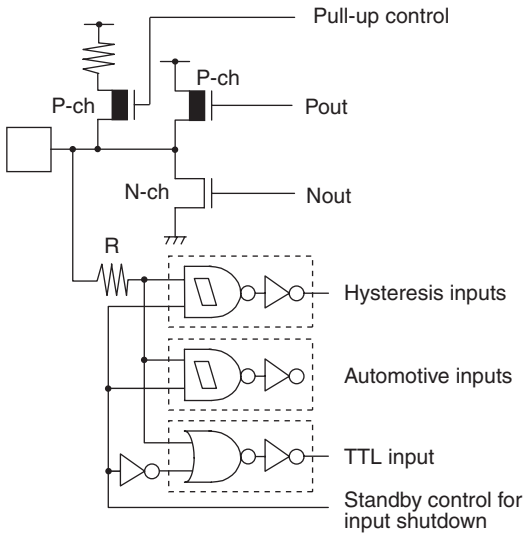
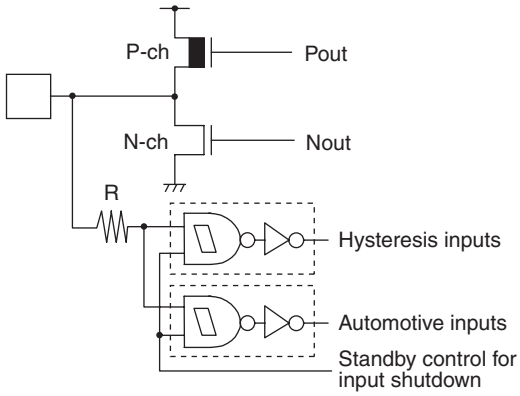
*2 : FPT-100P-M05

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

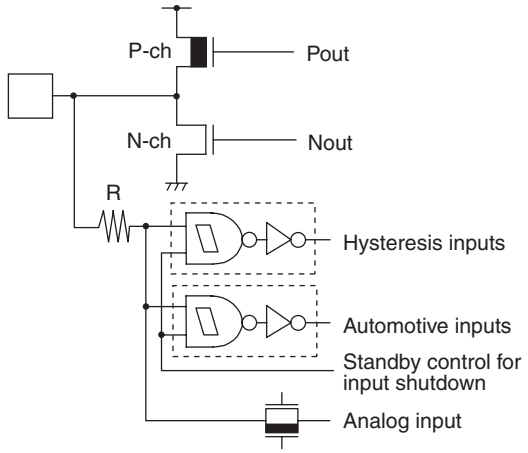
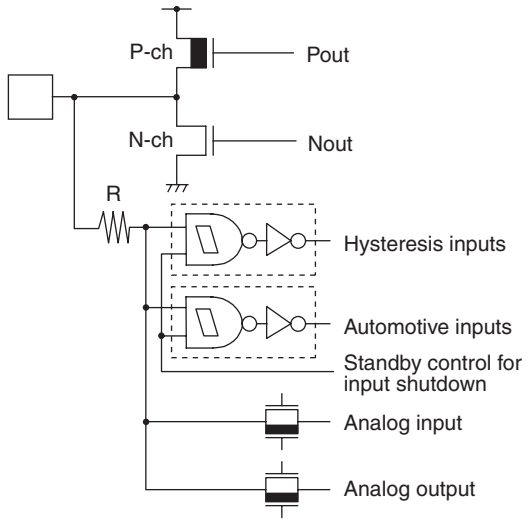
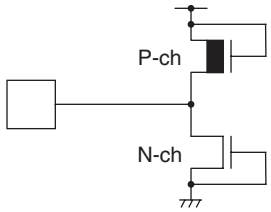
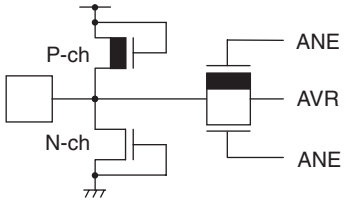
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		• Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		• Mask ROM and evaluation device: CMOS Hysteresis input pin • Flash device: CMOS input pin
D		• Mask ROM and evaluation device: CMOS Hysteresis input pin Pull-down resistor value: approx. 50 kΩ • Flash memory device: CMOS input pin No Pull-down
E		CMOS Hysteresis input pin Pull-up resistor value: approx. 50 kΩ

(Continued)

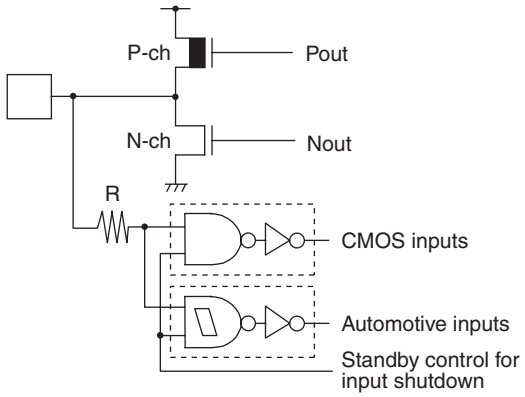
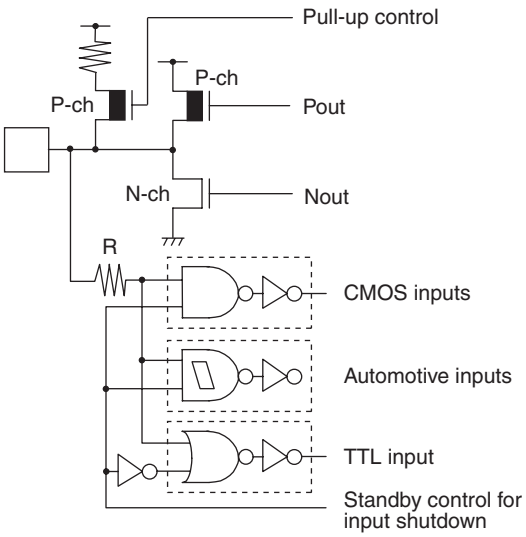
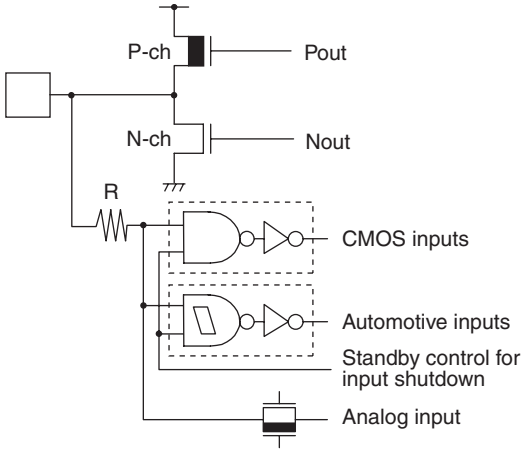
Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: 50 kΩ approx.
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

(Continued)

Type	Circuit	Remarks
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D converter analog input
J		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • D/A analog output • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D converter analog input
K		Power supply input protection circuit
L		• A/D converter reference voltage power supply input pin, with the protection circuit • Flash devices do not have a protection circuit against V_{CC} for pin AVRH

(Continued)

(Continued)

Type	Circuit	Remarks
M		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) Programmable pull-up registor:50 kΩ approx
O		• CMOS level output(I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D converter analog input

■ HANDLING DEVICES

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

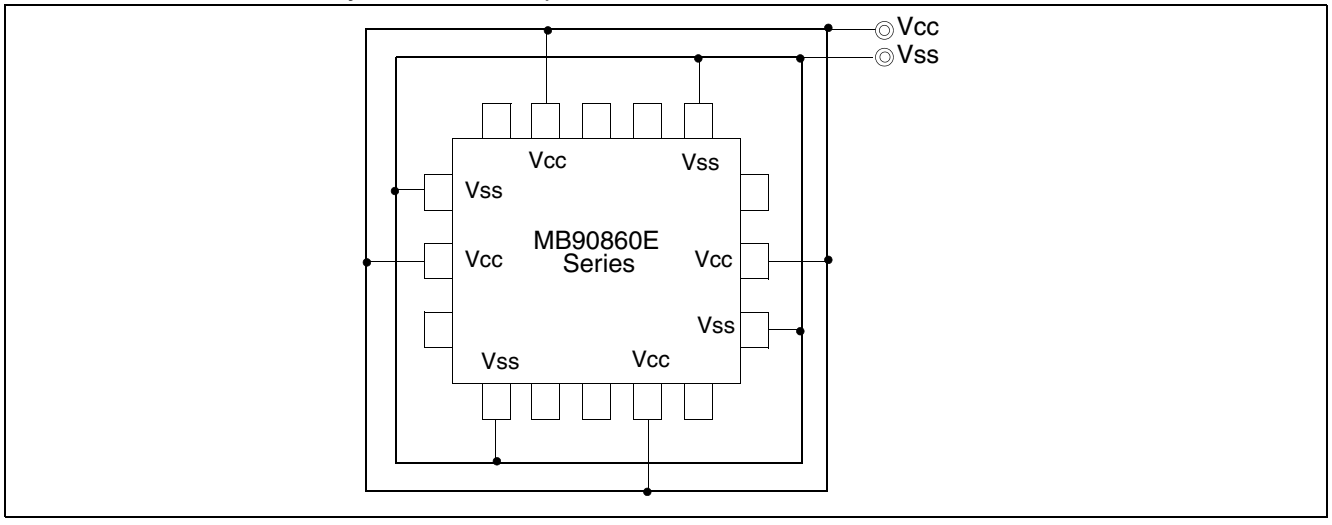
2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device



4. Mode Pin (MD0 to MD2)

Connect the mode pin directly to V_{CC} or V_{SS} pins.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

5. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

6. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

7. Crystal Oscillator Circuit

X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

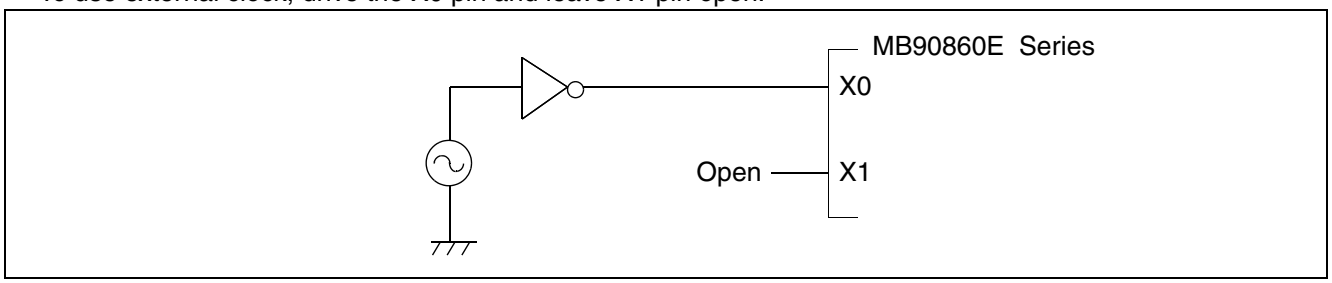
It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

8. Pull-up/down resistors

The MB90860E Series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

9. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



10. Precautions for when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

11. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the MB90860 series attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more μs (0.2 V to 2.7 V)

13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.

For the reference, stabilize the supply voltage by setting the following value.

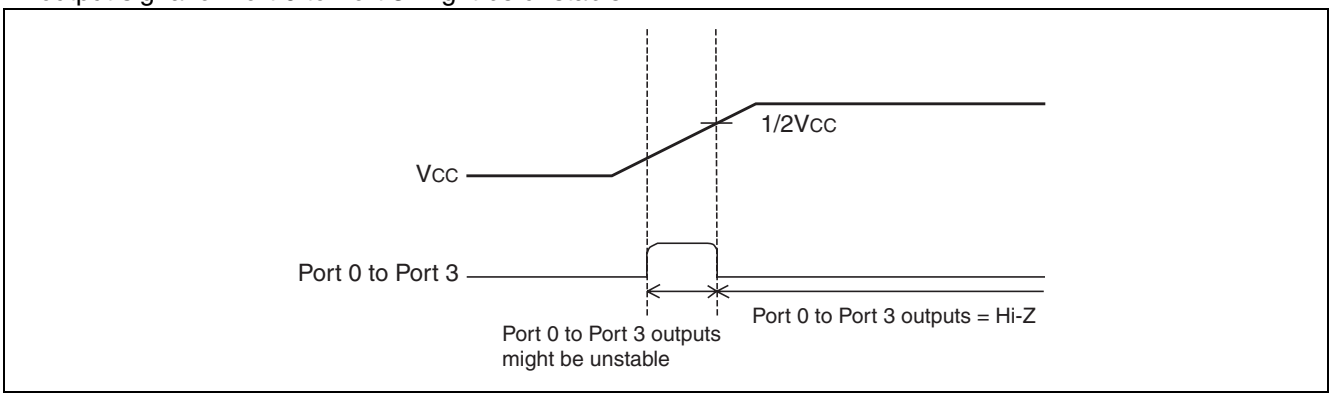
- V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage
- The coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

15. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in External-Bus mode, in spite of reset input, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



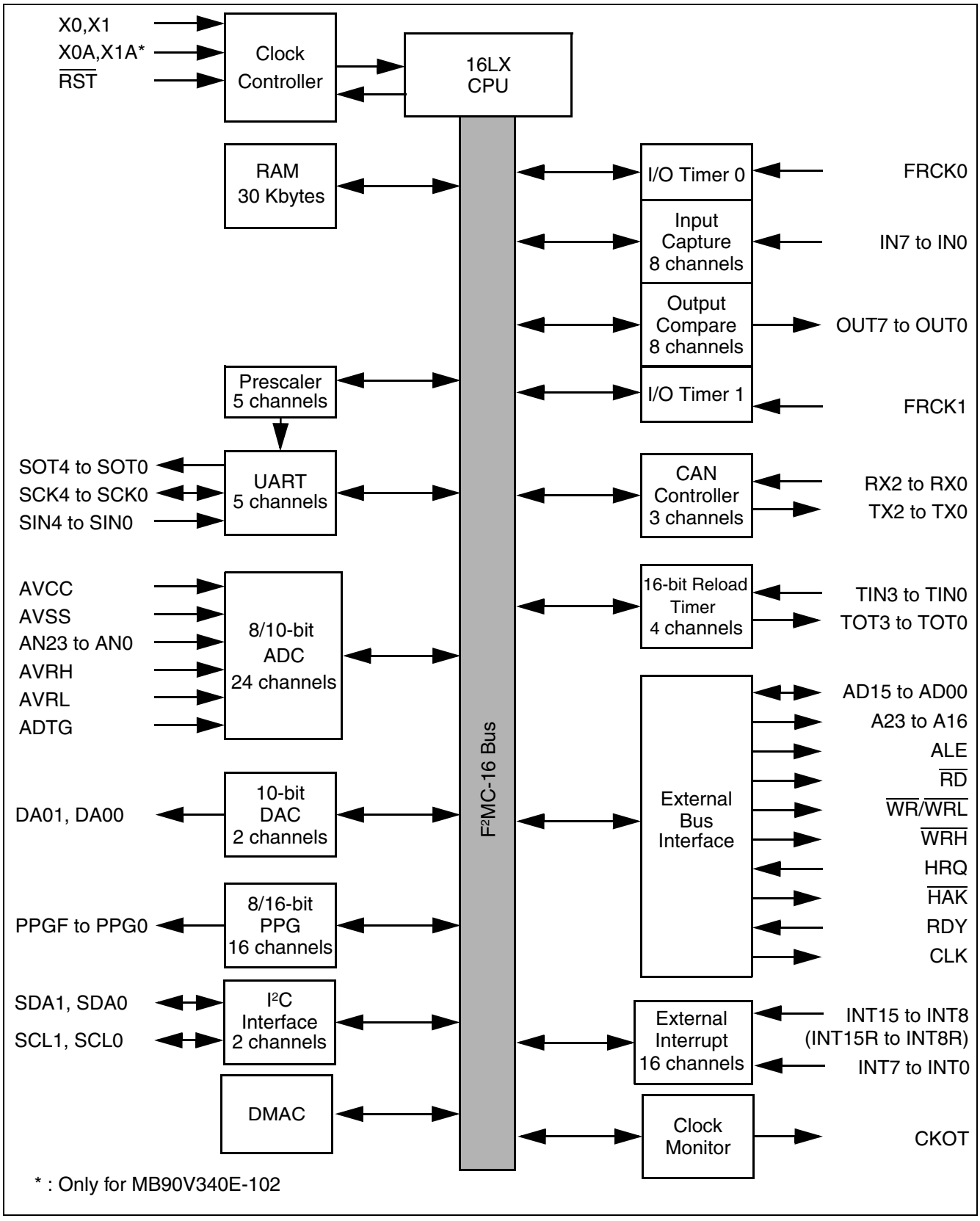
16. Flash security Function

The security bit is located in the area of the flash memory.
If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security bit.

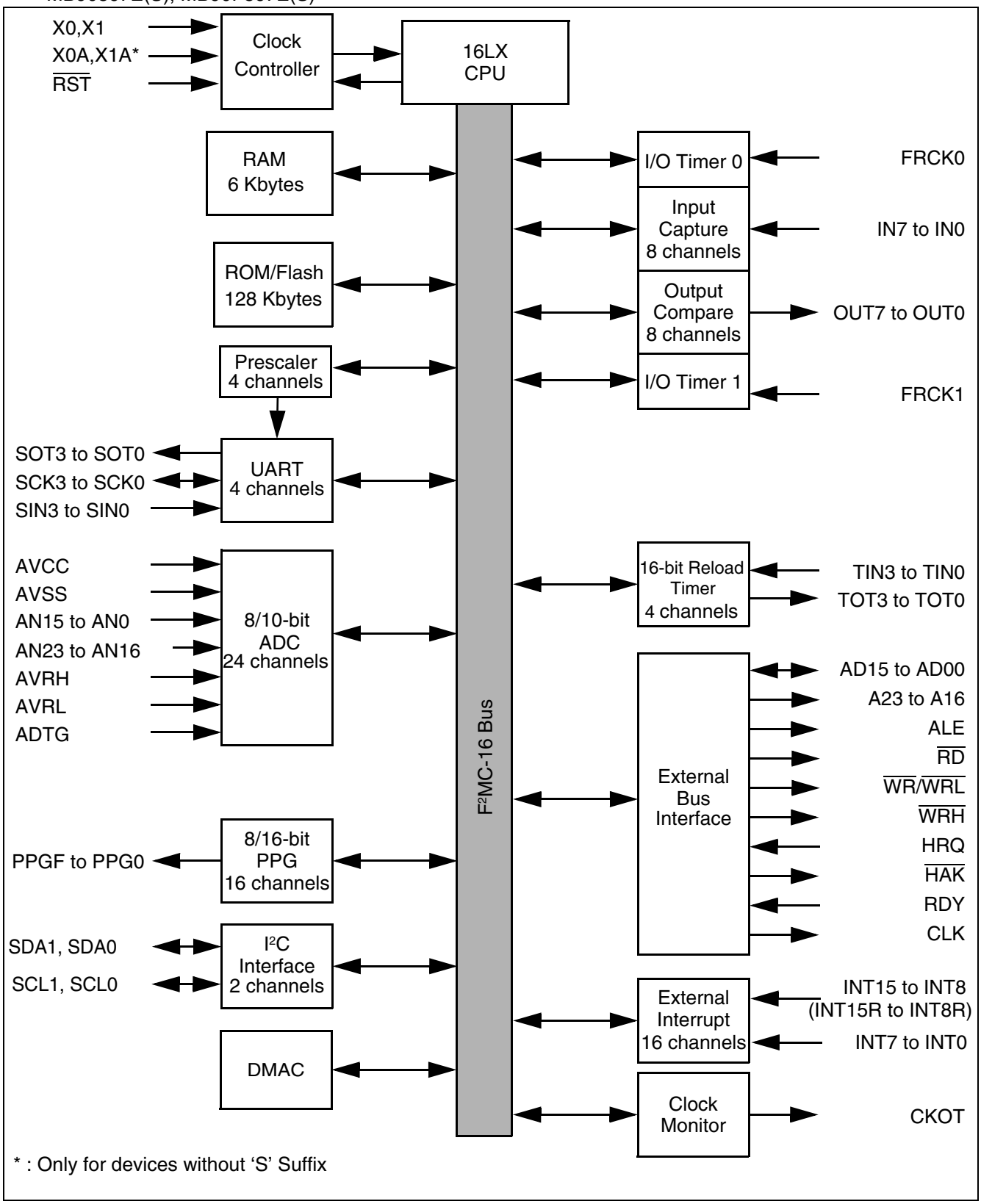
	Flash memory size	Address for security bit
MB90F867E(S)	Embedded 1 Mbit Flash Memory	$FE0001_H$

■ BLOCK DIAGRAMS

• MB90V340E-101/102

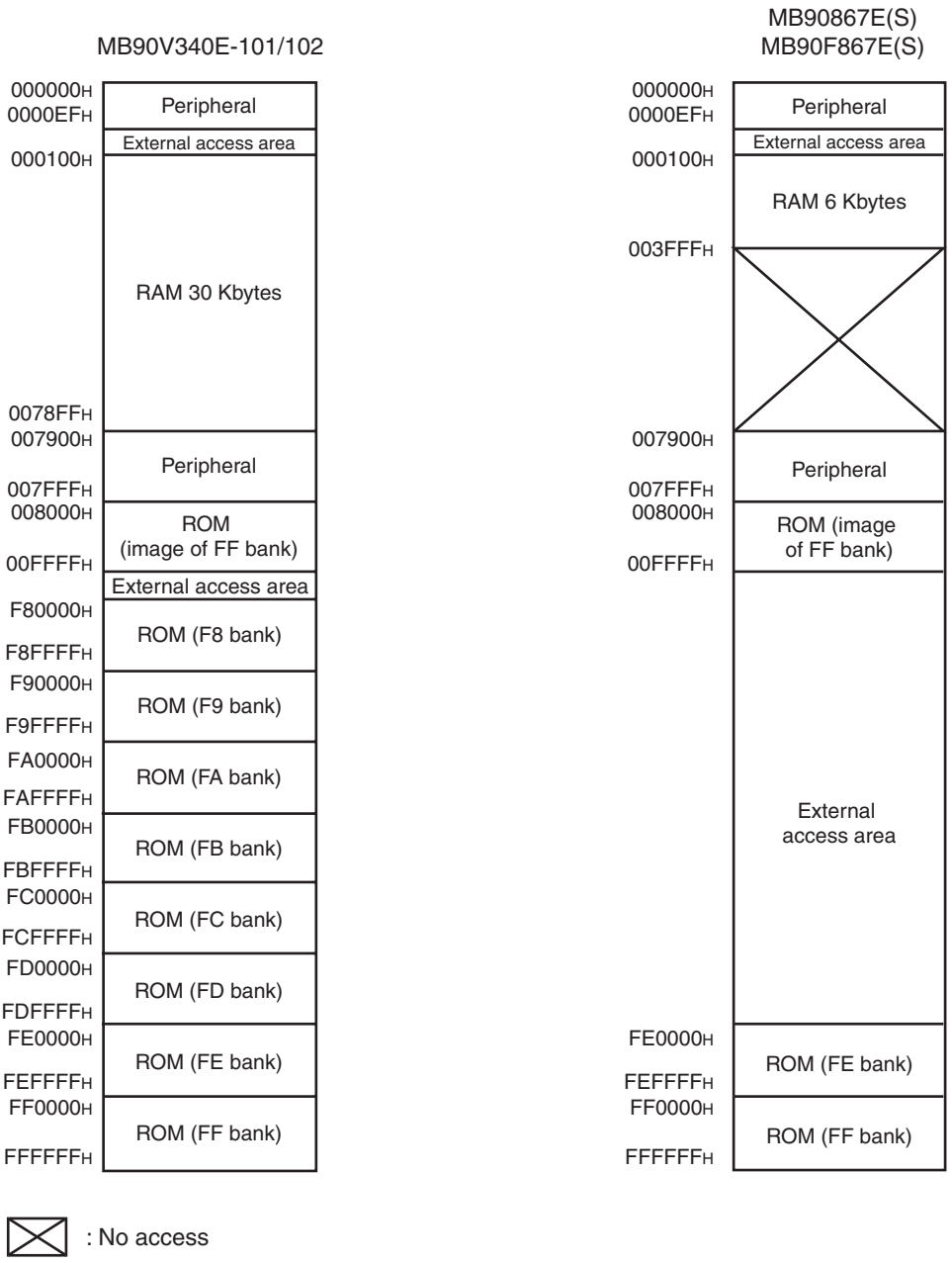


- MB90867E(S), MB90F867E(S)



* : Only for devices without ‘S’ Suffix

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
000000H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH	Port A Data Register	PDRA	R/W	Port A	XXXXXXXXB
00000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111B
00000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111B
00000DH	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	11111111B
00000EH	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXXB
00000FH	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXXB
000010H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000B
000012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000B
000013H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000B
00001AH	Port A Direction Register	DDRA	R/W	Port A	00000100B
00001BH	Reserved				
00001CH	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000B
00001DH	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000B
00001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000B
00001FH	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	00000000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000020H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000B
000021H	Serial Control Register 0	SCR0	W,R/W		00000000B
000022H	Reception/Transmission Data Register 0	RDR0/ TDR0	R/W		00000000B
000023H	Serial Status Register 0	SSR0	R,R/W		00001000B
000024H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XXB
000025H	Extended Status/Control Register 0	ESCR0	R/W		00000100B
000026H	Baud Rate Generator Register 00	BGR00	R/W		00000000B
000027H	Baud Rate Generator Register 01	BGR01	R/W		00000000B
000028H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000B
000029H	Serial Control Register 1	SCR1	W,R/W		00000000B
00002AH	Reception/Transmission Data Register 1	RDR1/ TDR1	R/W		00000000B
00002BH	Serial Status Register 1	SSR1	R,R/W		00001000B
00002CH	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XXB
00002DH	Extended Status/Control Register 1	ESCR1	R/W		00000100B
00002EH	Baud Rate Generator Register 10	BGR10	R/W		00000000B
00002FH	Baud Rate Generator Register 11	BGR11	R/W		00000000B
000030H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1B
000031H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001B
000032H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0B
000033H	Reserved				
000034H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1B
000035H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001B
000036H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0B
000037H	Reserved				
000038H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1B
000039H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001B
00003AH	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0B
00003BH	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000B
00003CH	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1B
00003DH	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001B
00003EH	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0B
00003FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000040H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1B
000041H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001B
000042H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0B
000043H	Reserved				
000044H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1B
000045H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001B
000046H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0B
000047H	Reserved				
000048H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1B
000049H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001B
00004AH	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0B
00004BH	Reserved				
00004CH	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1B
00004DH	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001B
00004EH	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0B
00004FH	Reserved				
000050H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000B
000051H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XXB
000052H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000B
000053H	Input Capture Edge 2/3	ICE23	R		XXXXXXXXB
000054H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000B
000055H	Input Capture Edge 4/5	ICE45	R		XXXXXXXXB
000056H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000B
000057H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XXB
000058H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00B
000059H	Output Compare Control Status 1	OCS1	R/W		0XX00000B
00005AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00B
00005BH	Output Compare Control Status 3	OCS3	R/W		0XX00000B
00005CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00B
00005DH	Output Compare Control Status 5	OCS5	R/W		0XX00000B
00005EH	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00B
00005FH	Output Compare Control Status 7	OCS7	R/W		0XX00000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000060H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000B
000061H	Timer Control Status 0	TMCSR0	R/W		XXXX0000B
000062H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000B
000063H	Timer Control Status 1	TMCSR1	R/W		XXXX0000B
000064H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000B
000065H	Timer Control Status 2	TMCSR2	R/W		XXXX0000B
000066H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000B
000067H	Timer Control Status 3	TMCSR3	R/W		XXXX0000B
000068H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0B
000069H	A/D Control Status 1	ADCS1	R/W		0000000XB
00006AH	A/D Data 0	ADCR0	R		00000000B
00006BH	A/D Data 1	ADCR1	R		XXXXXX00B
00006CH	ADC Setting 0	ADSR0	R/W		00000000B
00006DH	ADC Setting 1	ADSR1	R/W		00000000B
00006EH	Reserved				
00006FH	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXX1B
000070H to 00009AH	Reserved				
00009BH	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000B
00009CH	DMA Status L Register	DSRL	R/W		00000000B
00009DH	DMA Status H Register	DSRH	R/W		00000000B
00009EH	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000B
00009FH	Delayed Interrupt/release	DIRR	R/W	Delayed Interrupt	XXXXXXX0B
0000A0H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000B
0000A1H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100B
0000A2H, 0000A3H	Reserved				
0000A4H	DMA Stop Status Register	DSSR	R/W	DMA	00000000B
0000A5H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00B
0000A6H	External Address Output Control Register	HACR	W		00000000B
0000A7H	Bus Control Signal Selection Register	ECSR	W		0000000XB
0000A8H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A9H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100B
0000AAH	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000B
0000ABH	Reserved				
0000ACH	DMA Enable L Register	DERL	R/W	DMA	00000000B
0000ADH	DMA Enable H Register	DERH	R/W		00000000B
0000AEH	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000B
0000AFH	Reserved				
0000B0H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111B
0000B1H	Interrupt Control Register 01	ICR01	W,R/W		00000111B
0000B2H	Interrupt Control Register 02	ICR02	W,R/W		00000111B
0000B3H	Interrupt Control Register 03	ICR03	W,R/W		00000111B
0000B4H	Interrupt Control Register 04	ICR04	W,R/W		00000111B
0000B5H	Interrupt Control Register 05	ICR05	W,R/W		00000111B
0000B6H	Interrupt Control Register 06	ICR06	W,R/W		00000111B
0000B7H	Interrupt Control Register 07	ICR07	W,R/W		00000111B
0000B8H	Interrupt Control Register 08	ICR08	W,R/W		00000111B
0000B9H	Interrupt Control Register 09	ICR09	W,R/W		00000111B
0000BAH	Interrupt Control Register 10	ICR10	W,R/W		00000111B
0000BBH	Interrupt Control Register 11	ICR11	W,R/W		00000111B
0000BCH	Interrupt Control Register 12	ICR12	W,R/W		00000111B
0000BDH	Interrupt Control Register 13	ICR13	W,R/W		00000111B
0000BEH	Interrupt Control Register 14	ICR14	W,R/W		00000111B
0000BFH	Interrupt Control Register 15	ICR15	W,R/W		00000111B
0000C0H	D/A Converter Data 0 Register	DAT0	R/W	D/A Converter	XXXXXXXXB
0000C1H	D/A Converter Data 1 Register	DAT1	R/W		XXXXXXXXB
0000C2H	D/A Control 0 Register	DACR0	R/W		XXXXXXX0B
0000C3H	D/A Control 1 Register	DACR1	R/W		XXXXXXX0B
0000C4H, 0000C5H	Reserved				
0000C6H	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000B
0000C7H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXXB
0000C8H	External Interrupt Level Setting 0	ELVR0	R/W		00000000B
0000C9H	External Interrupt Level Setting 0	ELVR0	R/W		00000000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000CA$_H$	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000$_B$
0000CB$_H$	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX$_B$
0000CC$_H$	External Interrupt Level Setting 1	ELVR1	R/W		00000000$_B$
0000CD$_H$	External Interrupt Level Setting 1	ELVR1	R/W		00000000$_B$
0000CE$_H$	External Interrupt Source Select	EISSR	R/W		00000000$_B$
0000CF$_H$	PLL/Sub Clock Control Register	PSCCR	W	PLL	XXXX0000$_B$
0000D0$_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX$_B$
0000D1$_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX$_B$
0000D2$_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX$_B$
0000D3$_H$	DMA Control Register	DMACS	R/W		XXXXXXXX$_B$
0000D4$_H$	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX$_B$
0000D5$_H$	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX$_B$
0000D6$_H$	Data Counter L Register	DCTL	R/W		XXXXXXXX$_B$
0000D7$_H$	Data Counter H Register	DCTH	R/W		XXXXXXXX$_B$
0000D8$_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000$_B$
0000D9$_H$	Serial Control Register 2	SCR2	W,R/W		00000000$_B$
0000DA$_H$	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000$_B$
0000DB$_H$	Serial Status Register 2	SSR2	R,R/W		00001000$_B$
0000DC$_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX$_B$
0000DD$_H$	Extended Status Control Register 2	ESCR2	R/W		00000100$_B$
0000DE$_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000$_B$
0000DF$_H$	Baud Rate Generator Register 21	BGR21	R/W		00000000$_B$
0000E0$_H$ to 0000FF$_H$	External area				
007900$_H$	Reload Register L0	PRLL0	R/W	16-bit PPG 0/1	XXXXXXXX$_B$
007901$_H$	Reload Register H0	PRLH0	R/W		XXXXXXXX$_B$
007902$_H$	Reload Register L1	PRLL1	R/W		XXXXXXXX$_B$
007903$_H$	Reload Register H1	PRLH1	R/W		XXXXXXXX$_B$
007904$_H$	Reload Register L2	PRLL2	R/W	16-bit PPG 2/3	XXXXXXXX$_B$
007905$_H$	Reload Register H2	PRLH2	R/W		XXXXXXXX$_B$
007906$_H$	Reload Register L3	PRLL3	R/W		XXXXXXXX$_B$
007907$_H$	Reload Register H3	PRLH3	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007908H	Reload Register L4	PRLL4	R/W	16-bit PPG 4/5	XXXXXXXXB
007909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
00790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
00790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
00790CH	Reload Register L6	PRLL6	R/W	16-bit PPG 6/7	XXXXXXXXB
00790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
00790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
00790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
007910H	Reload Register L8	PRLL8	R/W	16-bit PPG 8/9	XXXXXXXXB
007911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
007912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
007913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
007914H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	XXXXXXXXB
007915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
007916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
007917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
007918H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	XXXXXXXXB
007919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
00791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
00791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
00791CH	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXXB
00791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
00791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
00791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
007920H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
007921H	Input Capture 0	IPCP0	R		XXXXXXXXB
007922H	Input Capture 1	IPCP1	R		XXXXXXXXB
007923H	Input Capture 1	IPCP1	R		XXXXXXXXB
007924H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
007925H	Input Capture 2	IPCP2	R		XXXXXXXXB
007926H	Input Capture 3	IPCP3	R		XXXXXXXXB
007927H	Input Capture 3	IPCP3	R		XXXXXXXXB
007928H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
007929H	Input Capture 4	IPCP4	R		XXXXXXXXB
00792AH	Input Capture 5	IPCP5	R		XXXXXXXXB
00792BH	Input Capture 5	IPCP5	R		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
00792C$_H$	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX$_B$
00792D$_H$	Input Capture 6	IPCP6	R		XXXXXXXX$_B$
00792E$_H$	Input Capture 7	IPCP7	R		XXXXXXXX$_B$
00792F$_H$	Input Capture 7	IPCP7	R		XXXXXXXX$_B$
007930$_H$	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX$_B$
007931$_H$	Output Compare 0	OCCP0	R/W		XXXXXXXX$_B$
007932$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
007933$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
007934$_H$	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
007935$_H$	Output Compare 2	OCCP2	R/W		XXXXXXXX$_B$
007936$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
007937$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
007938$_H$	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
007939$_H$	Output Compare 4	OCCP4	R/W		XXXXXXXX$_B$
00793A$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$
00793B$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$
00793C$_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX$_B$
00793D$_H$	Output Compare 6	OCCP6	R/W		XXXXXXXX$_B$
00793E$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
00793F$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
007940$_H$	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
007941$_H$	Timer Data 0	TCDT0	R/W		00000000$_B$
007942$_H$	Timer Control Status 0	TCCSL0	R/W		00000000$_B$
007943$_H$	Timer Control Status 0	TCCSH0	R/W		0XXXXXXX$_B$
007944$_H$	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000$_B$
007945$_H$	Timer Data 1	TCDT1	R/W		00000000$_B$
007946$_H$	Timer Control Status 1	TCCSL1	R/W		00000000$_B$
007947$_H$	Timer Control Status 1	TCCSH1	R/W		0XXXXXXX$_B$
007948$_H$	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
007949$_H$			R/W		XXXXXXXX$_B$
00794A$_H$	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
00794B$_H$			R/W		XXXXXXXX$_B$
00794C$_H$	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
00794D$_H$			R/W		XXXXXXXX$_B$
00794E$_H$	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
00794F$_H$			R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000B
007951H	Serial Control Register 3	SCR3	W,R/W		00000000B
007952H	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000B
007953H	Serial Status Register 3	SSR3	R,R/W		00001000B
007954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
007955H	Extended Status Control Register	ESCR3	R/W		00000100B
007956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
007957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
007958H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000B
007959H	Serial Control Register 4	SCR4	W,R/W		00000000B
00795AH	Reception/Transmission Data Register 4	RDR4/ TDR4	R/W		00000000B
00795BH	Serial Status Register 4	SSR4	R,R/W		00001000B
00795CH	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XXB
00795DH	Extended Status Control Register	ESCR4	R/W		00000100B
00795EH	Baud Rate Generator Register 40	BGR40	R/W		00000000B
00795FH	Baud Rate generator Register 41	BGR41	R/W		00000000B
007960H to 00796BH	Reserved				
00796CH	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000B
00796DH to 00796FH	Reserved				
007970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
007971H	I²C bus Control Register 0	IBCR0	W,R/W		00000000B
007972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
007973H		ITBAH0	R/W		00000000B
007974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
007975H		ITMKH0	R/W		00111111B
007976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
007977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
007978H	I²C Data Register 0	IDAR0	R/W		00000000B
007979H, 00797AH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
00797B$_H$	I^{2}C Clock Control Register 0	ICCR0	R/W	I^{2}C Interface 0	00011111$_B$
00797C$_H$ to 00797F$_H$	Reserved				
007980$_H$	I^{2}C Bus Status Register 1	IBSR1	R	I^{2}C Interface 1	00000000$_B$
007981$_H$	I^{2}C Bus Control Register 1	IBCR1	W,R/W		00000000$_B$
007982$_H$	I^{2}C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000$_B$
007983$_H$		ITBAH1	R/W		00000000$_B$
007984$_H$	I^{2}C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111$_B$
007985$_H$		ITMKH1	R/W		00111111$_B$
007986$_H$	I^{2}C 7-bit Slave Address Register 1	ISBA1	R/W		00000000$_B$
007987$_H$	I^{2}C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111$_B$
007988$_H$	I^{2}C Data Register 1	IDAR1	R/W		00000000$_B$
007989$_H$, 00798A$_H$	Reserved				
00798B$_H$	I^{2}C Clock Control Register 1	ICCR1	R/W	I^{2}C Interface 1	00011111$_B$
00798C$_H$ to 0079C1$_H$	Reserved				
0079C2$_H$	Clock modulator control register (setting prohibited)	CMCR	R, R/W	Clock modulator (using prohibited)	0001X000$_B$
0079C3$_H$ to 0079DF$_H$	Reserved				
0079E0$_H$	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX$_B$
0079E1$_H$	Detect Address Setting 0	PADR0	R/W		XXXXXXXX$_B$
0079E2$_H$	Detect Address Setting 0	PADR0	R/W		XXXXXXXX$_B$
0079E3$_H$	Detect Address Setting 1	PADR1	R/W		XXXXXXXX$_B$
0079E4$_H$	Detect Address Setting 1	PADR1	R/W		XXXXXXXX$_B$
0079E5$_H$	Detect Address Setting 1	PADR1	R/W		XXXXXXXX$_B$
0079E6$_H$	Detect Address Setting 2	PADR2	R/W		XXXXXXXX$_B$
0079E7$_H$	Detect Address Setting 2	PADR2	R/W		XXXXXXXX$_B$
0079E8$_H$	Detect Address Setting 2	PADR2	R/W		XXXXXXXX$_B$
0079E9$_H$ to 0079EF$_H$	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Resource name	Initial value
0079F0H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
0079F1H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F2H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F3H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F4H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F5H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F6H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F7H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F8H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F9H to 007FFFH	Reserved				

Notes : • Initial value of “X” represents unknown value.
• Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
(Reserved)	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
(Reserved)	N	—	#12	FFFFCC$_H$		
Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
Input Capture 7	Y1	—	#14	FFFFC4$_H$		
I²C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
(Reserved)	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 0/1/4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
8/10-bit A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O Timer 0, I/O Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5, I²C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 Reception	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 Transmission	Y1	11	#36	FFFF6C$_H$		
UART 1 Reception / UART 3 Reception	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 Transmission / UART 3 Transmission	Y1	13	#38	FFFF64$_H$		

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Interrupt cause	EI²OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 Reception / UART 4 Reception	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 Transmission / UART 4 Transmission	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N	—	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	–4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	–100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	–50	mA	*4
Power consumption	P_D	—	340	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

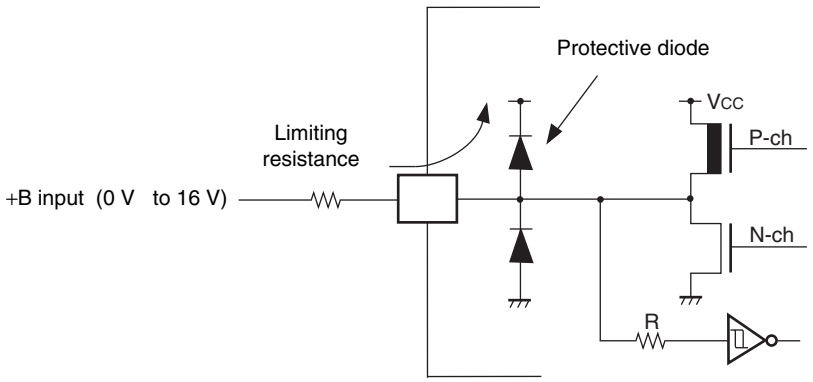
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*5 : • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits

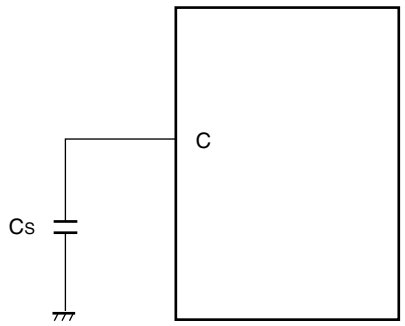


WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	−40	—	+105	°C	



C Pin Connection Diagram

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} – 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = –3.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	

(Continued)

(Continued)

(T_A = −40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−1	—	+ 1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash devices
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing FLASH memory.	—	70	85	mA	Flash devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing FLASH memory.	—	75	90	mA	Flash devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At sub operation T_A = +25°C	—	70	140	µA	
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At sub sleep T_A = +25°C	—	20	50	µA	
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At watch mode T_A = +25°C	—	10	35	µA	
	I_{CCH}		V_{CC} = 5.0 V, At Stop mode, T_A = +25°C	—	7	25	µA	
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS},	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

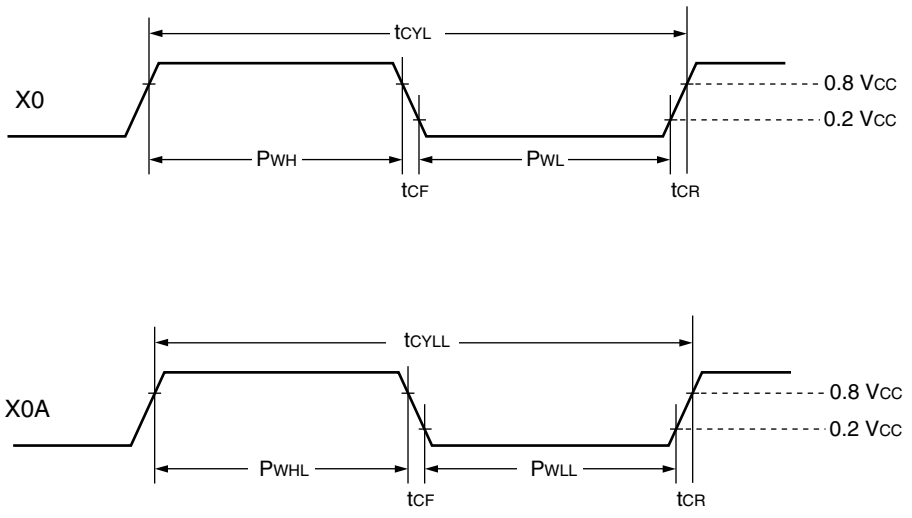
4. AC Characteristics

(1) Clock Timing

(T_A = −40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

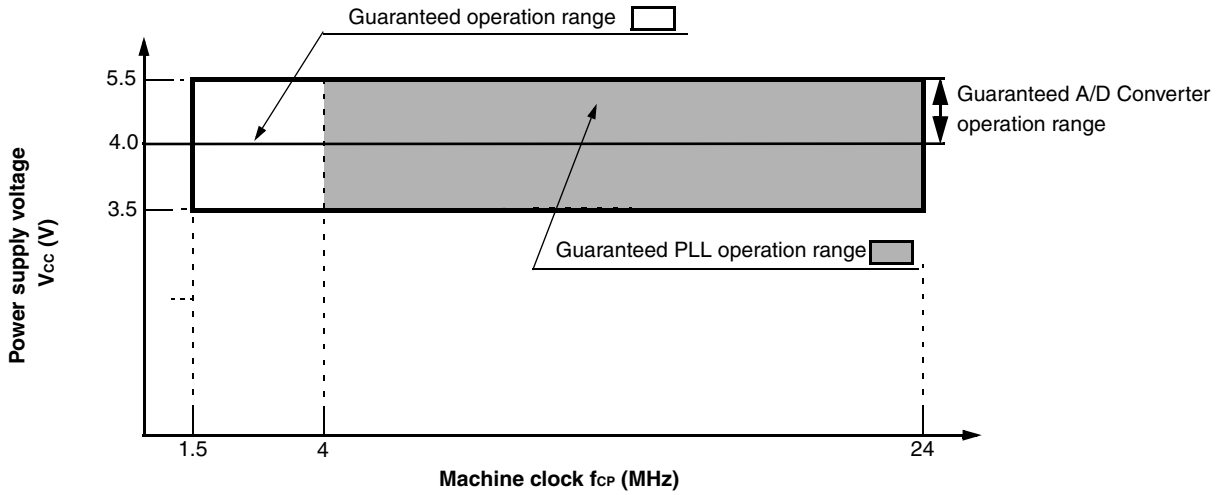
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
		X0, X1	3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relation among external clock frequency and machine clock frequency”.

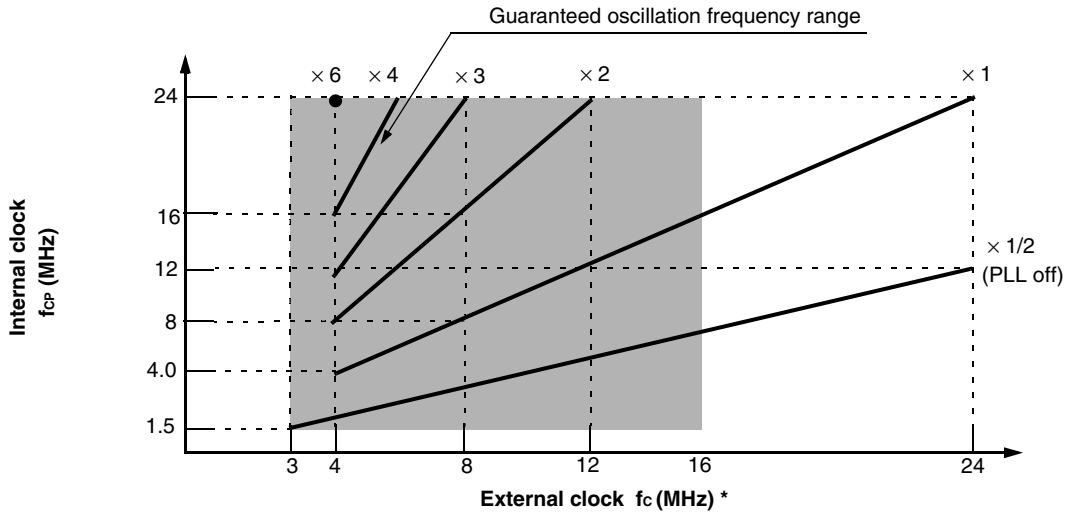


Clock Timing

• Guaranteed PLL operation range



Guaranteed operation range of MB90860E series



* : When using crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

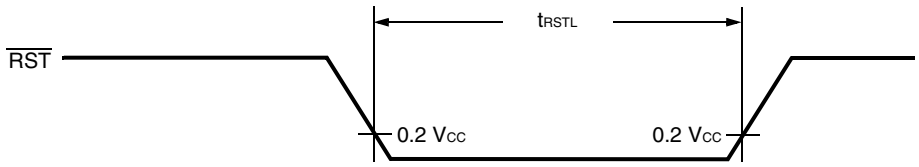
(2) Reset Standby Input

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

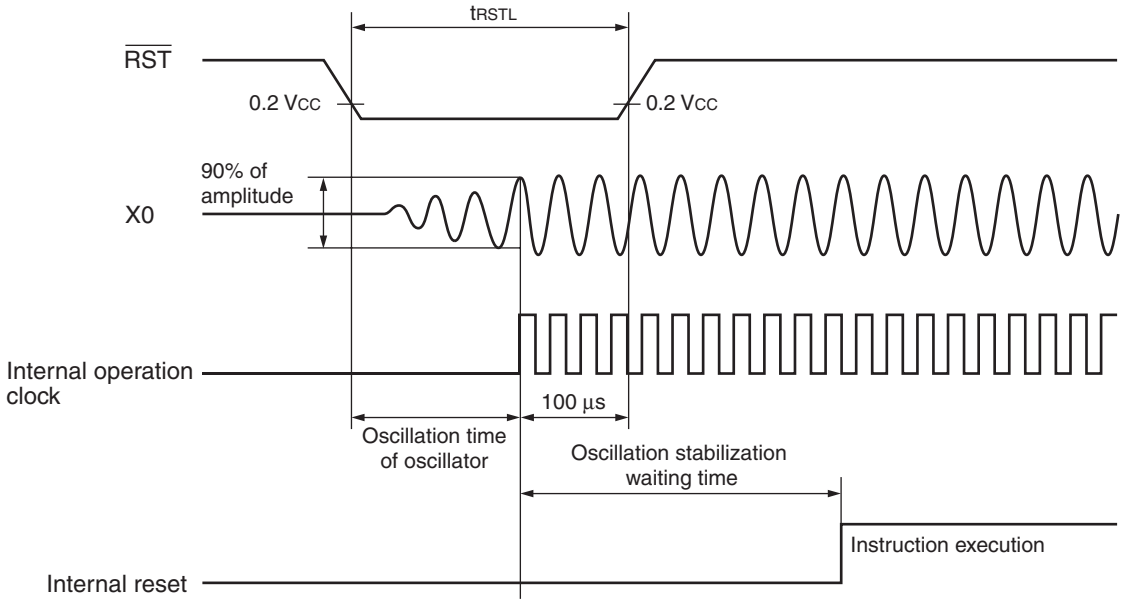
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	ns	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Time Timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode, Power-on:



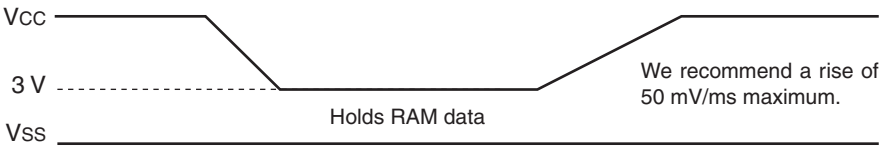
(3) Power On Reset

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



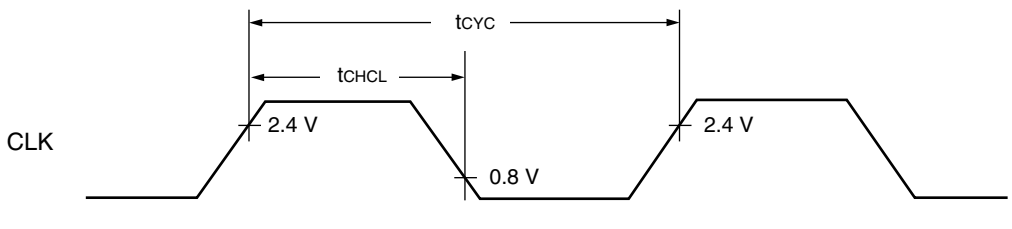
If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate



(4) Clock Output Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

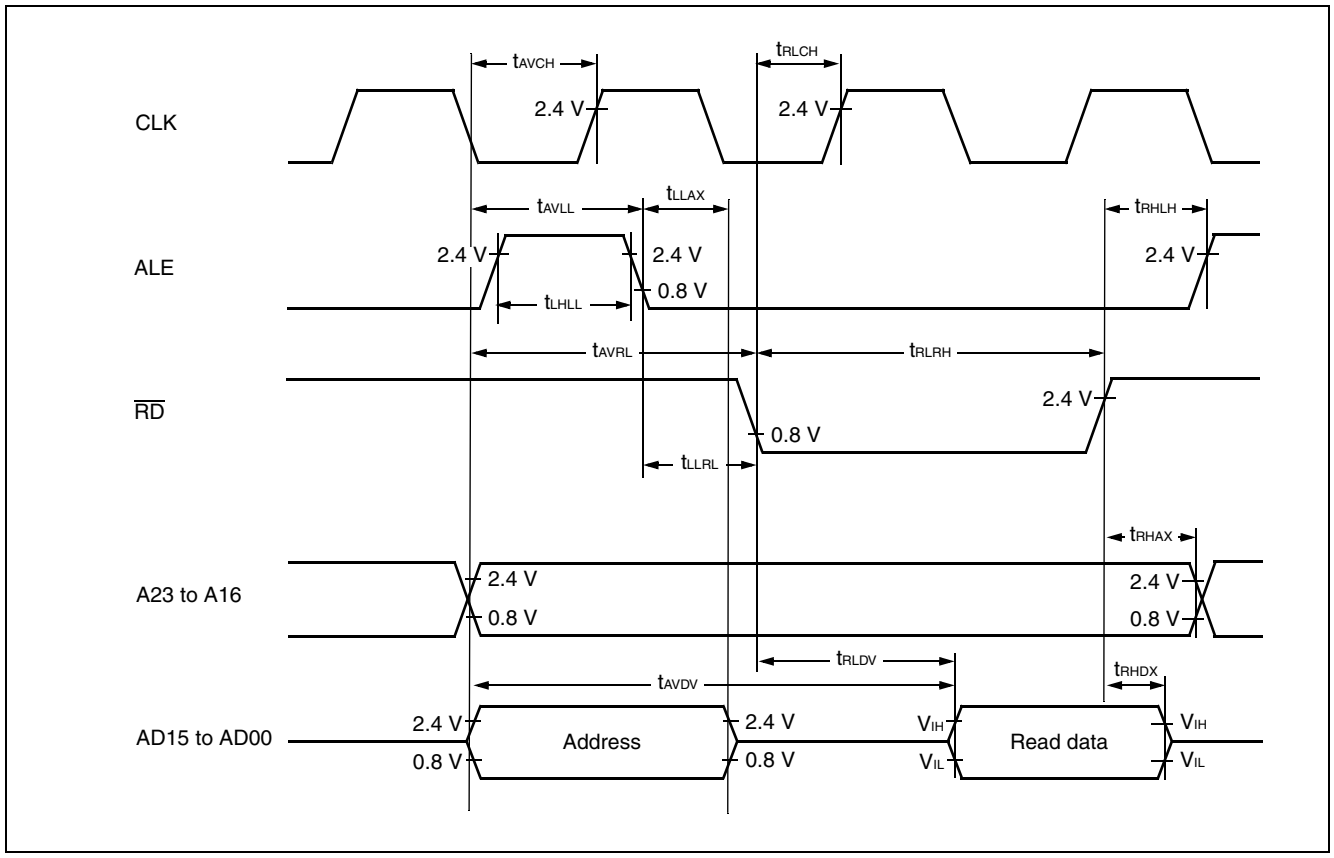
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.76	—	ns	f_{CP} = 24 MHz
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz



(5) Bus Timing (Read)

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

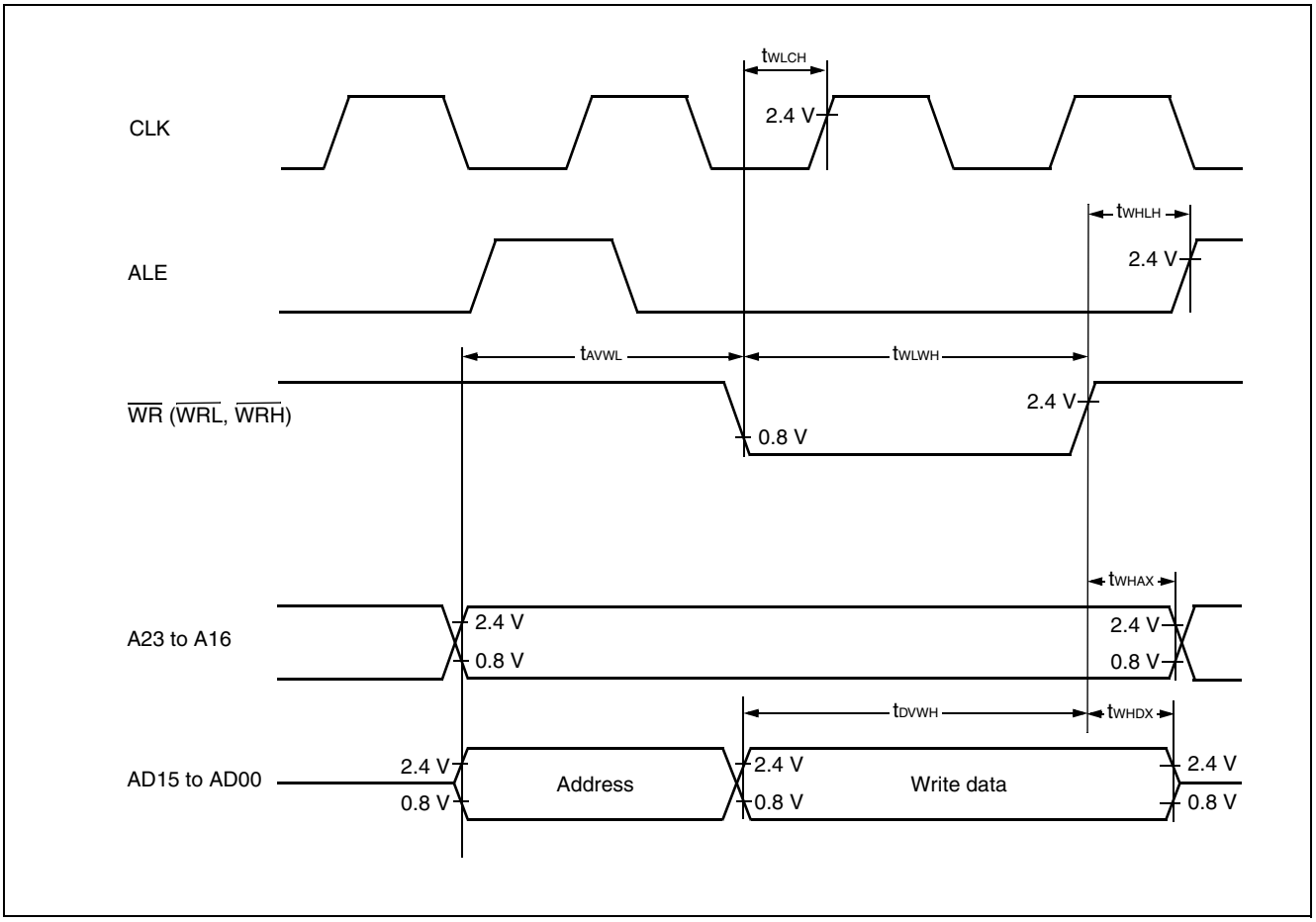
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns
Valid address → Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$3\ t_{CP}/2 - 20$	—	ns
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$3\ t_{CP}/2 - 50$	ns
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns
$\overline{RD}$ ↓ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns



(6) Bus Timing (Write)

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}–15	—	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 – 20	—	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 – 20	—	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	—	ns

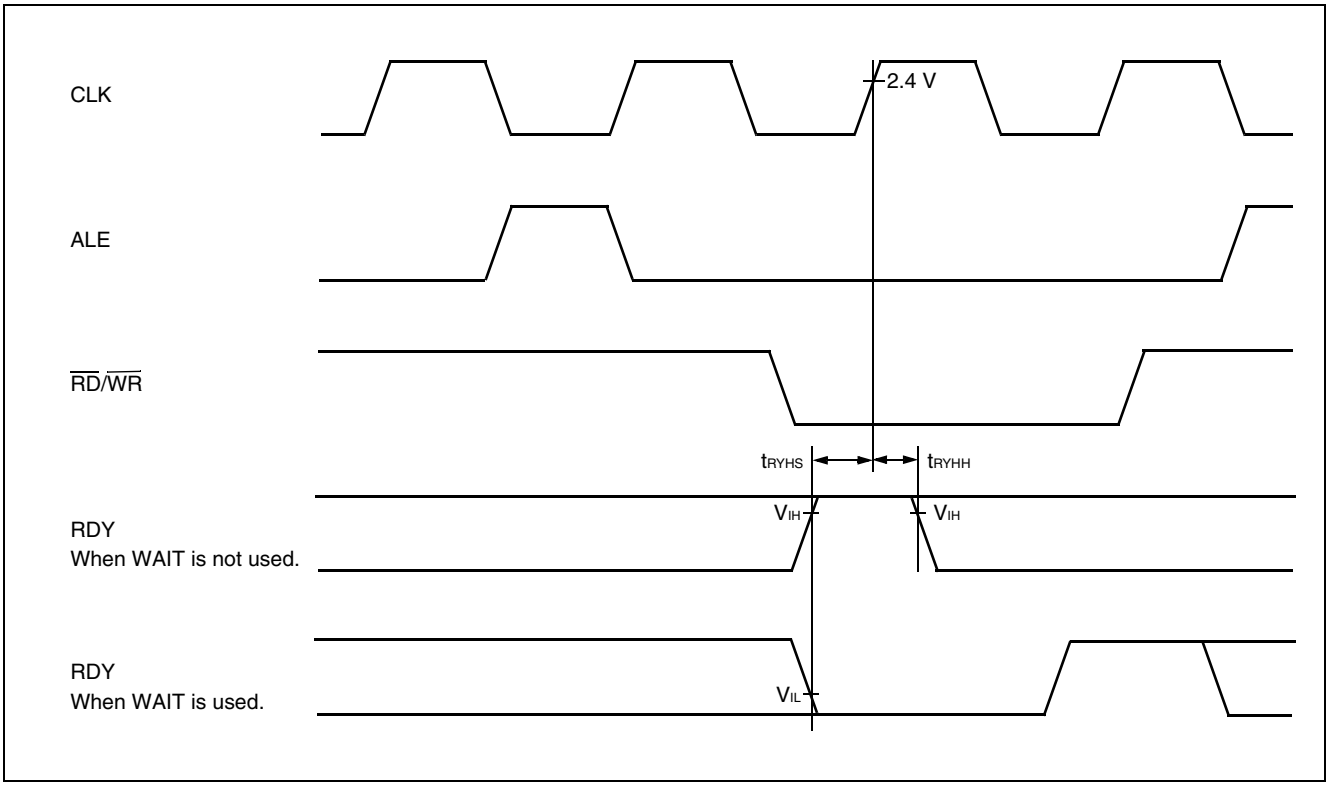


(7) Ready Input Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

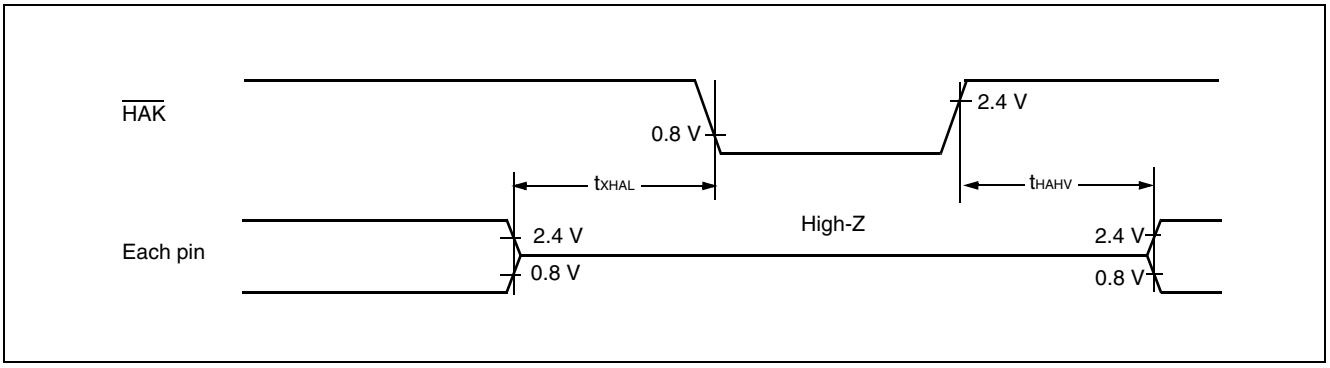


(8) Hold Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns
$\overline{HAK}$ ↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

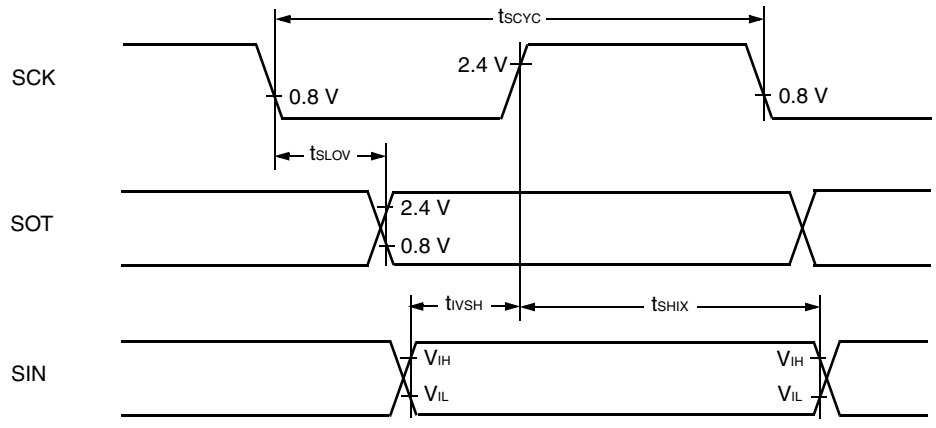


(9) UART0/1/2/3/4

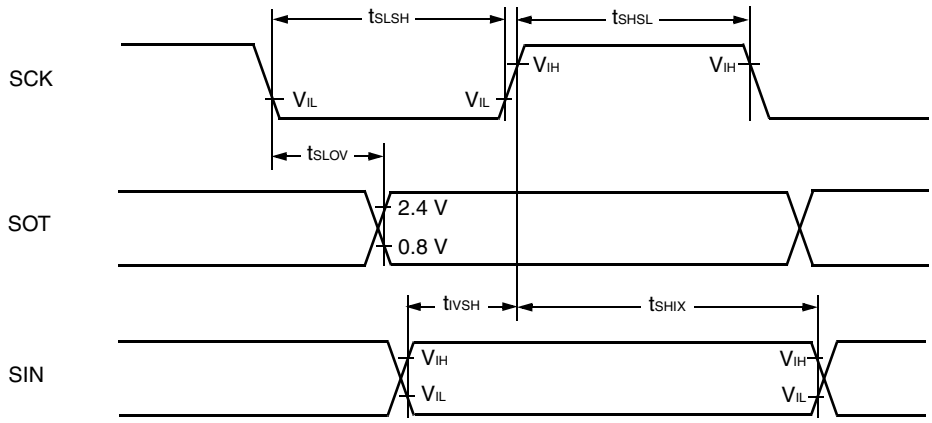
(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, $f_{CP} \leq$ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		–80	+80	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		100	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK4	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK4		4 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns

Notes : • AC characteristic in CLK synchronized mode.
• C_L is load capacity value of pins when testing.



Internal Shift Clock Mode

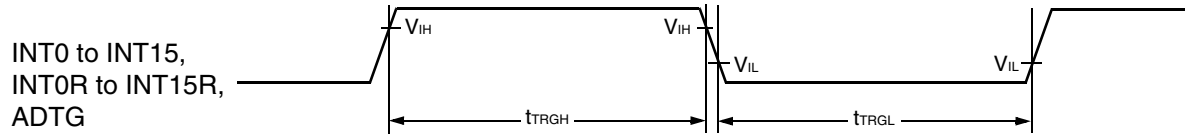


External Shift Clock Mode

(10) Trigger Input Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

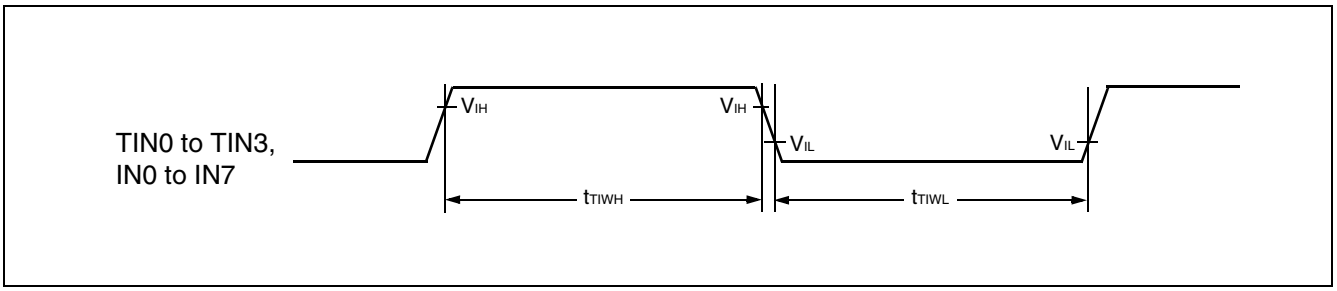
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT0R to INT15R, ADTG	—	5 t_{CP}	—	ns



(11) Timer Related Resource Input Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

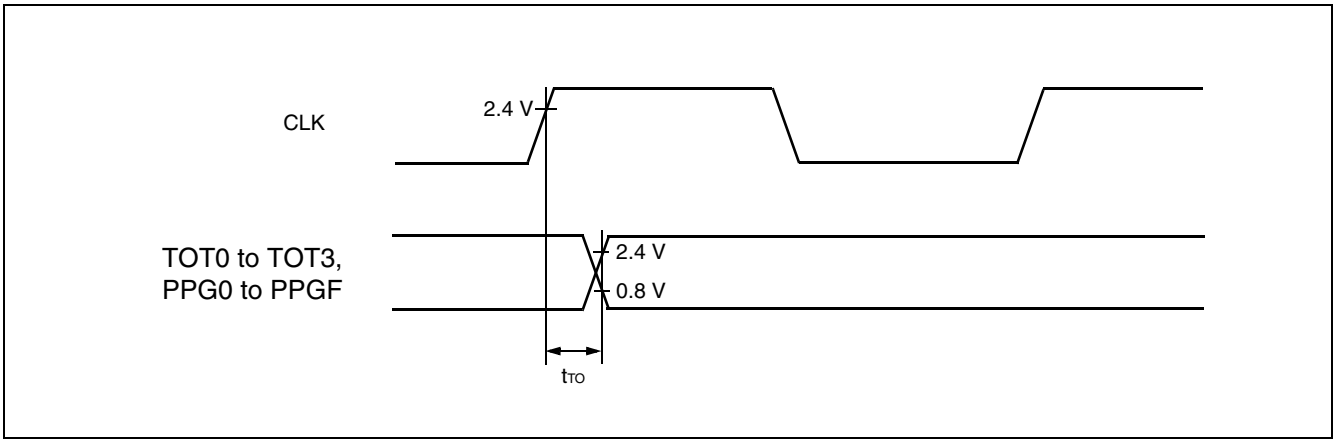
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns
	t_{TIWL}					



(12) Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



(13) I²C Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

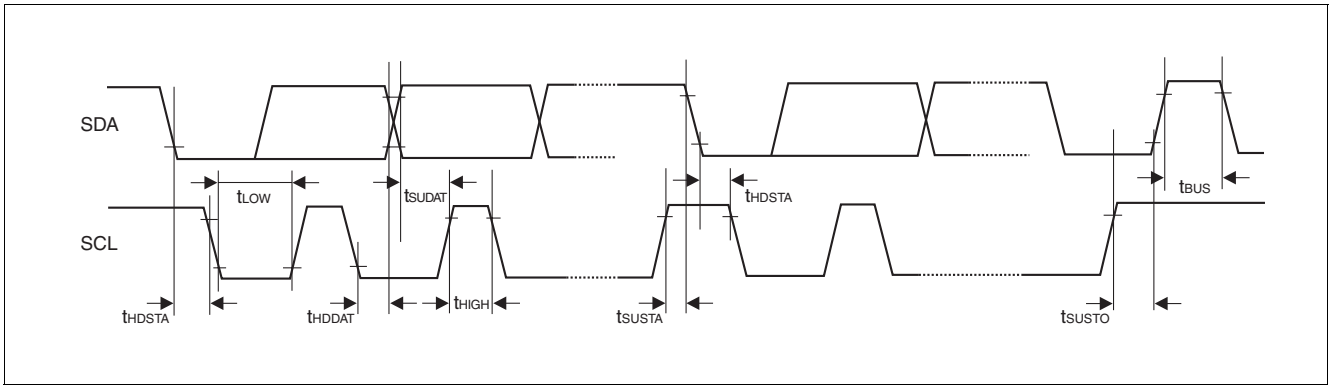
Parameter	Symbol	Condition	Standard-mode		Fast-mode*1		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*2	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	0	0.9*4	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*4 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.



5. A/D Converter

(T_A = –40 °C to +105 °C, 3.0 V ≤ AVRH – AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

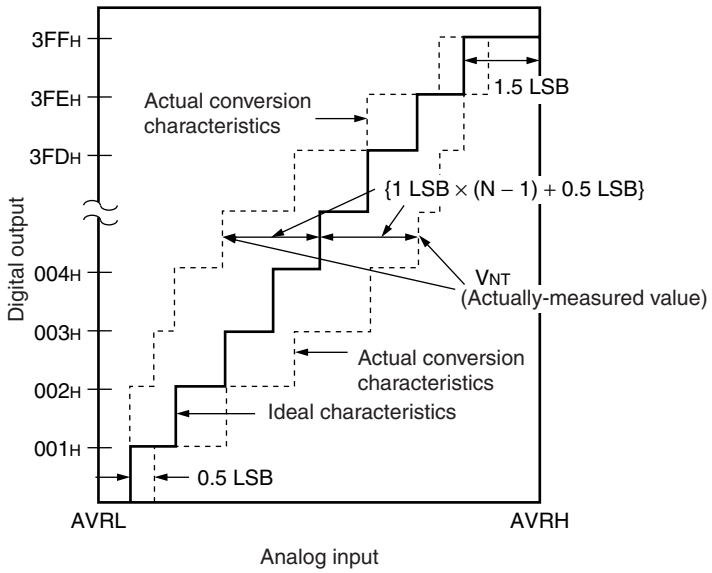
* : IF A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Note : The accuracy gets worse as AVRH – AVRL becomes smaller.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.
Zero reading voltage	:	Input voltage which results in the minimum conversion value.
Full scale reading voltage	:	Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

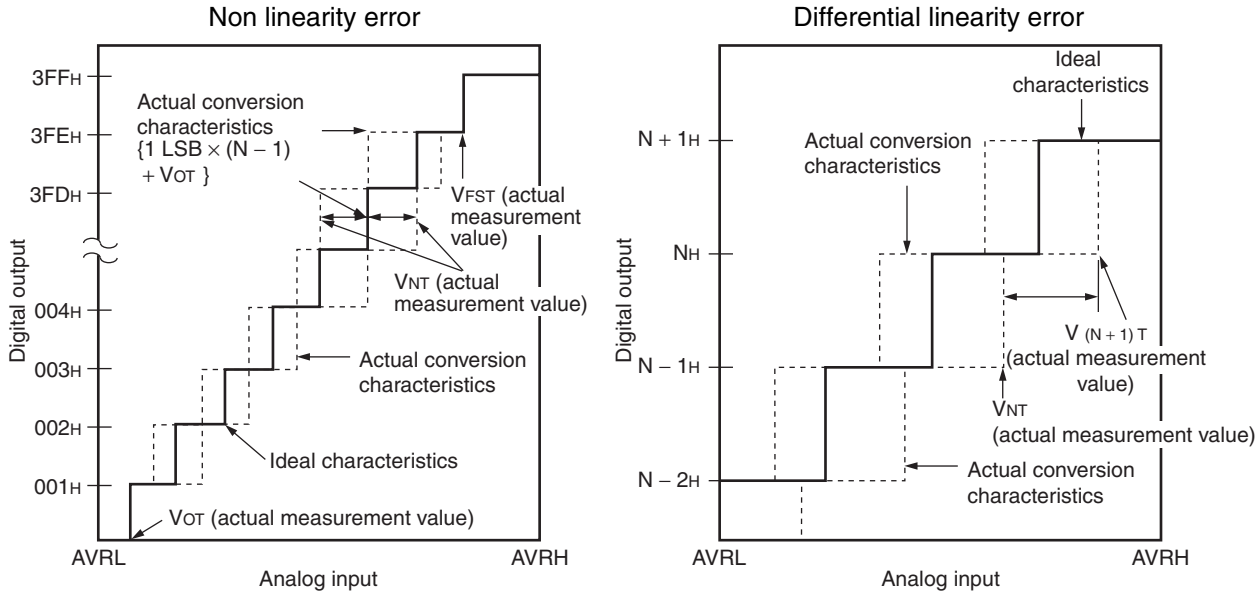
$$V_{OT}\ \text{(Ideal value)} = \text{AVRL} + 0.5\ \text{LSB}\ [\text{V}]$$

$$V_{FST}\ \text{(Ideal value)} = \text{AVRH} - 1.5\ \text{LSB}\ [\text{V}]$$

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

(Continued)

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Notes on A/D Converter Section

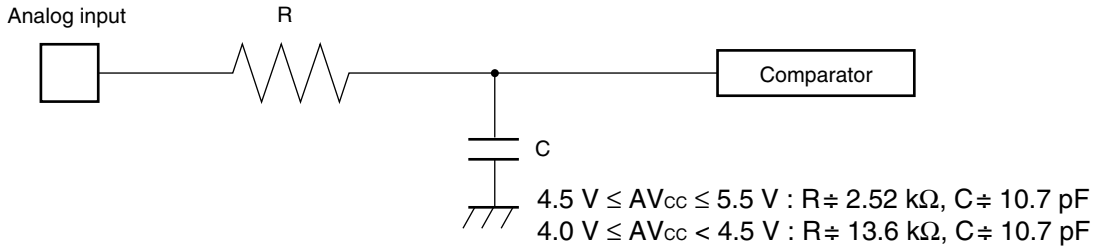
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ AV_{CC} ≤ 5.5 V, sampling period ≤ 0.5 µs)

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



Note : Use the values in the figure only as a guideline.

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Programs/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T_A = +85 °C	20	—	—	Year	*

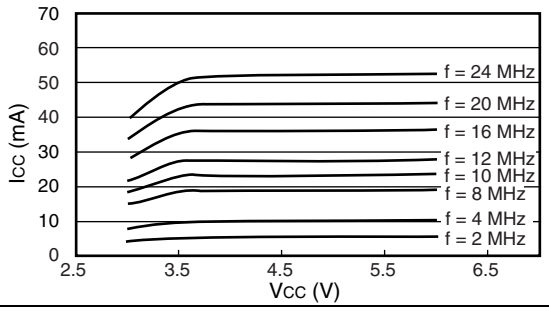
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ EXAMPLE CHARACTERISTICS

- MB90F867E, MB90F867ES

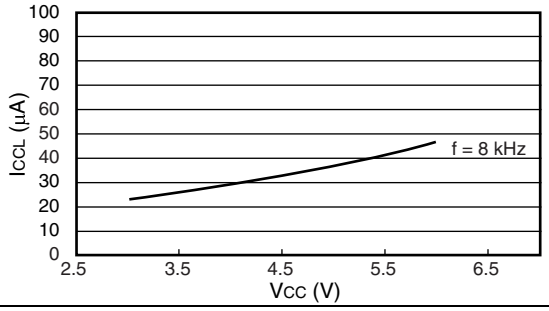
I_{CC} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



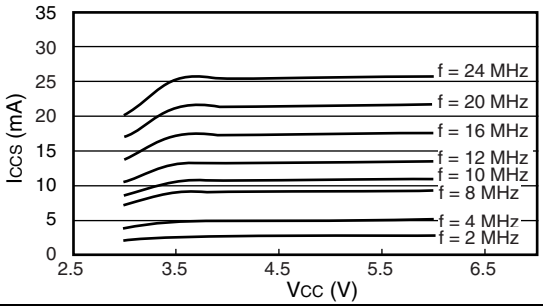
I_{CCL} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



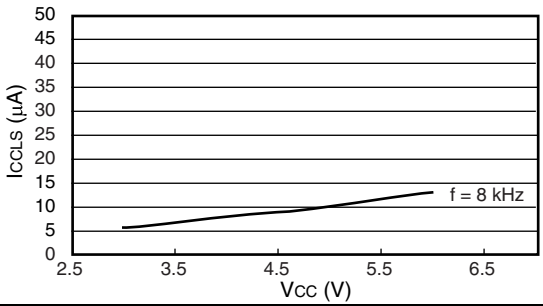
I_{CCS} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



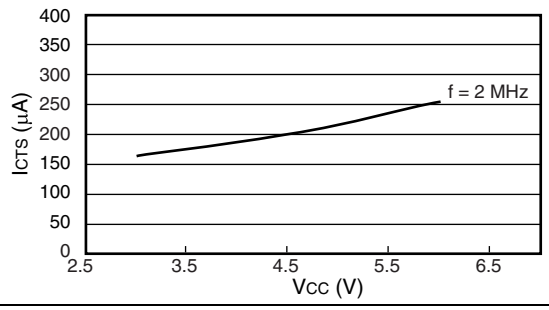
I_{CCLS} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



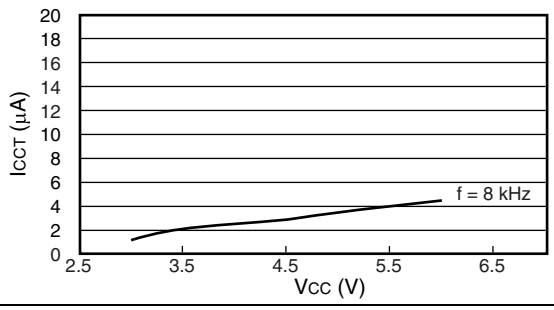
I_{CTS} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



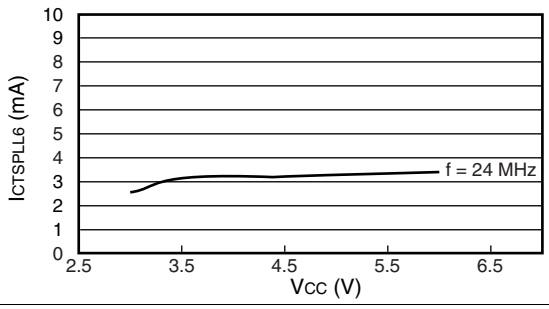
I_{CCT} – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



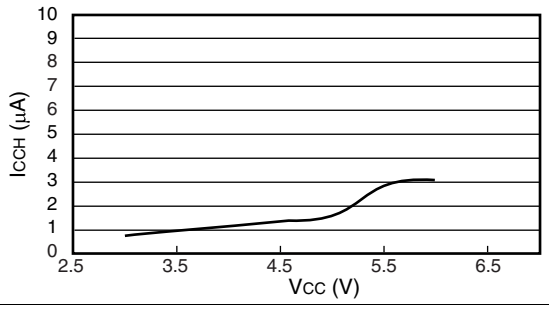
$I_{CTSPLL6}$ – V_{CC}

T_A = +25 °C, at external clock operating
f = Internal operation frequency



I_{CCH} – V_{CC}

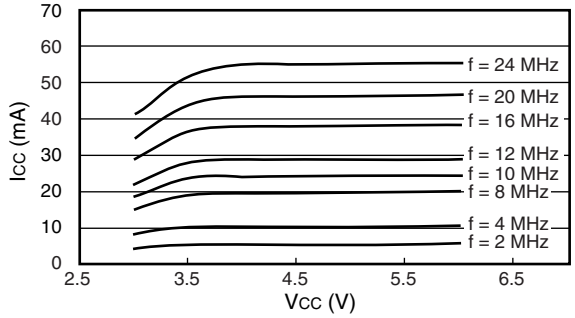
T_A = +25 °C, at stop



- MB90867E, MB90867ES

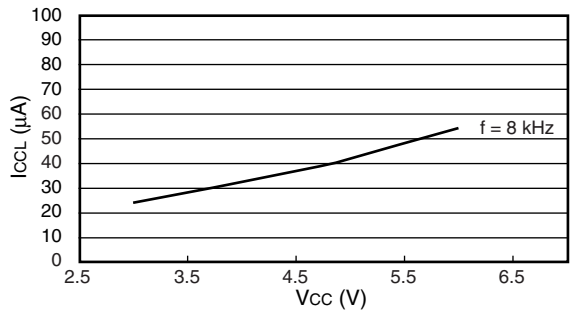
$I_{CC} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



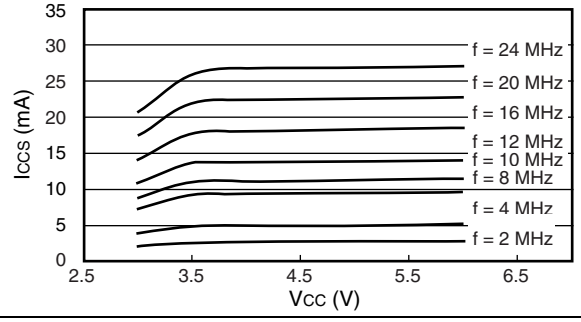
$I_{CCL} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



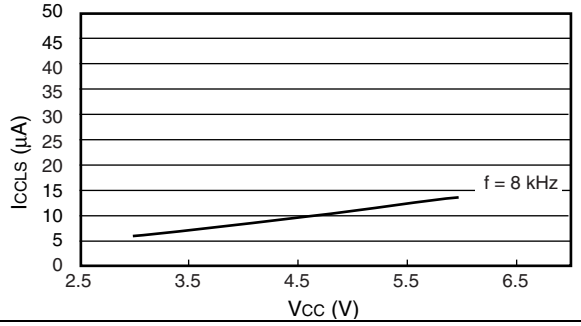
$I_{CCS} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



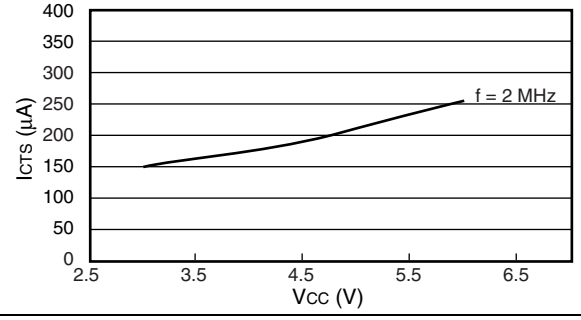
$I_{CCLS} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



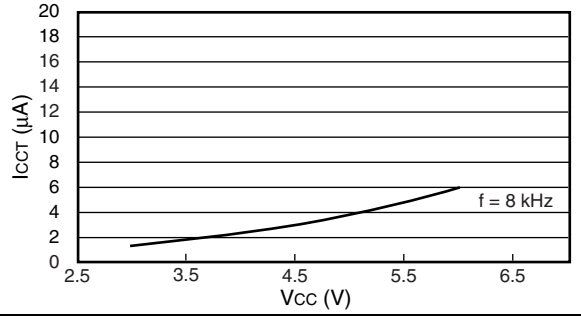
$I_{CTS} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



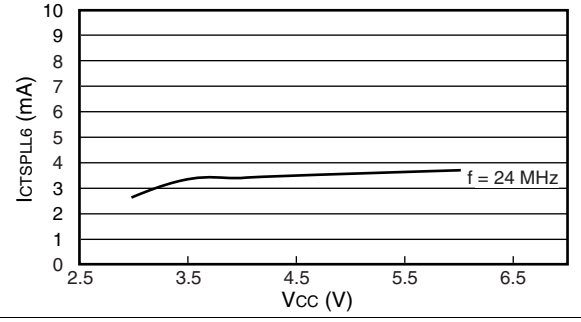
$I_{CCT} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



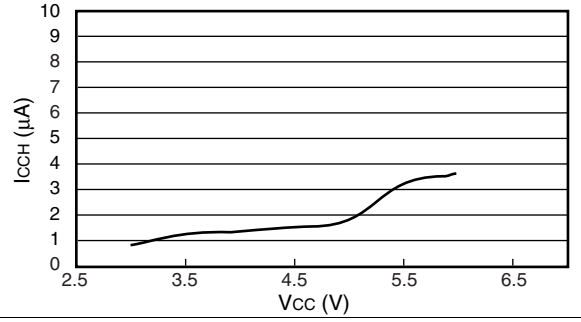
$I_{CTSPLL6} - V_{CC}$

T_A = +25 °C, at external clock operating
f = Internal operation frequency



$I_{CCH} - V_{CC}$

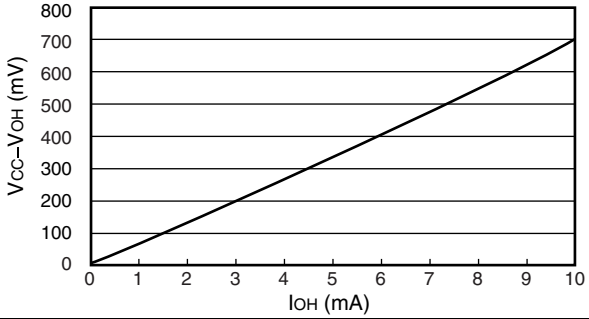
T_A = +25 °C, at stop



- I/O characteristics

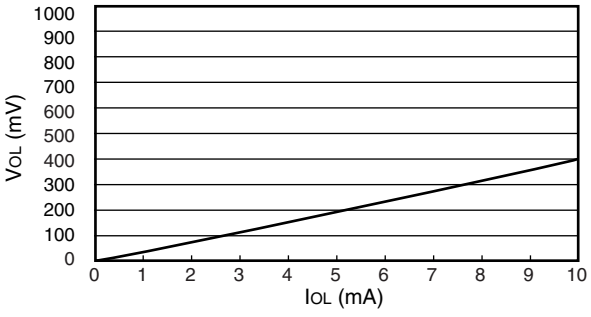
$(V_{CC}–V_{OH})$ – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



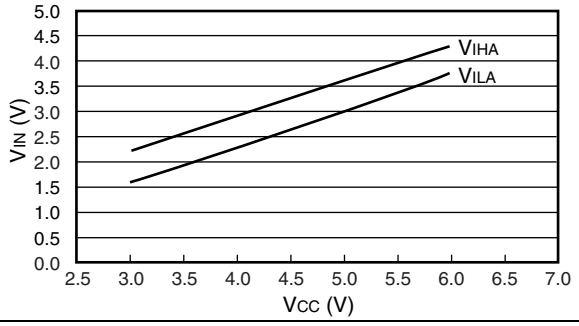
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



Automotive V_{IN} – V_{CC}

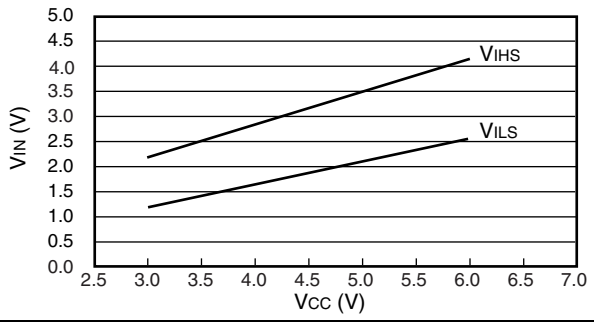
T_A = +25 °C



CMOS V_{IN} – V_{CC}

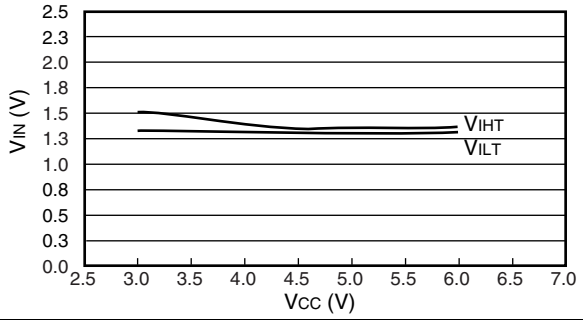
UART-SIN pin, other than I^2C pin

T_A = +25 °C



TTL V_{IN} – V_{CC}

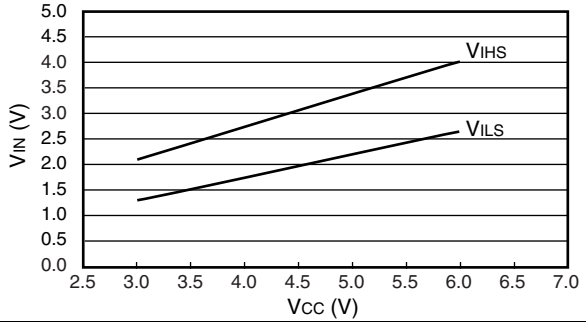
T_A = +25 °C



CMOS V_{IN} – V_{CC}

UART-SIN pin, I^2C pin

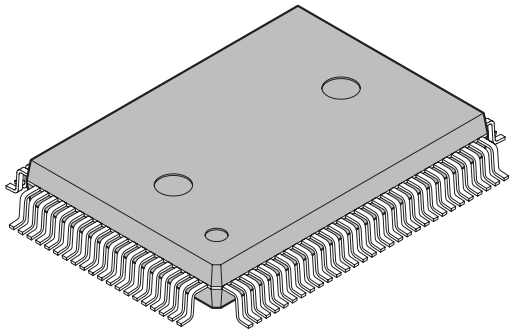
T_A = +25 °C

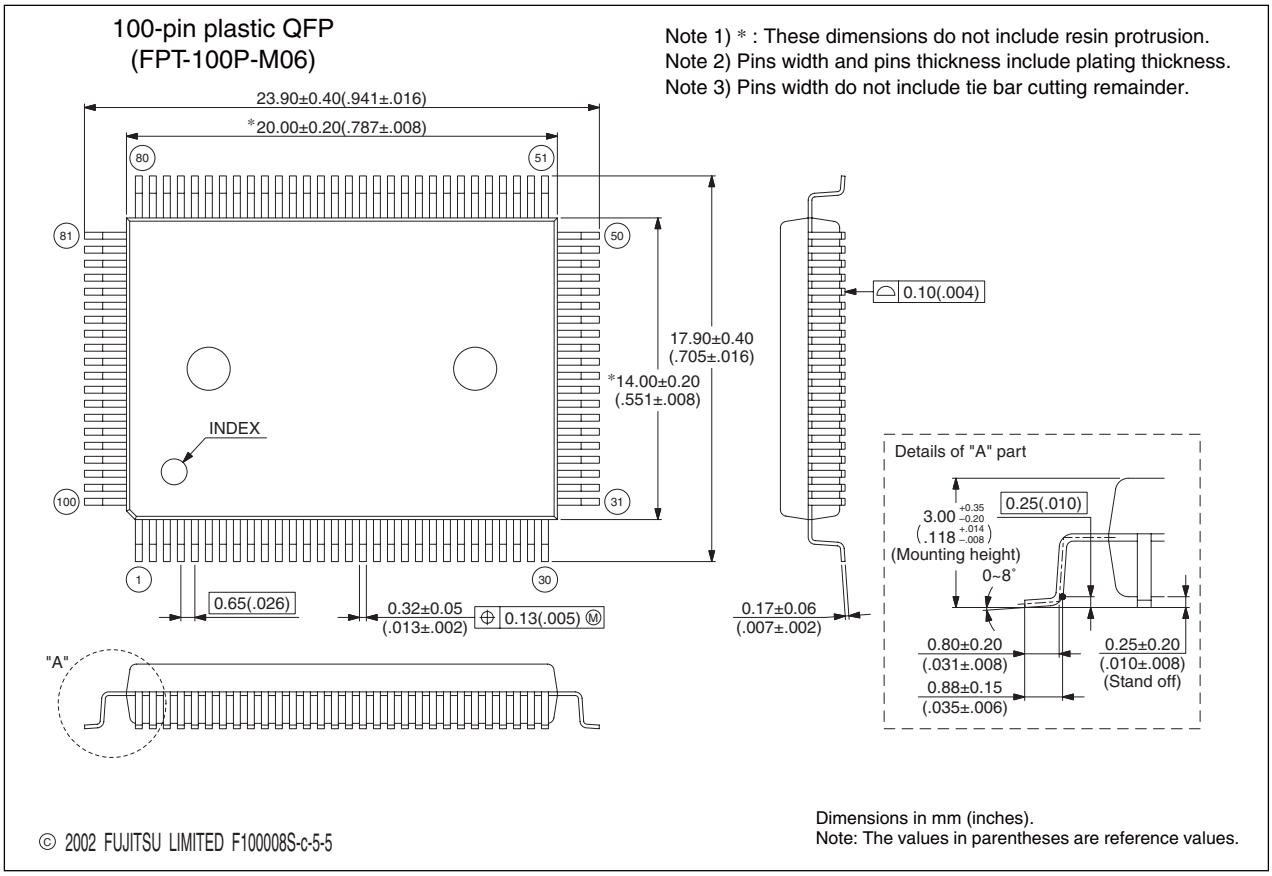


■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F867EPF	100-pin Plastic QFP (FPT-100P-M06)	Flash memory product
MB90F867ESPF		
MB90F867EPFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F867ESPFV		
MB90867EPF	100-pin Plastic QFP (FPT-100P-M06)	MASK ROM product
MB90867ESPF		
MB90867EPFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90867ESPFV		
MB90V340E-101	299-pin Ceramic PGA (PGA-299C-A01)	Evaluation product
MB90V340E-102		

■ PACKAGE DIMENSIONS

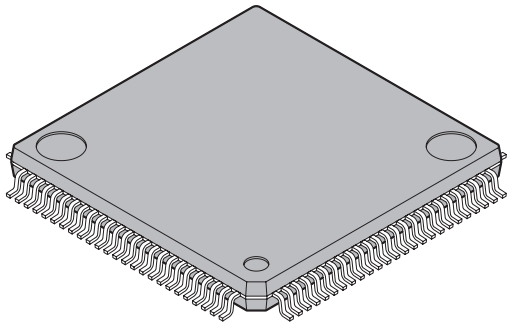
100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		

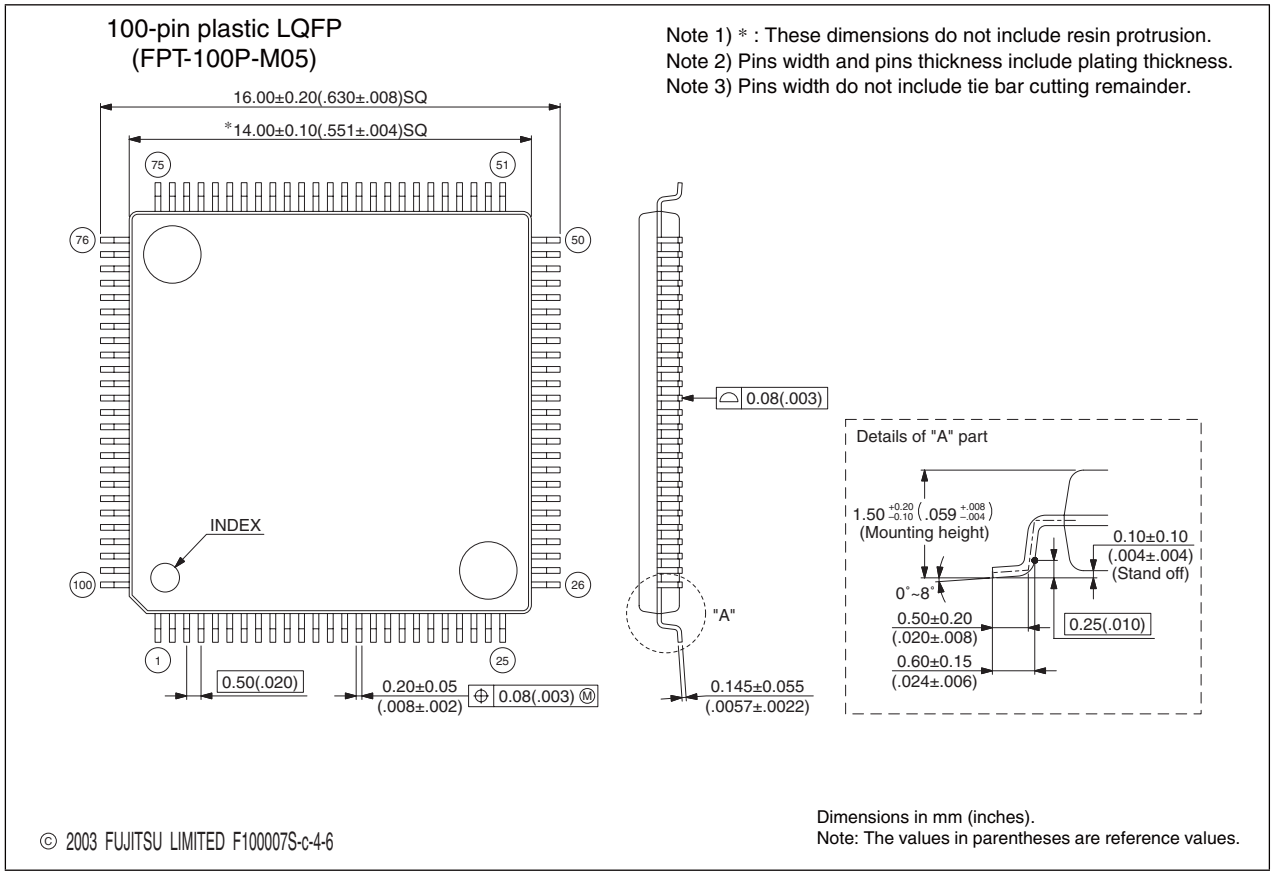


Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

(Continued)

(Continued)

100-pin plastic LQFP		
 (FPT-100P-M05)	Lead pitch	0.50 mm
	Package width × package length	14.0 × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65g
	Code (Reference)	P-LFQFP100-14×14-0.50



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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