SPECTRALINEAR

SL2309

Low Jitter and Skew 10 to 140 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 140 MHz operating frequency range
- Low output clock skew: 50ps-typ
- Low output clock jitter:
  - 50 ps-typ cycle-to-cycle jitter
- Low part-to-part output skew: 150 ps-typ
- 3.3 V power supply range
- Low power dissipation:
  - 28 mA-max at 66 MHz
  - 44 mA –max at 140 MHz
- One input drives 9 outputs organized as 4+4+1
- Select mode to bypass PLL or tri-state outputs
- SpreadThru™ PLL that allows use of SSCG
- Standard and High-Drive options
- Available in 16-pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades

Applications

- Printers and MFPs
- Digital Copiers
- PCs and Work Stations
- DTV
- Routers, Switchers and Servers
- Digital Embeded Systems

Description

The SL2309 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to nine (9) clock outputs from one (1) reference input clock, for high speed clock distribution applications.

The product has an on-chip PLL which locks to the input clock at CLKIN and receives its feedback internally from the CLKOUT pin.

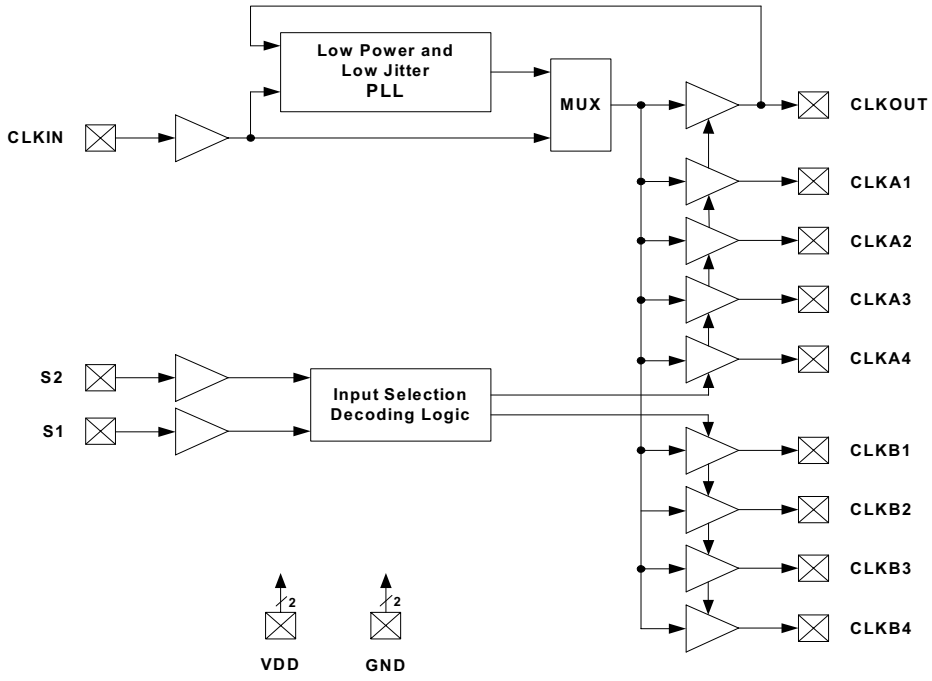
The SL2309 has two (2) clock driver banks each with four (4) clock outputs. These outputs are controlled by two (2) select input pins S1 and S2. When only four (4) outputs are needed, four (4) bank-B output clock buffers can be tri-stated to reduce power dissipation and jitter. The select inputs can also be used to tri-state both banks A and B or drive them directly from the input bypassing the PLL and making the product behave like a Non-Zero Delay Buffer (NZDB).

The high-drive (-1H) version operates up to 140MHz and low drive (-1) version operates up to 100MHz at 3.3V.

Benefits

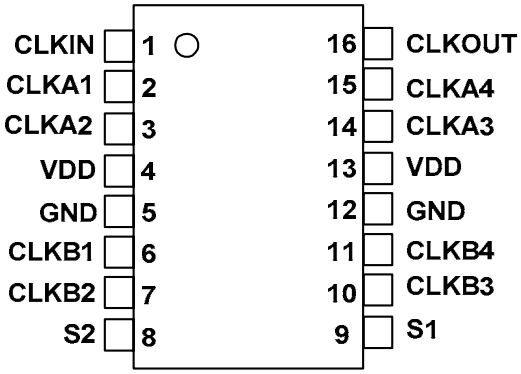
- Up to nine (9) distribution of input clock
- Standard and High-Dirive levels to control impedance level, frequency range and EMI
- Low power dissipation, jitter and skew
- Low cost

Block Diagram



2200 Laurelwood Road, Santa Clara, CA 95054 Tel: (408) 855-0555 Fax: (408) 855-0550 www.SpectraLinear.com

Pin Configuration



16-Pin SOIC and TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (250kΩ).
2	CLKA1	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
3	CLKA2	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
4	VDD	Power	3.3V Power Supply.
5	GND	Power	Power Ground.
6	CLKB1	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
7	CLKB2	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
8	S2	Input	Select Input, select pin S2. Weak pull-up (250kΩ).
9	S1	Input	Select Input, select pin S1. Weak pull-up (250kΩ).
10	CLKB3	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
11	CLKB4	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
12	GND	Power	Power Ground.
13	VDD	Power	3.3V Power Supply.
14	CLKA3	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
15	CLKA4	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
16	CLKOUT	Output	Buffered Clock Output, PLL Internal Feedback Output. Weak pull-down (250kΩ).

General Description

The SL2309 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces nine (9) output clock drivers tracking the input reference clock for systems requiring clock distribution.

in addition to CLKOUT that is used for internal PLL feedback, there are two (2) banks with four (4) outputs in each bank, bringing the number of total available output clocks to nine (9).

Input and Output Frequency Range

The input and output frequency range is the same. But, it depends on the drive and CL levels as given in the below Table 1.

Drive	CL(pF)	Min(MHz)	Max(MHz)
HIGH	15	10	140
HIGH	30	10	100
LOW	15	10	100
LOW	30	10	66

Table 1. Input/Output Frequency Range

If the input clock is DC (GND to VDD) or floating, this is detected by an input frequency detection circuitry and all nine (9) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 12µA-max supply current.

In PLL by-pass mode (S2=1 and S1=0), the detection circuit is disabled and input frequency range is 10 to 100MHz for standard (-1) drive and 10 to 140MHz for high (-1H) drive.

SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL2309 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency

Select Input Control

The SL2309 provides two (2) input select control pins called S1 (Pin-9) and S2 (Pin-8). This feature enables users to select various states of output clock banks-A and bank-B, output source and PLL shutdown features as shown in the Table 2.

The S1 (Pin-9) and S2 (Pin-8) inputs include 250 kΩ weak pull-up resistors to VDD.

PLL Bypass Mode

If the S1 and S2 pins are logic Low(0) and High(1) respectively, the on-chip PLL is shutdown and bypassed, and all the nine output clocks bank A, bank B and CLKOUT clocks are driven by directly from the reference input clock. In this operation mode SL2309 works like a non-ZDB fanout buffer. In this operation mode the input power-down detection circuit is disabled and outputs follow the input clock from DC to rated frequencies based on drive levels and load specifications.

High and Low-Drive Product Options

The SL2309 is offered with High Drive “-1H” and Standard Drive “-1” options. These drive options enable the users to control load levels, frequency range and EMI. Refer to the switching electrical tables for the details.

Skew and Zero Delay

All outputs should drive the similar load to achieve the output-to-output skew and input-to-output specifications given in the switching electrical tables. However, Zero Delay between input and outputs can be adjusted by changing the loading at CLKOUT relative to the banks A and B clocks since CLKOUT is the feedback to the PLL.

Power Supply Range (VDD)

The SL2309 is designed to operate at VDD=3.3V (+/- 10%). An internal on-chip voltage regulator is used to provide PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation.

Refer to SL23EP09 for 3.3V to 2.5V and SL23EPL09 for 1.8V power supply operations.

S2	S1	Clock A1-A4	Clock B1-4	CLKOUT	Output Source	PLL Status
0	0	Tri-state	Tri-state	Driven	PLL	On
0	1	Driven	Tri-state	Driven	PLL	On
1	0	Driven	Driven	Driven	Reference	Off
1	1	Driven	Driven	Driven	PLL	On

Table 2. Select Input Decoding

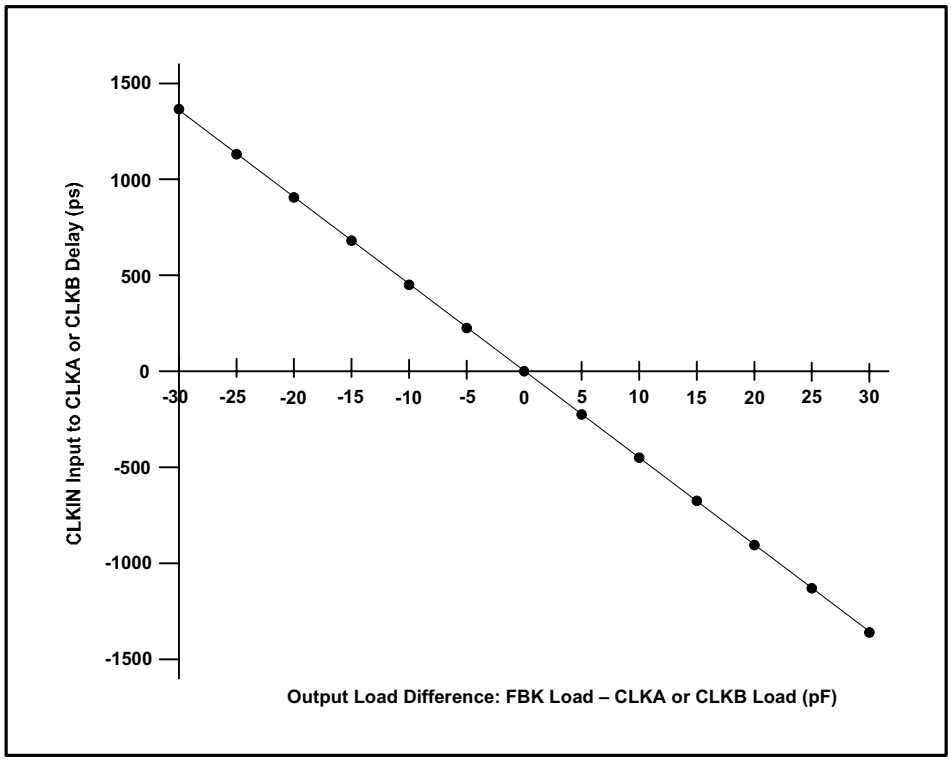


Figure 1. CLKIN Input to CLK A and B Delay
(In terms of load difference between CLKOUT and CLK A and B)

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD		– 0.5	4.6	V
All Inputs and Outputs		– 0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	85	°C
Ambient Operating Temperature	In operation, I-Grade	– 40	85	°C
Storage Temperature	No power is applied	– 65	150	°C
Junction Temperature	In operation, power is applied	–	125	°C
Soldering Temperature		–	260	°C
ESD Rating (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V

Operating Conditions: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	3.3V Supply Voltage	3.3V+/-10%	3.0	3.6	V
TA	Operating Temperature(Ambient)	Commercial	0	85	°C
		Industrial	– 40	85	°C
CLOAD	Load Capacitance	10 to 140 MHz, -1H high drive All active PLL modes	–	15	pF
		10 to 100 MHz, -1H high drive All active PLL modes	–	30	pF
		10 to 100MHz, -1 standard drive All active PLL modes	–	15	pF
		10 to 66MHz, -1 standard drive All active PLL modes	–	30	pF
CIN	Input Capacitance	S1, S2 and CLKIN pins	–	7	pF
tpu	Power-up Time	Power-up time for all VDDs to reach minimum VDD voltage (VDD=3.0V).	0.05	100	ms
CLBW	Closed-loop bandwidth	3.3V, (typical)	1.2		MHz
ZOUT	Output Impedance	3.3V, (typical), -1H high drive	22		Ω
		3.3V, (typical), -1 standard drive	32		Ω

DC Electrical Specifications: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	Supply Voltage		3.0	3.6	V
VIL	Input LOW Voltage	CLKIN, S2 and S1 Pins	–	0.8	V
VIH	Input HIGH Voltage	CLKIN, S2 and S1 pins	2.0	V_{DD}+0.3	V
IIL	Input LOW Current	CLKIN, S2 and S1 Pins, 0 < VIN < 0.8V	–	25	µA
IIH	Input HIGH Current	CLKIN, S2 and S1 Pins, VIN = VDD	–	50	µA
VOL	Output LOW Voltage (All outputs)	IOL = 8 mA (standard drive)	–	0.4	V
		IOL = 12 mA (high drive)	–	0.4	V
VOH	Output HIGH Voltage (All outputs)	IOH = –8 mA (standard drive)	2.4	–	V
		IOH = –12 mA (high drive)	2.4	–	V
IDDPD	Power Down Supply Current CLKIN=0 to VDD or floating (input will be pulled-down by 250kΩ weak pull-down on-chip resistor)	C-Grade	–	12	µA
		I-Grade	–	25	µA
IDD1	Power Supply Current	All Outputs CL=0, 33MHz CLKIN S2=S1=1 (High)	–	20	mA
IDD2	Power Supply Current	All Outputs CL=0, 66MHz CLKIN S2=S1=1 (High)	–	28	mA
IDD3	Power Supply Current	All Outputs CL=0, 100MHz CLKIN S2=S1=1 (High)	–	36	mA
IDD4	Power Supply Current	All Outputs CL=0, 140MHz CLKIN S2=S1=1 (High)	–	44	mA
RPU/D	Pull-up and Pull-down Resistors	Pins-1/2/3/6/7/8/9/10/11/14/15/16 250kΩ-typ	175	325	kΩ

Switching Specifications: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

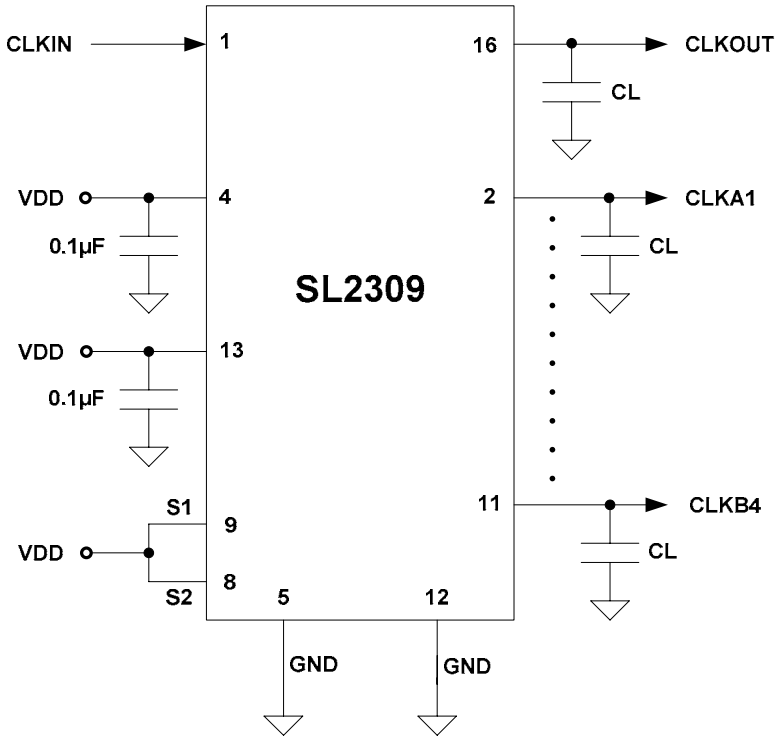
Symbol	Description	Condition	Min	Typ	Max	Unit
FMAX1	Maximum Frequency [1] (Input=Output) All Active PLL Modes	High drive (-1H). All outputs CL=15pF	10	–	140	MHz
		High drive (-1H), All outputs CL=30pF	10	–	100	MHz
		Standard drive, (-1), All outputs CL=15pf	10	–	100	MHz
		Standard drive, (-1), All outputs CL=30pf	10	–	66	MHz
FMAX2	Maximum Frequency [1] (Input=Output) PLL Bypass Mode (S2=1 and S1=0)	High drive (-1H). All outputs CL=15pF	0	–	140	MHz
		High drive (-1H), All outputs CL=30pF	0	–	100	MHz
		Standard drive, (-1), All outputs CL=15pf	0	–	100	MHz
		Standard drive, (-1), All outputs CL=30pf	0	–	66	MHz
INDC	Input Duty Cycle	Measured at 1.4V, Fout=66MHz, CL=15pF	30	50	70	%
OUTDC	Output Duty Cycle[2]	Measured at 1.4V, Fout=66MHz, CL=15pF	40	50	60	%
tr/f	Rise, Fall Time (3.3V) [2] (Measured at: 0.8 to 2.0V)	High drive (-1H), CL=15pF	–	–	1.5	ns
		High drive (-1H), CL=30pF	–	–	1.8	ns
		Standard drive (-1), CL=15pF	–	–	2.2	ns
		Standard drive (-1), CL=30pF	–	–	2.5	ns
t1	Output-to-Output Skew[2] (Measured at VDD/2)	All outputs CL=0 or equally loaded, -1 or -1H drives	–	50	120	ps
t2	Device-to-Device Skew[2] (Measured at VDD/2)	All outputs CL=0 or equally loaded, -1 or -1H drives	–	150	400	ps
t3	Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge[2] (Measured at VDD/2)	PLL Bypass mode Only when S2=1 and S1=0	1.5	5	8.7	ns
		PLL enabled All active PLL modes	–150	–	150	ps
tPLOCK	PLL Lock Time[2]	Time from 90% of VDD to valid clocks on all the output clocks	–	–	1.0	ms
CCJ	Cycle-to-cycle Jitter [2]	Fin=Fout=66 MHz, <CL=15pF, -1H drive	–	50	100	ps
		Fin=Fout=66 MHz, <CL=15pF, -1 drive	–	60	120	ps
		Fin=Fout=66 MHz, <CL=30pF, -1H drive	–	65	130	ps
		Fin=Fout=66 MHz, <CL=30pF, -1 drive	–	75	150	ps

Notes:

1. For the given maximum loading conditions. See CL in Operating Conditions Table.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor s on the component side of the PCB as close to the VDD pins as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output clocks and the load is over 1 ½ inch. The nominal impedance of the clock outputs is given on the page 4. Place the series termination resistors as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for feedback to PLL, and sees an additional 2 pF load with respect to Bank A and B clocks. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between Bank A and B clocks and CLKIN.

For minimum pin-to-pin skew, the external load at all the Bank A and B clocks must be the same.

Switching Waveforms

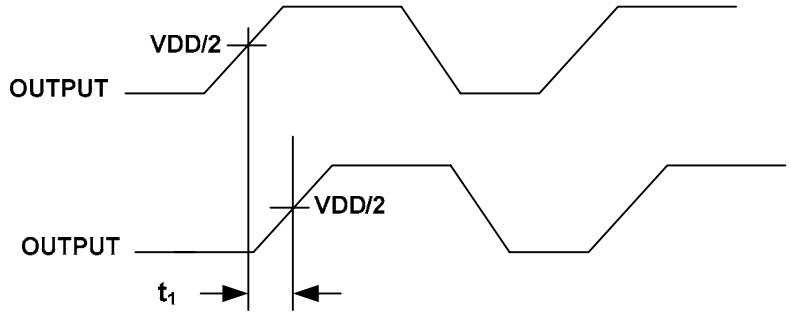


Figure 2. Output to Output Skew

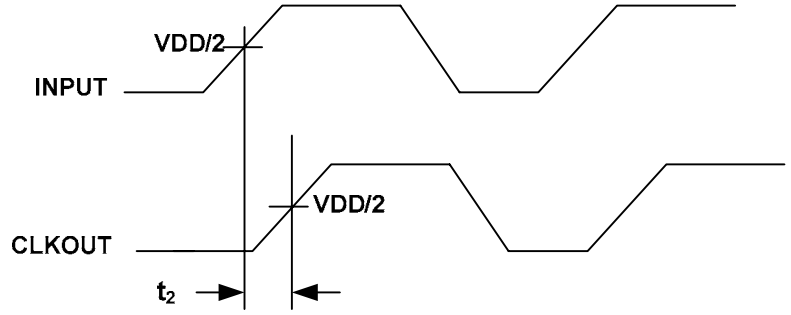


Figure 3. Input-to-Output Skew

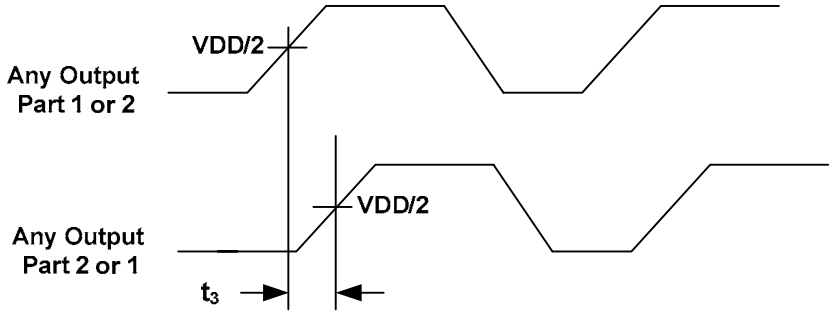
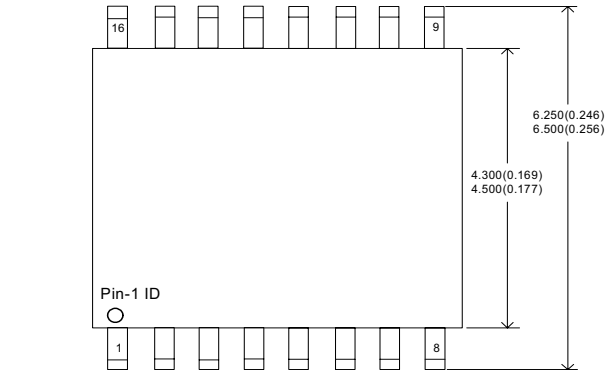


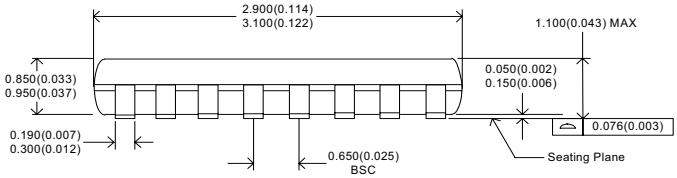
Figure 4. Part-to-Part Skew

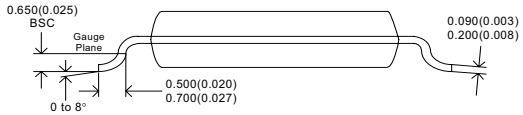
Package Drawing and Dimensions

16-Lead TSSOP (4.4mm)



Dimensions are in milimeters(inches).
Top line: (MIN) and Bottom line: (Max)



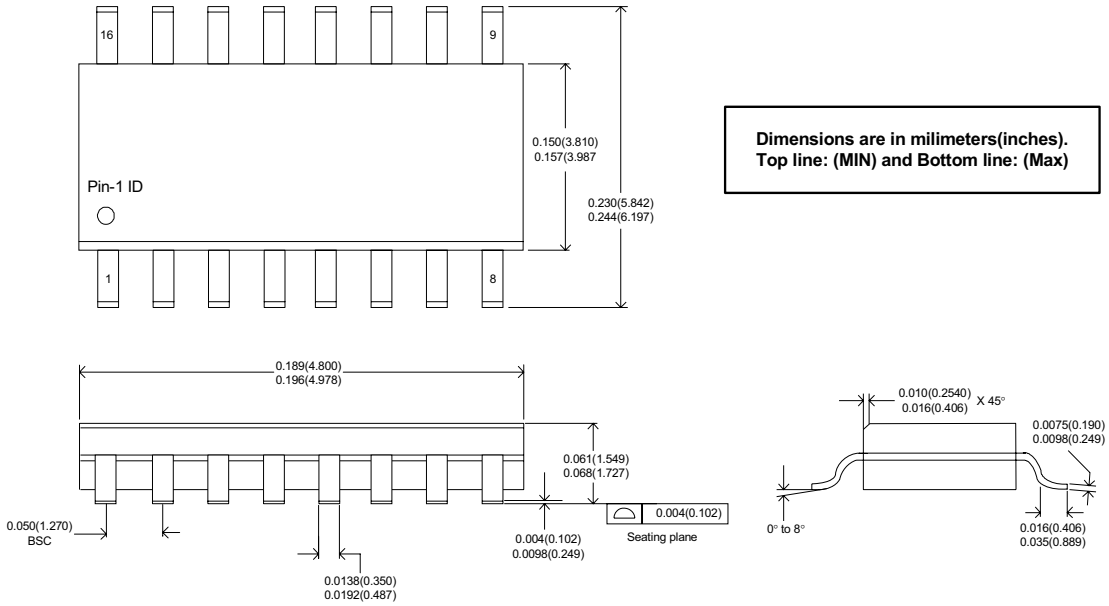


Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	80	-	°C/W
	θ JA	1m/s air flow	-	70	-	°C/W
	θ JA	3m/s air flow	-	68	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	36	-	°C/W

Package Drawing and Dimensions (Cont.)

16-Lead SOIC (150 Mil)



Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	120	-	°C/W
	θ JA	1m/s air flow	-	115	-	°C/W
	θ JA	3m/s air flow	-	105	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	60	-	°C/W

Ordering Information[3]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL2309ZC-1	SL2309ZC-1	Tube	16-pin TSSOP	0 to 70°C
SL2309ZC-1T	SL2309ZC-1	Tape and Reel	16-pin TSSOP	0 to 70°C
SL2309ZC-1H	SL2309ZC-1H	Tube	16-pin TSSOP	0 to 70°C
SL2309ZC-1HT	SL2309ZC-1H	Tape and Reel	16-pin TSSOP	0 to 70°C
SL2309ZI-1	SL2309ZI-1	Tube	16-pin TSSOP	-40 to 85°C
SL2309ZI-1T	SL2309ZI-1	Tape and Reel	16-pin TSSOP	-40 to 85°C
SL2309ZI-1H	SL2309ZI-1H	Tube	16-pin TSSOP	-40 to 85°C
SL2309ZI-1HT	SL2309ZI-1H	Tape and Reel	16-pin TSSOP	-40 to 85°C
SL2309SC-1	SL2309SC-1	Tube	16-pin SOIC	0 to 70°C
SL2309SC-1T	SL2309SC-1	Tape and Reel	16-pin SOIC	0 to 70°C
SL2309SC-1H	SL2309SC-1H	Tube	16-pin SOIC	0 to 70°C
SL2309SC-1HT	SL2309SC-1H	Tape and Reel	16-pin SOIC	0 to 70°C
SL2309SI-1	SL2309SI-1	Tube	16-pin SOIC	-40 to 85°C
SL2309SI-1T	SL2309SI-1	Tape and Reel	16-pin SOIC	-40 to 85°C
SL2309SI-1H	SL2309SI-1H	Tube	16-pin SOIC	-40 to 85°C
SL2309SI-1HT	SL2309SI-1H	Tape and Reel	16-pin SOIC	-40 to 85°C

Notes:

3. The SL2309 products are RoHS compliant.

While SLI has reviewed all information herein for accuracy and reliability, Spectra Linear Inc. assumes no responsibility for the use of any circuitry or for the infringement of any patents or other rights of third parties which would result from each use. This product is intended for use in normal commercial applications and is not warranted not is it intended for use in life support, critical medical instruments, or any other application requiring extended temperature range, high reliability, or any other extraordinary environmental requirements unless pursuant to additional processing by Spectra Linear Inc., and an expressed written agreement by Spectra Linear Inc. Spectra Linear Inc. reserves the right to change any circuitry or specification without notice.