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4BIT D-TYPE REGISTERS

GENERAL DESCRIPTION

The MMC 4076 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4076 types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disble inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at ether Output Disable input, and present a high impedance.

FEATURES

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs.

ABSOLUTE MAXIMUM RATINGS

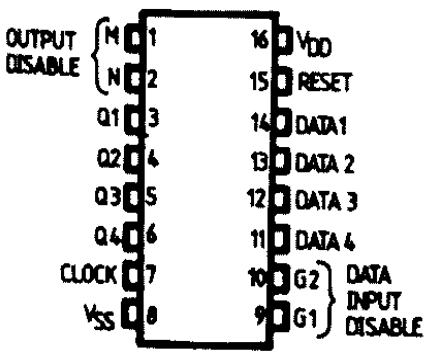
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TRUTH TABLE

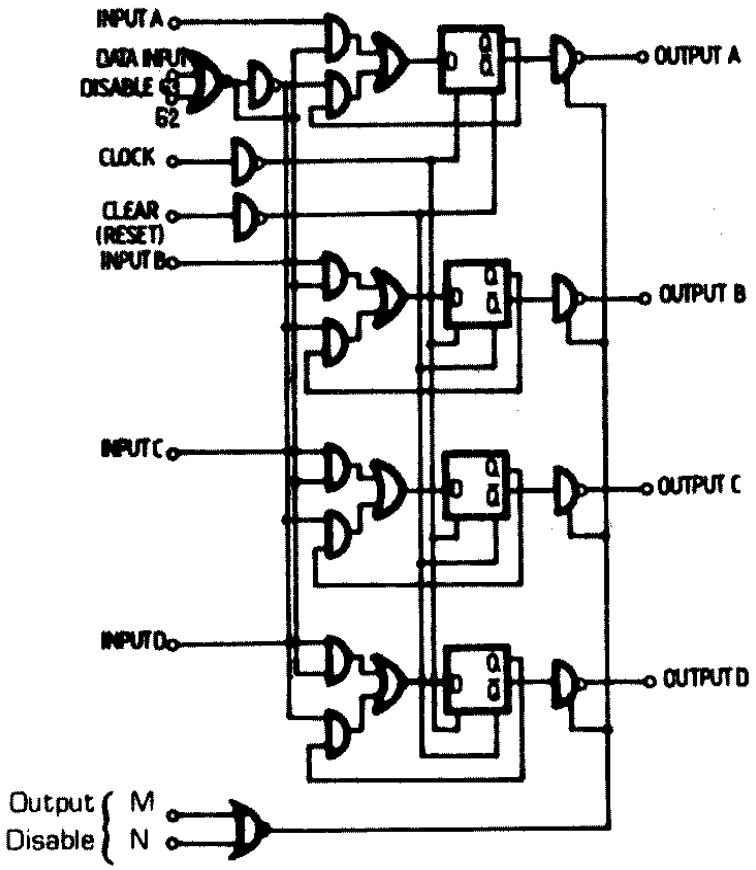
Reset	Clock	Data Input Disable G_1	Data Input Disable G_2	Data D	Next State Output Q	
1	x	x	x	x	0	
0	0	x	x	x	Q	NC
0	⌒	1	x	x	Q	NC
0	⌒	x	1	x	Q	NC
0	⌒	0	0	1	1	
0	⌒	0	0	0	0	
0	1	x	x	x	Q	NC
0	⌒	x	x	x	Q	NC

1 = High Level
0 = Low Level

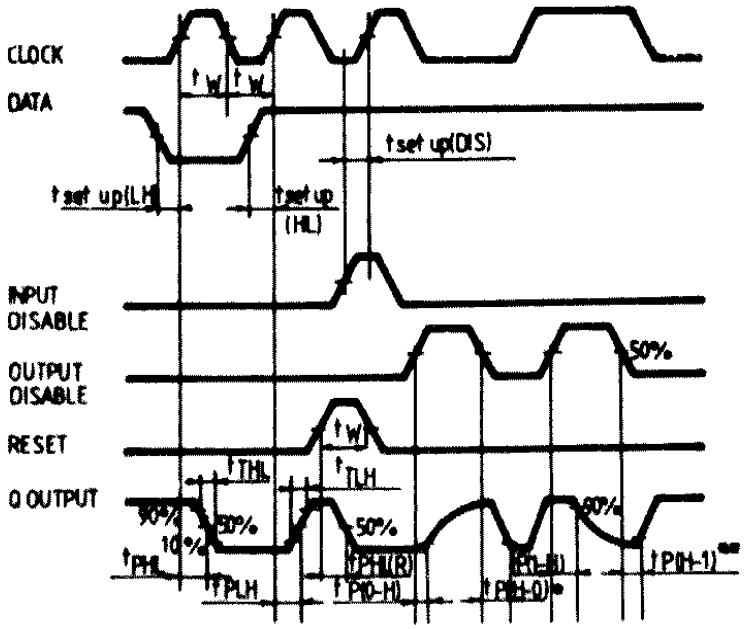
X = Don't Care
NC = No Change

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LOGIC DIAGRAM



WAVEFORMS



* Output tied to V_{DD} through 1 kΩ

** Output tied to V_{SS} through 1 kΩ

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STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$±10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$±10^{-4}$	±1.0		±7.5	

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PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{LOW}* Min.	T_{LOW}* Max.	25°C Min.	25°C Typ	25°C Max.	T_{HIGH}* Min.	T_{HIGH}* Max.	
C_I Input capacitance		Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q output)		5		300	600	ns
			10		125	250	
			15		90	180	
t_{PHL}(R)	Propagation delay time (Reset)		5		230	460	ns
			10		100	200	
			15		75	150	
$t_{P(1-Hi)}$, $t_{P(0-Hi)}$	3-state output 1 or 0 to high impedance	R_L = 1 kΩ	5		150	300	ns
			10		75	150	
			15		60	120	
$t_{P(H-1)}$, $t_{P(H-0)}$	3-state high impedance to 1 or 0 output	R_L = 1 kΩ	5		150	300	ns
			10		75	150	
			15		60	120	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_w	Clock pulse width		5	200	100		ns
			10	100	50		
			15	80	40		
t_w	Reset pulse width		5	120	60		ns
			10	50	25		
			15	40	20		
t_{setup}	Data setup time		5	200	100		ns
			10	80	40		
			15	60	30		
t_{setup}	Data input disable setup time		5	180	90		ns
			10	100	50		
			15	70	35		
f_{max}	Maximum clock frequency		5	3	6		MHz
			10	6	12		
			15	8	16		
t_r, t_f	Clock input rise or fall time		5	15			µs
			10	5			
			15	5			