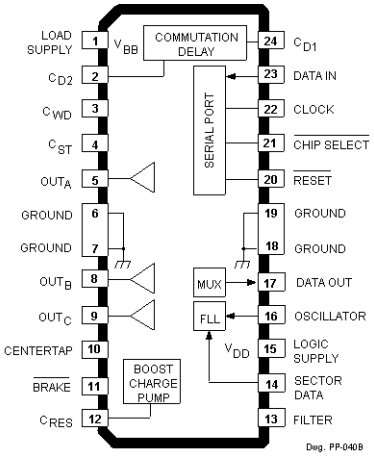
8904

Data Sheet
26301.5F

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING

A8904SLB (SOIC)



Absolute Maximum Ratings

Load Supply Voltage, V_{BB} . . . . . **15 V**
Output Current[1], I_{OUT} . . . . . **±1.4 A**
Peak Output Current (Brake)[2], $I_{OUT(BRK)}$. **±3.0 A**
Period[2] for $I_{OUT(BRK)}$ to fall from
±3.0 A to ±1.4 A . . . . . **800 ms**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
Logic Input Voltage Range, V_{IN}
(continuous) . . . . . **-0.3 V to V_{DD} + 0.3 V**
(t_w <30 ns) . . . . . **-1.0 V to V_{DD} + 1.0 V**
Package Power Dissipation, P_D . . **See Graph**
Operating Temperature, T_A . . . **-20°C to +85°C**
Junction Temperature[3], T_J . . . . . **+150°C**
Storage Temperature, T_S . . . . **-55°C to +150°C**

[1]Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.
[2]Peak output current is a transient condition that occurs during braking when the motor acts as a generator. The 3 A level is based on the maximum peak of a sine wave that is damped. The maximum period between the initial brake being applied and the current through the drivers falling to 1.4 A should not exceed 800 ms. See Braking section for more information.
[3]Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The A8904SLB and A8904SLP are three-phase brushless dc motor controller/drivers designed for applications where accurate control of high-speed motors is required. The three half-bridge outputs are low on-resistance n-channel DMOS devices capable of driving up to 1.2 A. The A8904 provides complete, reliable, self-contained back-EMF sensing, motor startup and running algorithms. A programmable digital frequency-locked loop speed control circuit together with the linear current control circuitry provides precise motor speed regulation.

A serial port allows the user to program various features and modes of operation, such as the speed control parameters, startup current limit, sleep mode, direction, and diagnostic modes.

The A8904 is fabricated in Allegro's BCD (Bipolar CMOS DMOS) process, an advanced mixed-signal technology that combines bipolar, analog and digital CMOS, and DMOS power devices. The A8904SLB is provided in a 24-lead wide-body SOIC batwing package. The A8904SLP is provided in a thin (<1.2 mm), 28-lead TSSOP package with an exposed thermal pad. Each package type is available in a lead-free version (100% matte tin leadframe).

Features

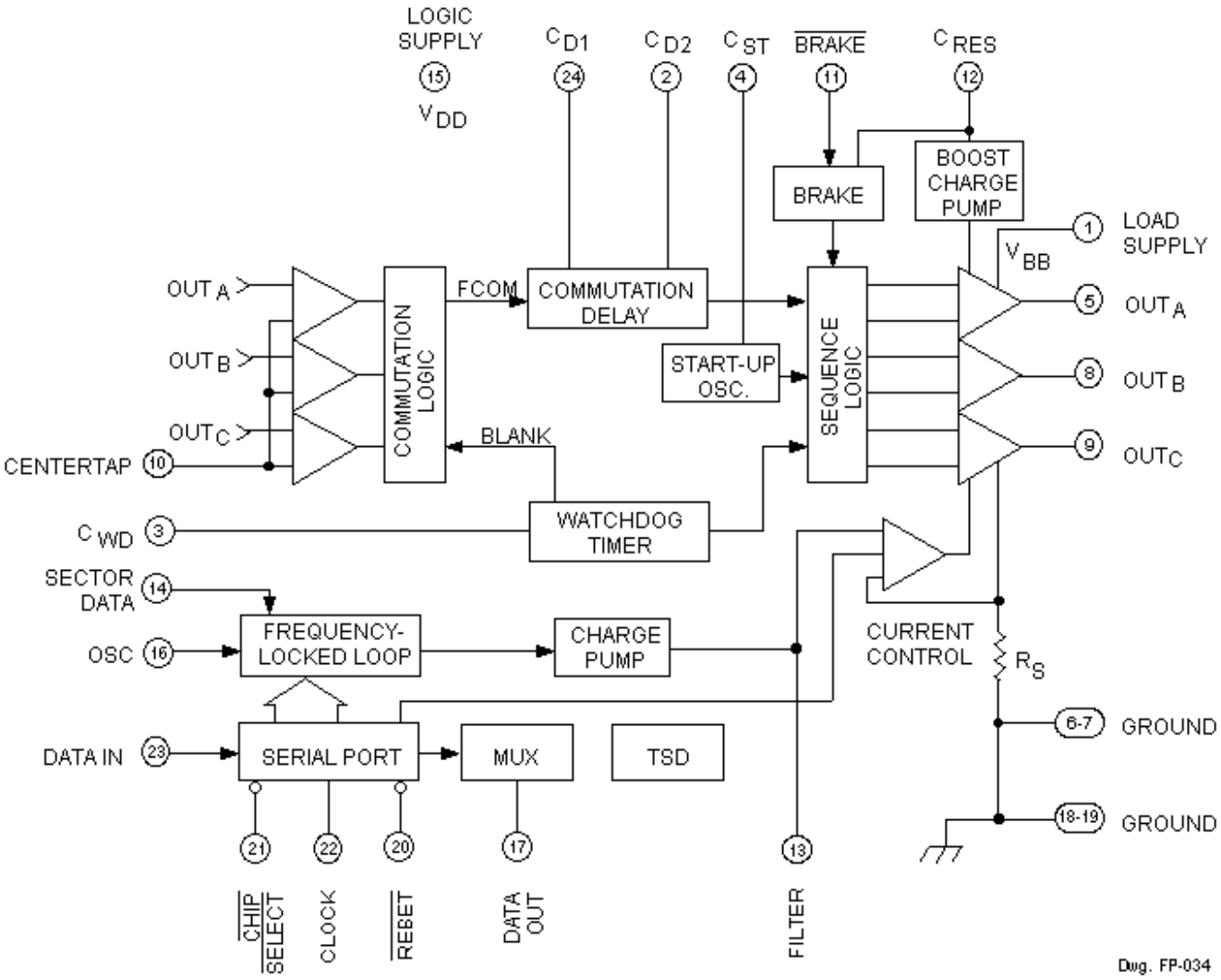
- Pin-for-pin replacement for A8902CLBA
- Startup commutation circuitry
- Sensorless commutation circuitry
- Option of external sector data tachometer signal
- Option of external speed control
- Oscillator operation up to 20 MHz
- Programmable overcurrent limit
- Transconductance gain options: 500 mA/V or 250 mA/V
- Programmable watchdog timer
- Directional control
- Serial Port Interface
- TTL-compatible inputs
- System diagnostics data out ported in real time
- Dynamic braking through serial port or external terminal

Part Number	Pb-free*	Package	Packing
A8904SLB-T	Yes	24-pin SOIC	31 per tube
A8904SLBTR-T	Yes	24-pin SOIC	450 per reel
A8904SLP-T	Yes	28-pin TSSOP	50 per tube
A8904SLPTR-T	Yes	28-pin TSSOP	4000 per reel

*Pb-based variants are being phased out of the product line. The variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadline for receipt fo LAST TIME BUY orders: April 27, 2007. These variants include: A8904SLB, A8904SLBTR, A8904SLP, and A8904SLPTR.

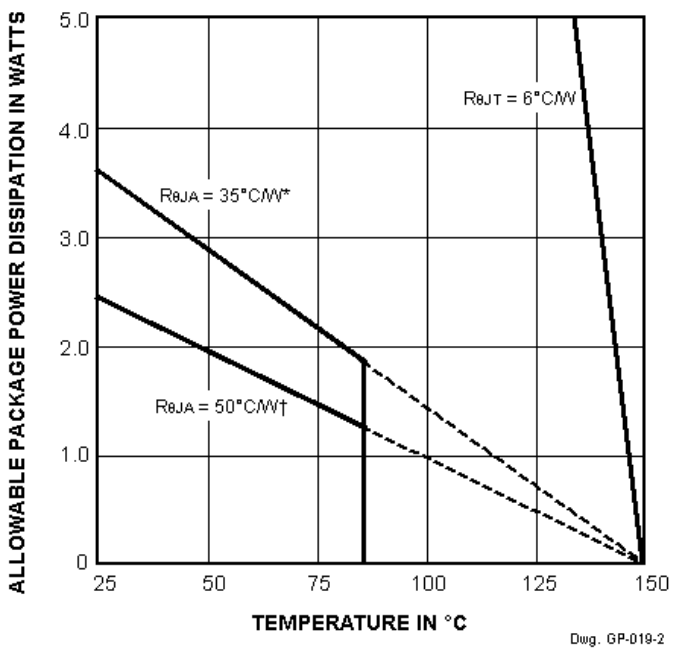
Functional Block Diagram

(A8904SLB terminal numbers shown)

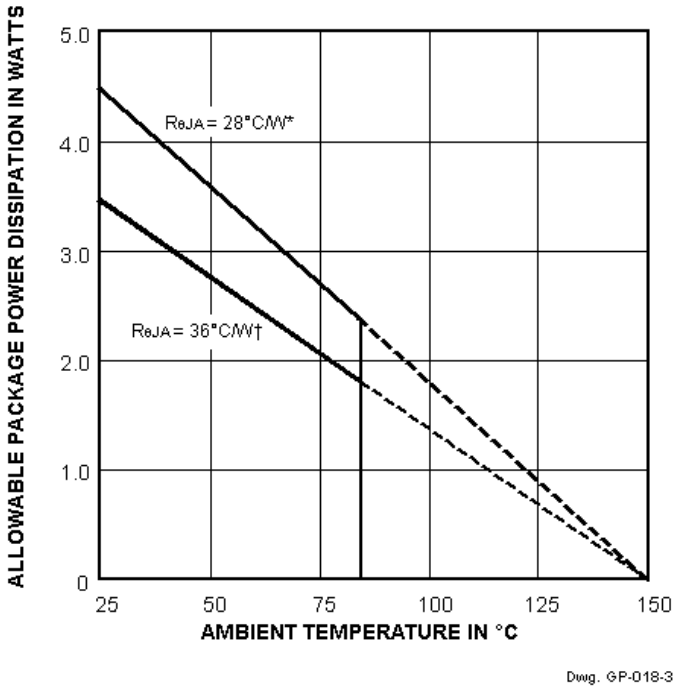


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LB (SOIC) Package



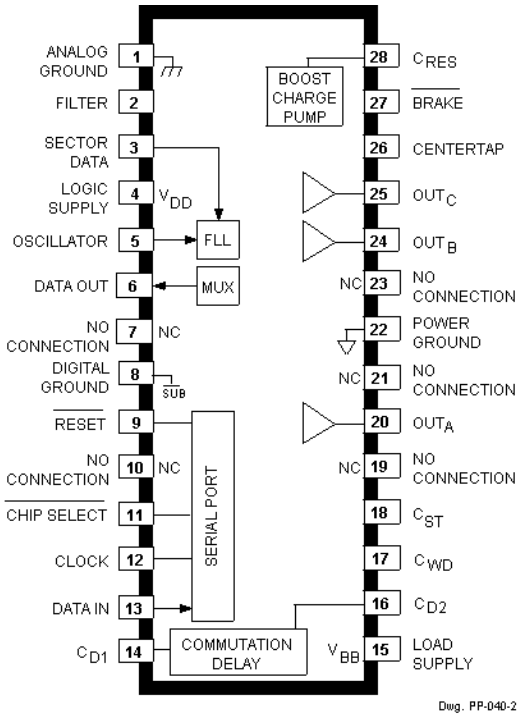
LP (TSSOP) Package



* Measured on “High-K” multi-layer PWB per JEDEC Standard JESD51-7.

† Measured on typical two-sided PWB with power tabs (LB package) or thermal pad (LP package) connected to copper foil with an area of three square inches (1935 mm^2). See Application Note 29501.5, *Improving Batwing Power Dissipation*, for additional information.

A8904SLP (TSSOP)



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep mode	—	250	500	µA
Undervoltage Threshold	UVLO	Decreasing V_{DD}	—	3.6	—	V
		Increasing V_{DD}	—	3.9	—	V
Load Supply Voltage	V_{BB}	Operating	4.0	—	14	V
Load Supply Current	I_{BB}	Operating	—	4.0	8.0	mA
		Sleep mode	—	20	30	µA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{BB} = 14 V, V_{OUT} = 14 V, sleep mode	—	200	300	µA
		V_{BB} = 14 V, V_{OUT} = 0 V	—	-2.0	-15	µA
Total Output ON Resistance (source + sink + R_S)	$r_{DS(on)}$	I_{OUT} = 600 mA	—	1.0	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	V_{BB} = 14 V, I_{OUT} = I_{OUT}(MAX), L = 3 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	SECTOR DATA, RESET, CLK,	—	—	0.8	V
	$V_{IN(1)}$	CHIP SELECT, OSC	2.0	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	±1.0	µA
BRAKE Threshold	V_{BRK}		1.5	1.75	2.0	V
BRAKE Hysteresis Current	I_{BRKL}	V_{BRK} = 750 mV	—	4.0	—	µA
BRAKE Current	I_{BRK}	Brake set, D2 = 1, I_{BRK} = 750 mV	—	20	—	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	-9.0	-10	-11	µA
		Discharging, V_{CST} = 2.5 V	—	500	—	µA
C_{ST} Threshold	V_{CSTH}	High	2.25	2.5	2.75	V
	V_{CSTL}	Low	0.85	1.0	1.15	V
Filter Current	I_{FILTER}	Charging	-9.0	-10	-11	µA
		Discharging	9.0	10	11	µA
		Leakage, V_{FILTER} = 2.5 V	—	—	±5.0	nA
Filter Threshold	$V_{FILTERTH}$		1.57	1.85	2.13	V
C_D Current (C_{D1} or C_{D2})	I_{CD}	Charging	-18	-20	-22	µA
		Discharging	32	40	48	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	1.8	2.0	2.2	—
C_D Threshold	V_{CDTH}		2.25	2.5	2.75	V
C_D Input Leakage	I_{CDIL}		—	—	1.0	µA

Continued next page …

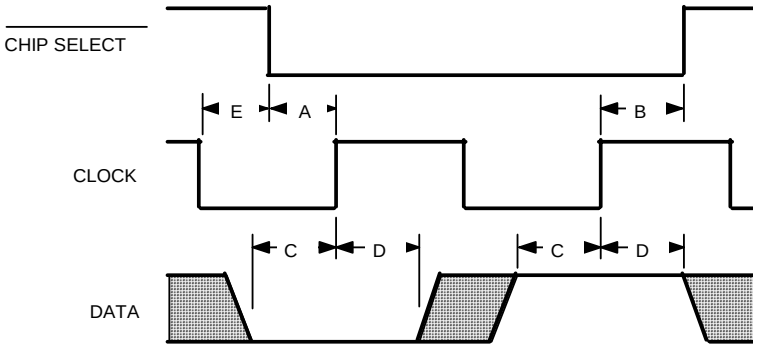
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ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
C_{WD} Current	I_{CWD}	Charging, D26 = 0, D27 = 0	-9.0	-10	-11	µA
		Charging, D26 = 0, D27 =1	-18	-20	-22	µA
		Charging, D26 = 1 D27 = 0	-27	-30	-33	µA
		Charging, D26 = 1, D27 =1	-36	-40	-44	µA
C_{WD} Threshold Voltage	V_{TL}		0.22	0.25	0.28	V
	V_{TH}		2.25	2.5	2.75	V
Max. FLL Oscillator Frequency	f_{OSC}		20*	—	—	MHz
Oscillator High Duration	ton		20	—	—	ns
Oscillator Low Duration	toff		20	—	—	ns
Maximum Output Current	I_{OUT}(MAX)	D3 = 0, D4 = 0, D28 = 0	1.0	1.2	1.4	A
		D3 = 0, D4 = 1, D28 = 0	0.9	1.0	1.1	A
		D3 = 1, D4 = 0, D28 = 0	500	600	700	mA
		D3 = 1, D4 = 1, D28 = 0	—	250	—	mA
		D3 = 0, D4 = 0, D28 = 1	500	600	700	mA
		D3 = 0, D4 = 1, D28 = 1	415	500	585	mA
		D3 = 1, D4 = 0, D28 = 1	—	300	—	mA
		D3 = 1, D4 = 1, D28 = 1	—	125	—	mA
Transconductance Gain	g_m	D28 = 1	210	250	290	mA/V
		D28 = 0	420	500	580	mA/V
Centertap Resistors	R_{CT}		5.0	10	13	kΩ
Back-EMF Threshold with respect to V_{CTAP} at FCOM transition	—		5.0	20	37	mV
			-5.0	-20	-37	mV

Negative current is defined as coming out of (sourcing) the specified device terminal.
* Operation at an oscillator frequency greater than the specified minimum value is possible but not waranteed.

Serial Port Timing Conditions



Dwg. W

A. Minimum CHIP SELECT setup time before CLOCK rising edge ..... **100 ns**
B. Minimum CHIP SELECT hold time after CLOCK rising edge ..... **150 ns**
C. Minimum DATA setup time before CLOCK rising edge ..... **150 ns**
D. Minimum DATA hold time after CLOCK rising edge ..... **150 ns**
E. Minimum CLOCK low time before CHIP SELECT ..... **50 ns**
F. Maximum CLOCK frequency ..... **3.3 MHz**
G. Minimum CHIP SELECT high time ..... **500 ns**

Note: the A8904 can be directly used in an existing A8902–A application, as the five most significant bits are reset to zero, which is the default condition for A8902–A operation. The only consideration when using the A8904 in an A8902-A application, is to ensure the minimum CHIP SELECT high time is at least 500 ns.

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Terminal Functions

Terminal Name	Function	A8904SLB (SOIC)	A8904SLP (TSSOP)
LOAD SUPPLY	V_{BB}; the 5 V or 12 V motor supply.	1	15
C_{D2}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.	2	16
C_{WD}	Timing capacitor used by the watchdog circuit to blank out the back-EMF comparators during commutation transients, and to detect incorrect motor position.	3	17
C_{ST}	Startup oscillator timing capacitor.	4	18
NC	No(internal) connection.	–	19
OUT_A	Power amplifier A output to motor.	5	20
NC	No (internal) connection.	–	21
GROUND	Power and logic ground and thermal heat sink.	6-7	–
POWER GROUND	Power ground.	–	22*
NC	No (internal) connection.	–	23
OUT_B	Power amplifier B output to motor.	8	24
OUT_C	Power amplifier C output to motor.	9	25
CENTERTAP	Motor centertap connection for back-EMF detection circuitry.	10	26
$\overline{\text{BRAKE}}$	Active low turns ON all three sink drivers shorting the motor windings to ground. External capacitor and resistor at BRAKE provide brake delay. The brake function can also be controlled via the serial port.	11	27
C_{RES}	External reservoir capacitor used to hold charge to drive the source drivers' gates. Also provides power for brake circuit.	12	28
ANALOG GROUND	Analog ground.	–	1*
FILTER	Analog voltage input/output to control motor current. Also, compensation node for internal speed control loop.	13	2
SECTOR DATA	External tachometer input. Can use sector or index pulses from disk to provide precise motor speed feedback to internal frequency-locked loop.	14	3
LOGIC SUPPLY	V_{DD}; the 5 V logic supply.	15	4
OSCILLATOR	Clock input for the speed reference counter.	16	5
DATA OUT	Thermal shutdown indicator, FCOM, TACH, or SYNC signals available in real time, controlled by 2-bit multiplexer via serial port.	17	6
NC	No (internal) connection.	–	7
GROUND	Power and logic ground and thermal heat sink.	18-19	–
DIGITAL GROUND	Logic ground.	–	8*
$\overline{\text{RESET}}$	When pulled low forces the chip into sleep mode; clears all serial port bits.	20	9
NC	No (internal) connection.	–	10
$\overline{\text{CHIP SELECT}}$	Strobe input (active low) for data word.	21	11
CLOCK	Clock input for serial port.	22	12
DATA IN	Sequential data input for the serial port.	23	13
C_{D1}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.	24	14

* For the A8904SLP, ground terminals 1, 8, and 22 must be connected together externally.

Functional Description

Overview of operation. Each electrical revolution contains six states that control the three half-bridge outputs. Optimized switching from state to state is achieved through the adaptive commutation circuitry. During any state, one output is high, one is low and the other is high impedance. The back-EMF at the high-impedance output is sensed and compared to the voltage of the centertap and when the two signals are equivalent, the FCOM signal toggles. A controlled delay is then introduced before the sequencer commutates into the next state.

Linear current-mode control is employed to provide precision control of the motor speed while maintaining extremely low electrical noise emissions. The speed control is realized through a frequency-locked loop that processes the sensed back-EMF signals from the stator phases to eventually produce a TACH signal. The TACH signal is then compared to the desired programmed speed, to produce an error. The error signal is then used to linearly control the current through the low-side DMOS power devices to obtain the correct speed.

Alternative control schemes can be introduced, giving the user maximum flexibility and optimization for each application. An external tachometer signal applied to the SECTOR DATA input, along with the internal speed reference can be used for high-precision speed control. As another alternative, the user can introduce external speed control by driving the FILTER terminal directly.

Start-up routines are inherent in the solution to guarantee reliable start-up. During start-up, a YANK feature allows rapid transition to the nominal operating condition on the FILTER terminal. This feature is also available when the external speed control is used.

Dynamic braking can be introduced by either the external BRAKE terminal or through the brake bit in the serial port.

A serial port allows the user to program various features and modes of operation, such as motor speed, internal or external speed control, internal or external speed reference, current limit, sleep mode, direction, charge current (for blanking pulse), motor poles, transconductance gain, and various diagnostic outputs.

Full device protection is incorporated, including programmable overcurrent limit, thermal shutdown, and undervoltage shutdown on the logic supply.

Power outputs. The power outputs of the A8904 are n-channel DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1 Ω. An internal charge pump provides a voltage rail above the load supply for driving the high-side DMOS gates. Intrinsic ground clamp and flyback diodes provide protection when switching inductive loads. These diodes will also rectify the motor back-EMF during power-down conditions. If necessary, a transient voltage supply can be provided, by connecting an external Schottky power diode or pass FET in series, between the power source and the load supply (V_{BB}). This FET or diode effectively isolates the low impedance path through the power source. A filter capacitor is also required to 'hold up' the rectified signal, and is connected between the load supply and ground.

Back-EMF sensing motor startup and running algorithm. The A8904 provides a complete self-contained back-EMF sensing, startup and running commutation scheme. A state machine with six states, (shown in the tables below for both forward and reverse direction) controls the three half-bridge outputs. In each state, one output is high (sourcing current), one low (sinking current), and one is OFF (high impedance or 'Z'). Motor back-EMF is sensed at the output that is OFF.

Sequencer State (forward direction)	OUT_A	OUT_B	OUT_C
1	High	Z	Low
2	High	Low	Z
3	Z	Low	High
4	Low	Z	High
5	Low	High	Z
6	Z	High	Low

Sequencer State (reverse direction)	OUT_A	OUT_B	OUT_C
1	High	Z	Low
6	Z	High	Low
5	Low	High	Z
4	Low	Z	High
3	Z	Low	High
2	High	Low	Z

At start-up, the outputs are always enabled in state 1. The back-EMF is examined at the OFF output by comparing the output voltage to the motor centertap voltage at CENTERTAP. The motor will then either step forward, step backward or remain stationary (if in a null-torque position).

If the motor does not move during the initial start-up state, the outputs are commutated automatically by the start-up oscillator. When suitable back-EMF signals are detected, the start-up oscillator is overridden and the corresponding timing clock is generated, providing synchronous back-EMF commutation. The start-up oscillator period is determined by

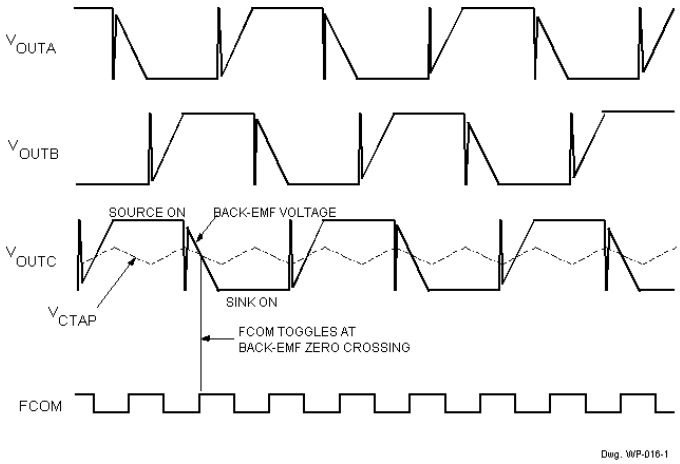
$$t_{CST} = (V_{CSTH} - V_{CSTL}) \times C_{ST} / I_{ST(charge)}$$

where C_{ST} is the start-up capacitor.

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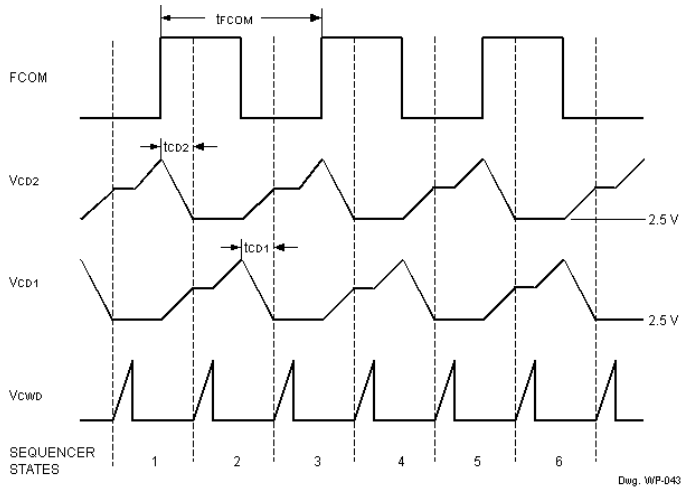
Functional Description (cont'd)

If the motor moves, the back-EMF detection and direction circuit waits for the correct polarity of back-EMF zero crossing (output crossing through centertap). If the correct polarity of back-EMF is not detected, a watchdog circuit commutates the output until the correct back-EMF is detected. Correct back-EMF sensing is indicated by the FCOM signal, which toggles every time the back-EMF completes a zero crossing (see waveforms below). FCOM is available at the DATA OUT terminal.



True back-EMF zero crossings are used by the adaptive commutation delay circuit to advance the state sequencer (commutate) at the proper time to synchronously run the motor. See next section.

Adaptive commutation delay. The adaptive commutation delay circuit uses the back-EMF zero-crossing indicator signal (FCOM) to determine an optimal commutation time for efficient synchronous switching of the output drivers. When the FCOM signal changes state, one of the delay capacitors (C_{D1} or C_{D2}) is discharged at approximately twice the rate of the charging current. When the capacitor reaches the 2.5 V threshold, a commutation occurs. During this discharge period, the other delay capacitor is being charged in anticipation of the next FCOM state change. In addition, there is an interruption to the charging, which is set by the blanking duration (see waveform below, $V_{CWD,}$ and next section). This additional charging delay causes the commutation to occur at slightly less than 50% of the FCOM on or off duration, to compensate for delays caused by winding inductance.



The typical delta voltage change during normal operation in the commutation capacitors (C_{D1} & C_{D2}), will range between 1.5 V and 2.0 V. The commutation capacitor values can be determined from:

$$C_{DX} = I_{CD} \times t / V_{CD}$$

where V_{CD} = 1.5 V, I_{CD} = 20 µA, and t = (60/rpm)/(#motor poles x 3), duration of each state.

To avoid the capacitors charging to the supply rail, the value selected should provide adequate margin, taking into account the effects of capacitor tolerance, charging current, etc.

Blanking and watchdog timing functions. The blanking and watchdog timing functions are derived from one timing capacitor C_{WD}.

During normal commutation, at the beginning of each new sequencer state, a blanking signal is created until the watchdog capacitor C_{WD} is charged to the threshold V_{TL} (see waveforms below). This blanking signal prohibits the back-EMF comparators from tripping due to the discharging of inductive energy and voltage settling transients during sequence state transitions. The duration of this blanking signal depends on the size of the C_{WD} capacitor and the programmed charge current, I_{CWD} (via D26-27). This blanking pulse also interrupts the commutation delay capacitors C_{D1} and C_{D2} from charging (see previous section).

The ability to select the minimum charge current for C_{WD} is particularly useful during start-up, where the duration of the diode recirculation current is highest. In applications where high motor speeds are experienced, the charge current can be increased so that the blanking period does not encroach significantly into the period of each sequencer state and does not cause

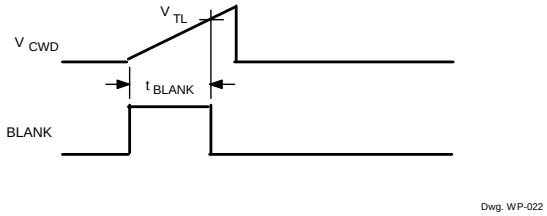
Functional Description (cont'd)

unbalance in the commutation points.

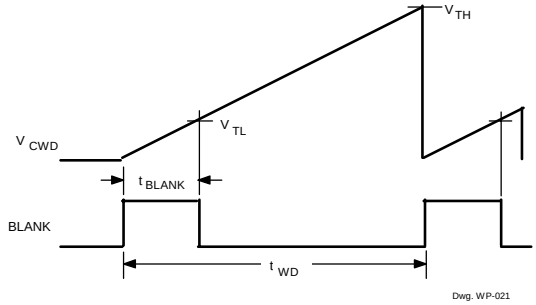
It is recommended to select the value of C_{WD} in the actual application circuit with the A8904 put into step mode. C_{ST} should be reselected (only for this test), to be between 4.7 µF and 10 µF, so that the motor comes to rest between steps and the maximum diode conduction time can be measured. The value of C_{WD} can be determined as:

$$C_{WD} = I_{CWD} \times t_d / V_{TL}$$

where t_d = measured diode conduction, I_{CWD} = charge current at start-up, and V_{TL} = 250 mV.



Normal commutation



Watchdog-triggered commutation

After the watchdog capacitor C_{WD} charges to the V_{TL} threshold, and if the correct polarity of back-EMF signal is detected, the back-EMF detection circuit discharges C_{WD} to zero volts (see waveform above) and the circuit is ready to detect the next back-EMF zero crossing.

If the correct polarity of back-EMF is not detected between the blanking period, $t_{BLANK,}$ and the watchdog period, t_{WD}, then the back-EMF detection circuit does not allow the watchdog capacitor C_{WD} to be discharged and the watchdog circuit commutates the outputs to the next sequencer state (see waveform above). This mode of operation continues until a suitable back-EMF signal is detected. This function is useful in preventing excessive reverse rotation, and helps in resynchronising (or starting) with a moving spindle.

The duration of the watchdog-triggered commutation is determined by:

$$t_{WD} = V_{TH} \times C_{WD} / I_{CWD}$$

where I_{CWD} = normal charge current.

Speed control. The actual speed of the motor is measured by either internally sensing the back-EMFs or by an external scheme via the SECTOR DATA terminal. A TACH signal is produced from these signals, which is then compared against the desired speed, which is programmed into a 14-bit counter (see diagram and waveforms below - assumes internal scheme used). The resulting error signal, ERROR, is then used to charge or discharge the FILTER terminal capacitor depending on whether the motor is running too slow or too fast. The FILTER terminal voltage is used to linearly drive the low-side MOSFETs to match the desired speed.

Each back-EMF signal detected causes the state of the FCOM signal to change. The number of FCOM transitions per mechanical revolution is equal to the number of poles times 3. For example, with a 4-pole motor (as shown on next page), the number of FCOM transitions will equal 12 per mechanical revolution. The number of poles are programmed via serial port bits D20 and D21. There are six electrical states per electrical revolution, therefore, for this example, there are 12 commutations or two electrical revolutions per mechanical revolution.

The TACH signal changes state once per mechanical revolution and as well as providing information on the actual motor speed is also used to trigger the REF counter which contains the information on the desired motor speed. Alternatively an external TACH signal can be used, an explanation of which is presented in the Sector Mode Section.

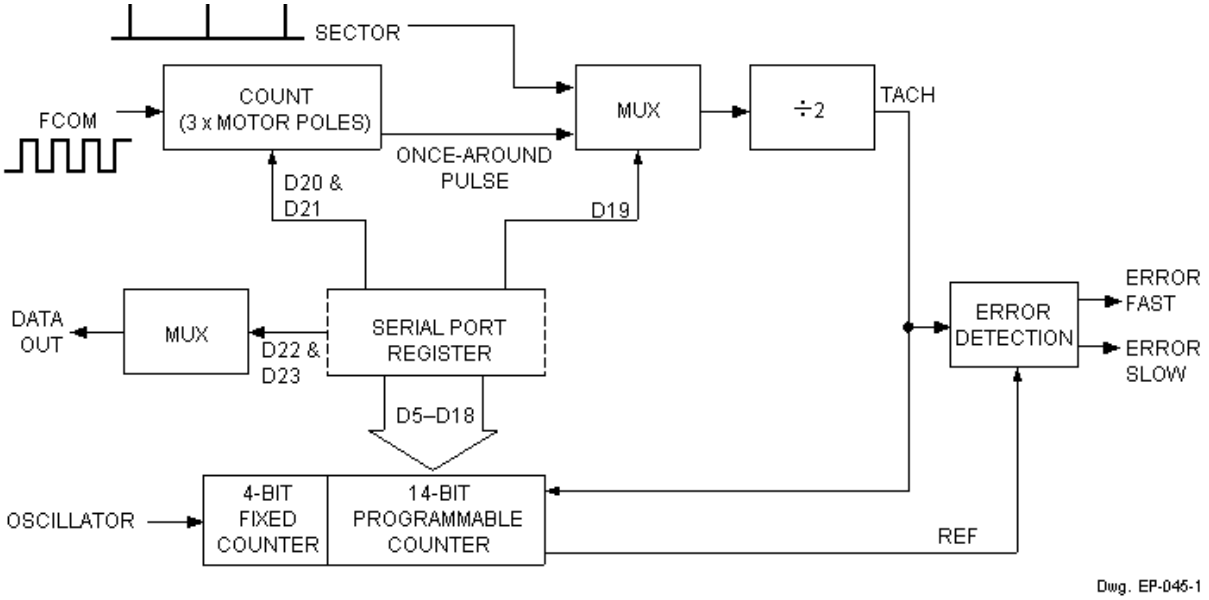
The duration of REF is set by programming the counter to count the desired number of OSCILLATOR cycles, according to the following:

$$\text{total count} = 60 \times f_{OSC} / \text{desired motor speed (rpm)}$$

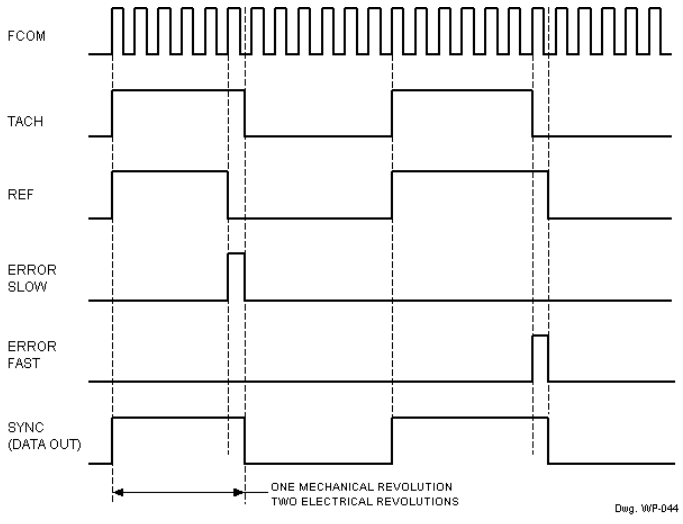
where the total count (number of oscillator cycles) is equal to the sum of the count numbers selected through bits D5 to D18 in the serial port and f_{OSC} corresponds to the OSCILLATOR frequency.

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Functional Description (cont'd)



Speed error detection



Speed error signals

A speed error signal is created by integrating the differences between the TACH and REF signal. If the TACH signal goes low before the REF signal then an ERROR FAST is produced and if the TACH signal goes low after the REF signal then an ERROR SLOW is produced. The error signal generated enables the appropriate current source (see diagram next page) to either charge or discharge the filter components on the FILTER terminal.

The FILTER voltage is then used to provide linear current control in the windings via the transconductance stage (see diagram next page). The output current is sensed through an internal sense resistor, R_S. The voltage across the sense resistor is compared to the lowest of either one-tenth of the voltage at the FILTER terminal, minus the filter threshold voltage, or to the maximum current limit reference.

Alternatively, external control of the FILTER terminal can be introduced by disabling the frequency-lock loop circuitry (D24 = 1).

The transconductance function is defined as:

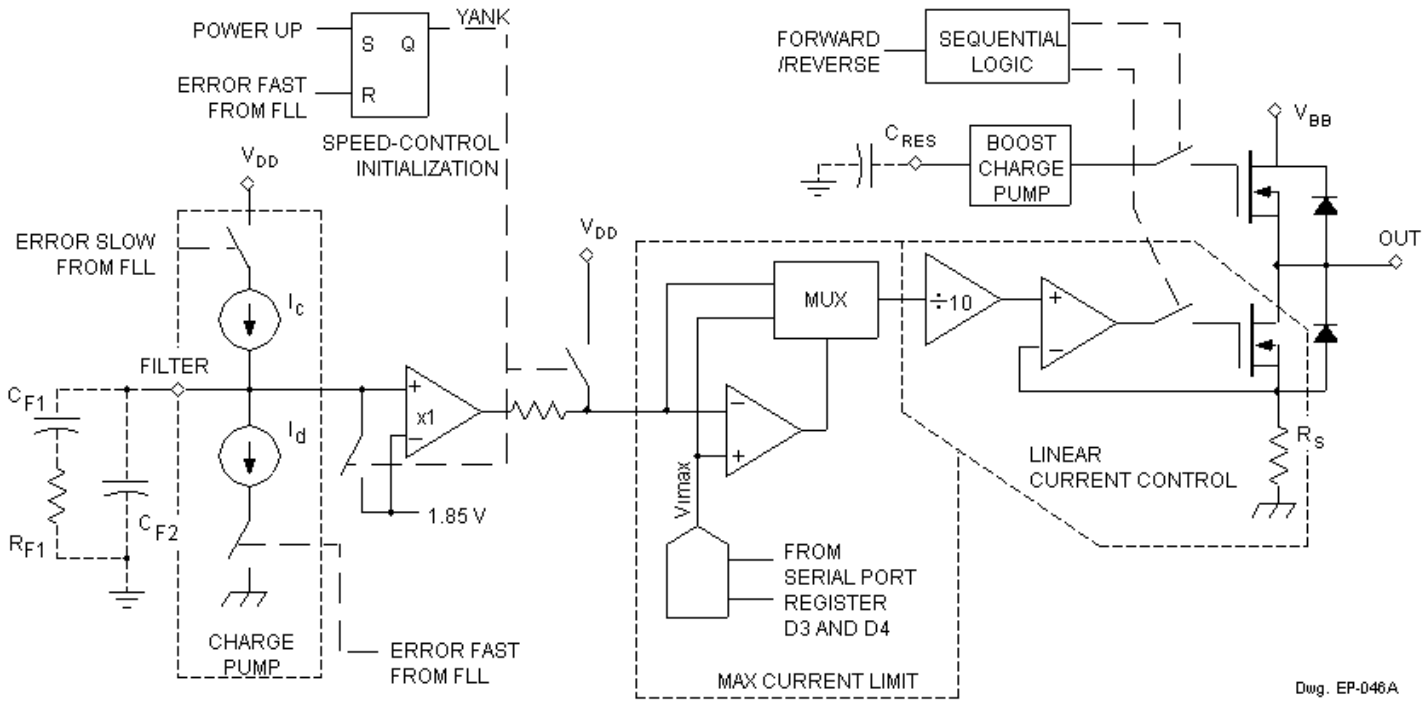
$$I_{OUT} = (V_{FILTER} - V_{FILTERTH}) / (10 \times R_S \times G)$$

where R_S is nominally 200 mΩ,
$V_{FILTERTH}$ is approximately 1.85 V,
G = 1, when D28 = 0 and gain = 500 mA/V or
G = 2, when D28 = 1 and gain = 250 mA/V.

The closed loop control response of the overall system is shaped via the filter components that are introduced at the FILTER terminal.

Clamping the current to a level defined by the serial port (D3 & D4) provides output current limit protection. This feature is particularly useful where high transient currents are experienced, e.g., during start-up. Once normal running conditions are reached, the current limit can be appropriately reduced. Note that the current limit is scaled according to the g_m value selected.

Functional Description (cont'd)



Speed and current control

Sector mode. An external tachometer signal, such as sector or index pulses, can be used to create the TACH signal, rather than the internally generated once-around scheme. The external signal is applied to the SECTOR DATA terminal and the serial port bit (D19 = 1) must be programmed to enable this feature.

In applications where both internal and external TACH signals are used, it is important to only switch between modes when the SYNC signal on DATA OUT is low. This ensures the speed control information that is being processed during the transition, is not corrupted. SYNC is accessed through the DATA OUT multiplexer, which is controlled by D22 & D23.

DATA OUT. The DATA OUT terminal is the output of a 2-bit input multiplexer controlled by D22 & D23 of the serial port. Data available are TACH signal (internally or externally generated), SYNC signal, FCOM signal, and thermal shutdown (LOW = A8904 operating within thermal limits, HIGH = thermal shutdown has occurred).

Speed loop initialization (YANK). To ensure rapid transition from start-up to the normal operating condition, the FILTER terminal is pulled up to the filter threshold voltage, $V_{FILTERTH}$, by the internal YANK command and the initial output current will be set to the maximum selected current limit. This condition is maintained until the motor reaches the correct speed and the first ERROR FAST signal is produced which removes the YANK and allows linear current control.

The YANK feature is also activated when an external speed control scheme is used (D24 = 1). To ensure the YANK is released at start-up by the internal speed control, it is important to ensure the speed reference is set at a lower speed than what the motor is designed to run at. Note that when the serial port is programmed to run initially, the default condition for the speed is set for the slowest condition so this will guarantee the YANK to be released. It is important when using external speed control that, as a minimum, the number of poles, speed control mode, and speed reference are programmed in the serial port.

Forward/reverse. Directional control is managed through D25 in the serial port.

Serial port. Control features and diagnostic data selection are communicated to the A8904 through the 29-bit serial port. See serial port timing diagrams on page 6. When CHIP SELECT is low, data is written to the serial port on the positive edge of the clock with the MSB (D28) fed in first. At the end of

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Functional Description (cont'd)

the write cycle, the CHIP SELECT goes high, the serial port is disabled and no more data can be transferred. In addition, the data written to the serial port is latched and becomes active.

If a word of less than 29 bits is sent, the unused most significant bits that are not programmed, are reset to zero. There are no compatibility issues when using the A8904 in an existing A8902-A application as the five MSBs are reset to zero, which is the default condition for A8902-A operation. The only consideration when using the A8904 in an A8902-A application is to ensure the minimum CHIP SELECT high time is at least 500 ns.

D0 - Sleep/Run Mode; LOW = Sleep, HIGH = Run. This bit allows the device to be powered down when not in use.

D1 - Step Mode; LOW = Normal Operation, HIGH = Step Only. When in the step-only mode the back-EMF commutation circuitry is disabled and the start-up oscillator commutates the power outputs. This mode is intended for device and system testing.

D2 - Brake; LOW = Run, HIGH = Brake.

D3, D4, and D28 - The output current limit is set by D3 & D4; D28 sets the transconductance gain.

D3	D4	D28	Current limit (typical)	Transconductance gain
0	0	0	1.2 A	500 mA/V
0	1	0	1.0 A	500 mA/V
1	0	0	600 mA	500 mA/V
1	1	0	250 mA	500 mA/V
0	0	1	600 mA	250 mA/V
0	1	1	500 mA	250 mA/V
1	0	1	300 mA	250 mA/V
1	1	1	125 mA	250 mA/V

D5 to D18 - 14-bit word, active low. Programs the count number to produce the corresponding REF signal, which indicates the desired motor speed.

Bit number	Count number
D5	16
D6	32
D7	64
D8	128
D9	256
D10	512
D11	1,024
D12	2,048
D13	4,096
D14	8,192
D15	16,384
D16	32,768
D17	65,536
D18	131,072

D19 - Speed control mode; LOW = internal, once-around speed signal, HIGH = external sector data.

D20 and D21 - Programs the number of motor poles for the once-around FCOM counter.

D20	D21	Motor poles
0	0	8
0	1	4
1	0	16
1	1	12

D22 and D23 - Controls the multiplexer for DATA OUT. See DATA OUT Section for status definitions.

D22	D23	DATA OUT
0	0	TACH (once around or sector) signal
0	1	Thermal shutdown
1	0	SYNC signal
1	1	FCOM signal

D24 - Speed Reference. LOW = Internal, using back-EMF technique, HIGH = External (internal control disabled).

D25 - Direction. LOW = Forward, HIGH = Reverse.

D26 and D27 - Programs the charging current for the watchdog capacitor. This function is used for adjusting the blanking duration and also the watchdog commutation period.

D26	D27	Watchdog charge current (typical)
0	0	-10 µA
0	1	-20 µA
1	0	-30 µA
1	1	-40 µA

Functional Description (cont'd)

D28 - Programs the transconductance gain. LOW = 500 mA/V, HIGH = 250 mA/V.

Reset. When the RESET terminal is pulled low, all the serial port bits are reset to LOW and the part operates in sleep mode.

Undervoltage lockout, V_{DD}. When an undervoltage condition occurs, all the serial port bits are reset to LOW and the part operates in sleep mode.

Charge pump. The charge pump is required to provide a voltage rail above the load supply for driving the high-side DMOS gates. In addition the charge pump supply capacitor, C_{RES}, also powers the brake control circuit during power-down conditions. C_{RES} should be 220 nF.

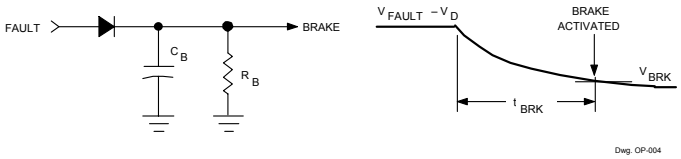
Braking. A dynamic braking feature of the A8904 shorts the three motor windings to ground. This is accomplished by turning the three source drivers OFF and the three sink drivers ON. Activation of the brake can be implemented through the BRAKE input or through the D2 bit in the serial port.

During braking, the motor is effectively acting as three sine-wave voltage generators, 120° out of phase, where the voltage developed by each of the windings is proportional to the motor speed and constant. The current through any sink driver is simply the generated voltage divided by the center tap to OUT resistance plus the sink driver resistance. As the motor tends to slow during the braking process, both the generated voltage and the corresponding current decreases.

When selecting a motor to use where braking will be applied, it is important to characterize the application to ensure that when braking is applied, the peak current in the sink drivers does not exceed 3A and the period from the peak current to the maximum current limit of the drivers does not exceed 800 ms. Another consideration is the thermals of the solution, where repeated spin-up followed by brake cycles could cause excessive junction temperatures.

The supply voltage for the brake circuit is derived from the charge pump supply capacitor, C_{RES}. With C_{RES} chosen to be 220 nF, the brake circuit will function for at least 100 ms after a power failure.

In certain applications such as disk drives, it is desirable to include a brake delay to allow sensitive circuitry such as the disk head to retract before activating the spindle motor brake. The brake delay can be simply implemented by using an external RC and diode to control the brake terminal.



The brake delay can be set using the equation:

$$t_{BRK} = -R_B C_B \times \ln (V_{BRK} / [V_{FAULT} - V_D]).$$

Once the brake is activated, the three sink drivers will remain active until the supply rails fall below the operating range. It is recommended that the part is reset before restarting.

Centertap. It is recommended that the centertap connection of the motor be connected to the CENTERTAP terminal. If the centertap of the motor is not connected to the CENTERTAP terminal, the A8904 internally emulates the centertap voltage of the motor through a series of 10 kΩ resistors connected between each output and CENTERTAP. This technique does not provide ideal commutation points.

External component selection. All capacitors should be rated to at least 25 V and the dielectric should be X7R, apart from the start-up capacitor C_{ST}, which can be Z5U dielectric or equivalent and the input capacitor C_{filter}, which should be an electrolytic type of value greater than 100 µF, 35 V, I_{ripple} > 100 mA. If the solution experiences ambient temperatures of greater than 70°C then C_{filter} should be rated for 105°C.

All resistors are at least 1/8 W and have a tolerance of ±5%.

In noise-sensitive systems where electromagnetic interference is an issue, or to stabilize the current waveforms with certain motors, it may be necessary to add RC snubbers across the motor windings as shown in the application circuit on the next page. The A8904 solution should be relatively noise immune from the effects of switching voltage spikes etc. if the correct watchdog capacitor has been selected for optimum blanking and good layout practices are implemented.

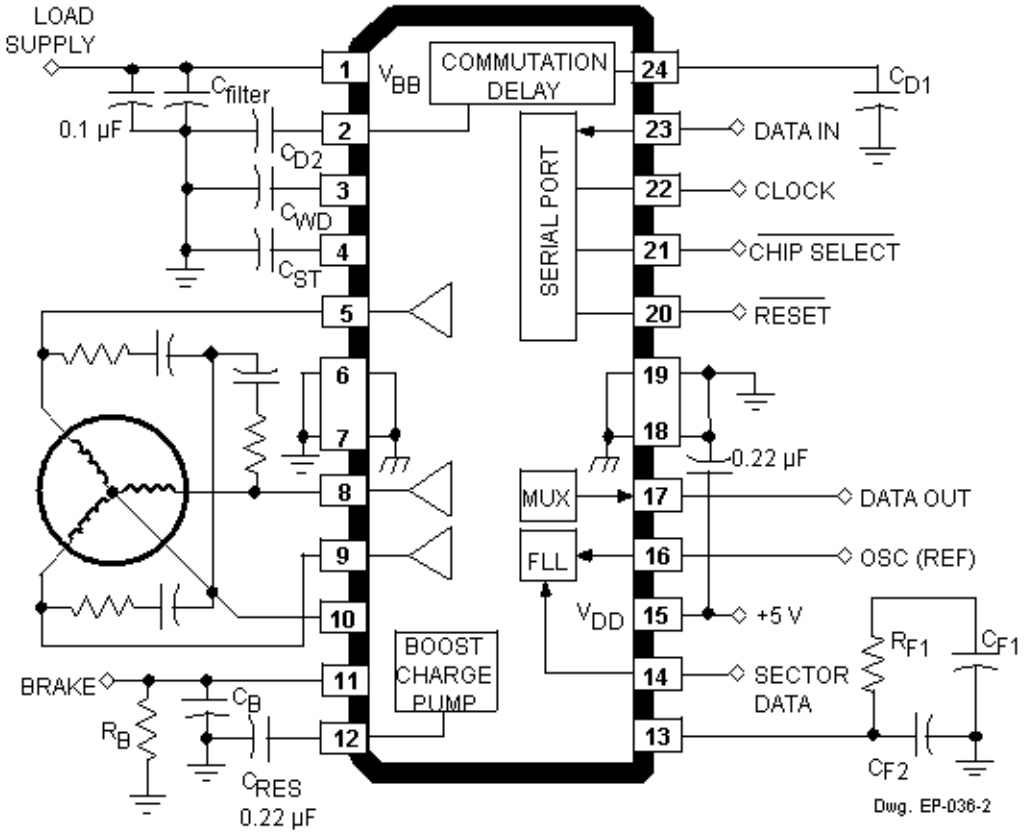
At the range of operating frequencies that the current pulses are drawn out of the load supply, it is the capacitance reactance

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as opposed to the ESR that dominates the overall impedance of the input filter, C_{filter}. Therefore, it is possible to reduce conducted electromagnetic emissions further, by simply increasing the value of $C_{filter.}$ In extremely sensitive systems, it may be necessary to introduce a differential mode inductor in series with the load supply line.

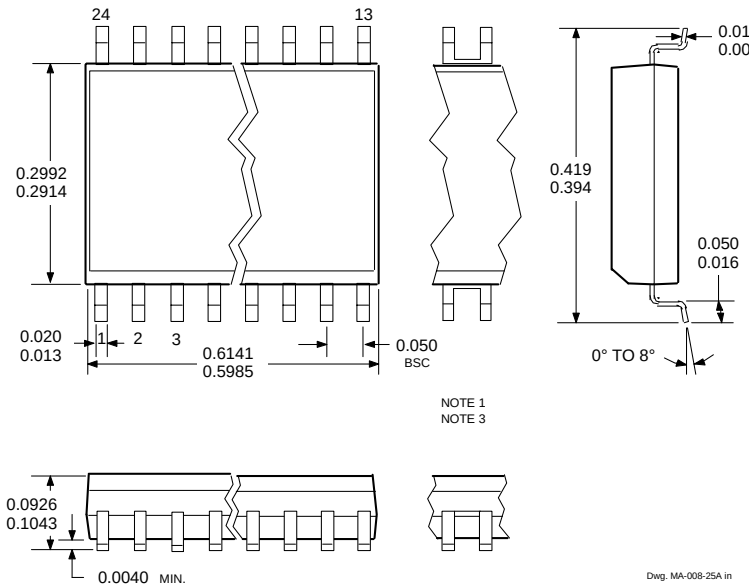
Layout considerations. The TSSOP part (A8904SLP) has three separate ground connections, analog, digital, and power that must be connected together externally. A ground plane should be used to provide heat sinking for the power switches and the reduction of potential noise pick-up through inductive loops and radiated emissions. The ground plane should cover the area beneath the A8904 and extend beyond the outline to form a plane around all the external components. The exposed thermal pad of the TSSOP part should be connected to the ground plane.

Filter components, especially C_{filter}, timing, and delay capacitors should be positioned as close as possible to the device terminals. It is also imperative that the traces to the serial port and oscillator are as short and as wide as possible to reduce stray inductance and prevent potential data corruption. In addition, these traces should be positioned well away from any noisy signals.

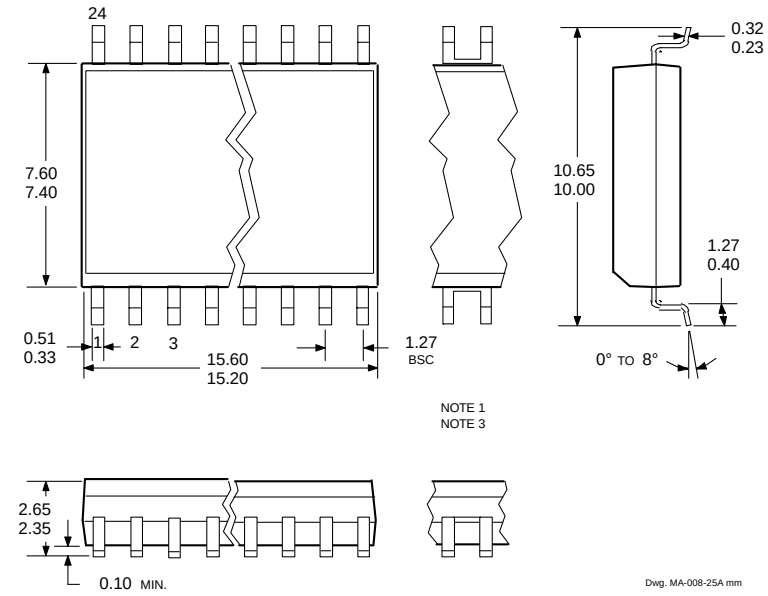


Typical application
(A8904SLB)

A8904SLB (SOIC)



Dimensions in Inches
(for reference only)

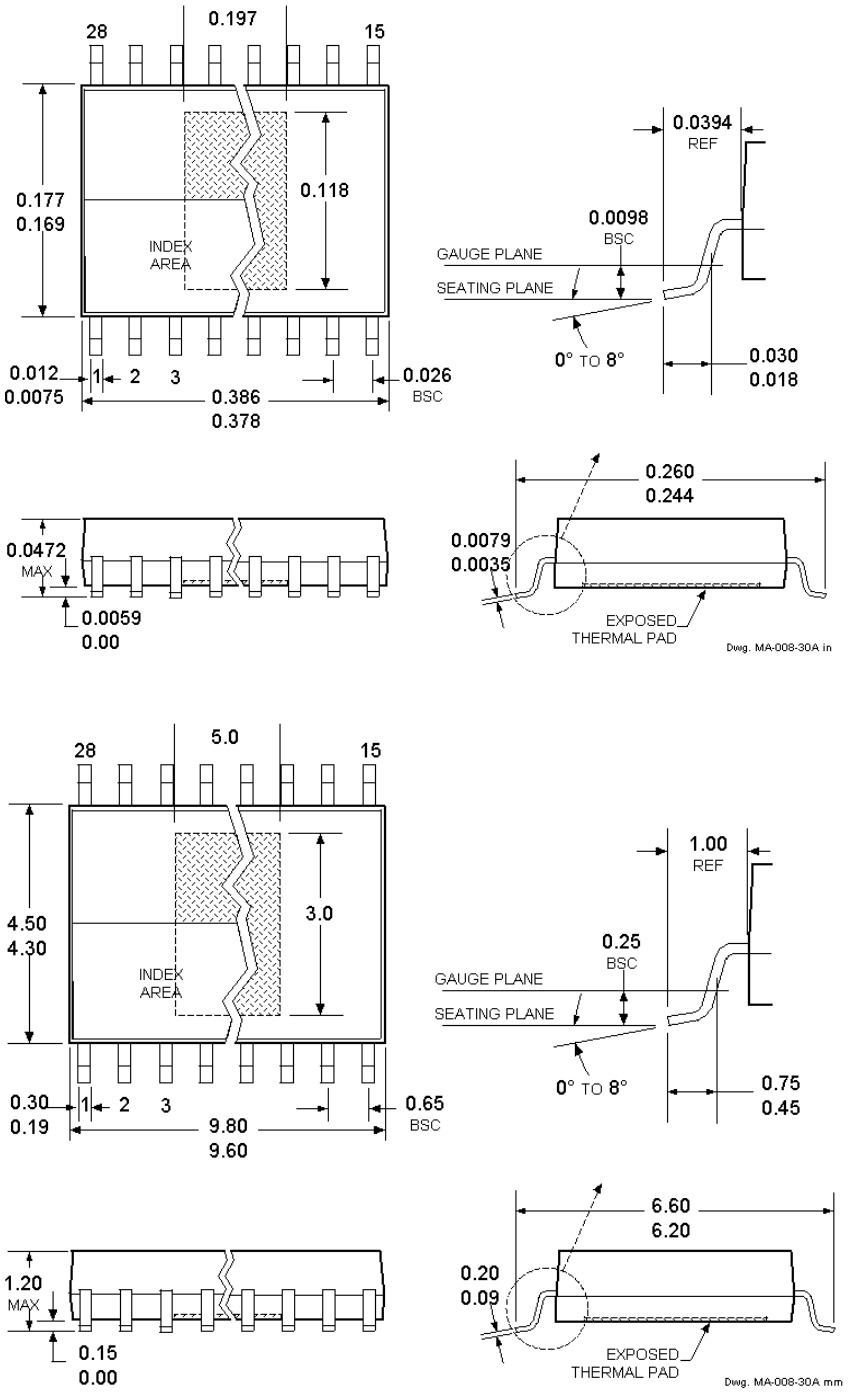


Dimensions in Millimeters
(controlling dimensions)

NOTES:
1. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

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A8904SLP (TSSOP)



Dimensions in Inches
(for reference only)

Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 49 devices or add "TR" to part number for tape and reel.

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