

Quad 18V Pin Electronics Driver/Window Comparator

The ISL55100B is a Quad pin driver and window comparator fabricated in a wide voltage CMOS process. It is designed specifically for Test During Burn-In (TDBI) applications, where cost, functional density, and power are all at a premium.

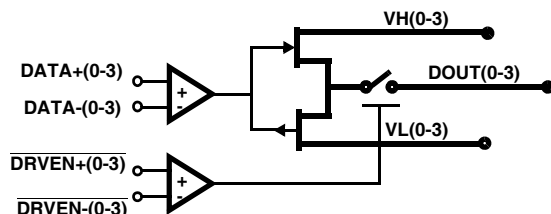
This IC incorporates four channels of programmable drivers and window comparators into a small 72 Ld QFN package. Each channel has independent driver levels, data, and high impedance control. Each receiver has dual comparators which provide high and low threshold levels.

The ISL55100B uses differential mode digital inputs, and can therefore mate directly with LVDS or CML outputs. Single-ended logic families are handled by connecting one of the digital input pins to an appropriate threshold voltage (e.g., 1.4V for TTL compatibility). The comparator outputs are single-ended, and the output levels are user defined to mate directly with any digital technology.

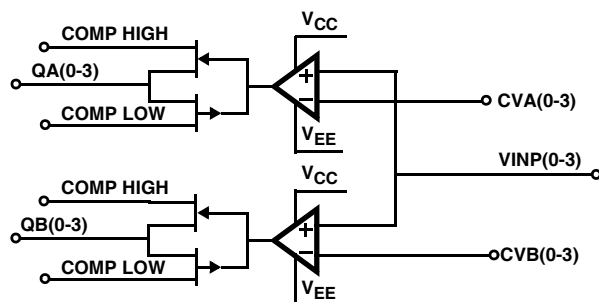
The 18V driver output and receiver input ranges allow this device to interface directly with TTL, ECL, CMOS (3V, 5V, and 7V), LVCMOS, and custom level circuitry, as well as the high voltage (Super Voltage) level required for many special test modes for Flash Devices.

Functional Block Diagram

QUAD - WIDE RANGE, LOW ROUT, TRI-STATEABLE - DRIVERS



QUAD - DUAL LEVEL COMPARATOR - RECEIVERS



Features

- Low Driver Output Resistance
 - R_{OUT} Typical: 9.0Ω
- 18V I/O Range
- 50MHz Operation
- 4 Channel Driver/Receiver Pairs with Per Pin Flexibility
- Dual Level - Per Pin - Input Thresholds
- Differential or Single-Ended Digital Inputs
- User Defined Comparator Output Levels
- Low Channel to Channel Timing Skew
- Small Footprint (72 Ld QFN)
- Pb-Free (RoHS Compliant)

Applications

- Burn In ATE
- Wafer Level Flash Memory Test
- LCD Panel Test
- Low Cost ATE
- Instrumentation
- Emulation
- Device Programmers

Ordering Information

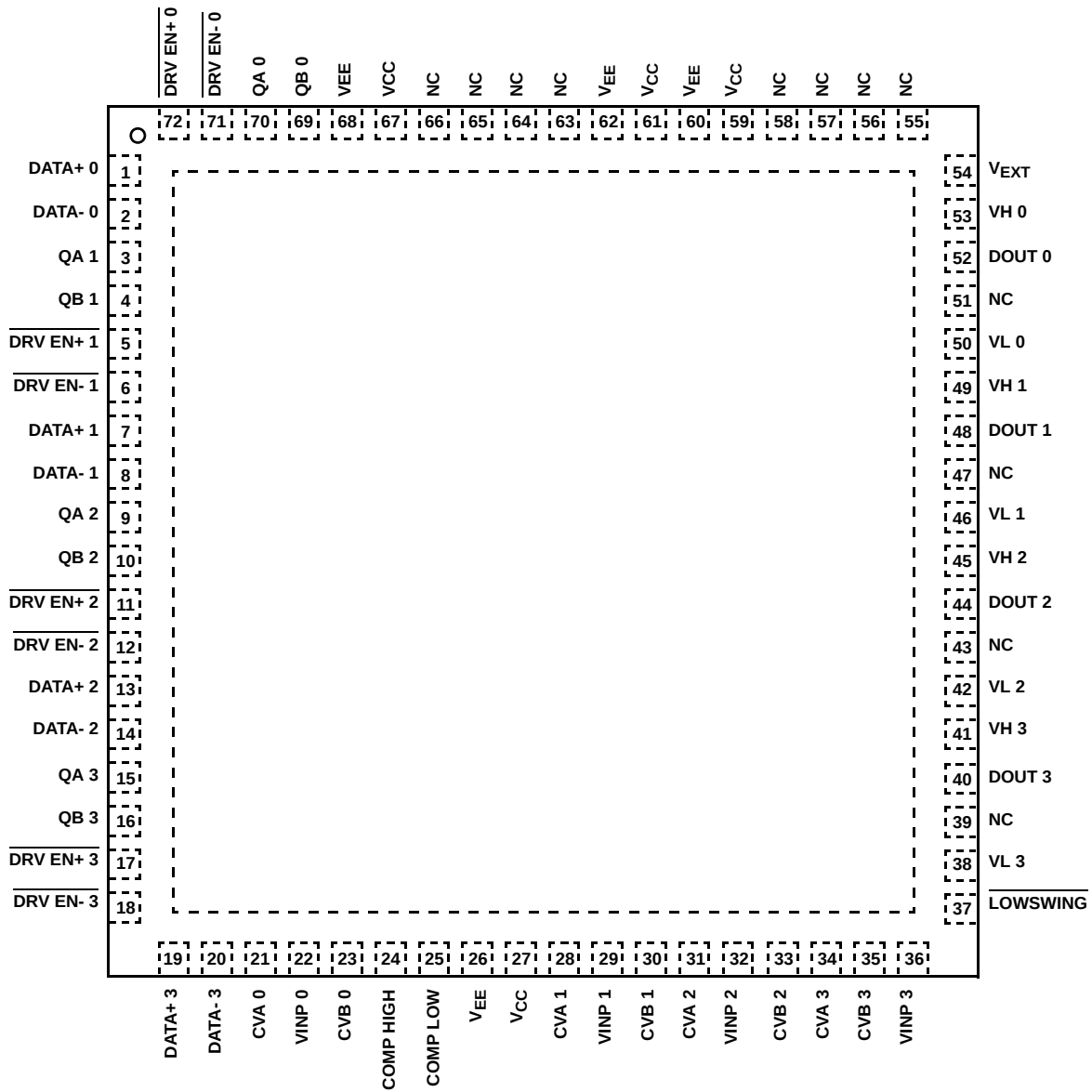
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55100BIRZ*	ISL55100 BIRZ	-40 to +85	72 Ld QFN	L72.10x10

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL55100B
(72 LD QFN)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
DATA+(0:3)	Positive differential digital input that determines the driver output state when it is enabled.
DATA-(0:3)	Negative differential digital input that determines the driver output state when it is enabled.
$\overline{\text{DRV EN}}+(0:3)$	Positive differential digital input that enables or disables the corresponding driver.
$\overline{\text{DRV EN}}-(0:3)$	Negative differential digital input that enables or disables the corresponding driver.
QA (0:3)	Comparator digital outputs. QA(X) is high when VINP(X) exceeds CVA(X).
QB (0:3)	Comparator digital outputs. QB(X) is high when VINP(X) exceeds CVB(X).
DOUT (0:3)	Driver outputs.
VINP (0:3)	Comparator inputs.
VH (0:3)	Unbuffered analog inputs that set each individual driver's "high" voltage level.
VL (0:3)	Unbuffered analog inputs that set each individual driver's "low" voltage level. VL must be a lower voltage than VH.
NC	No internal connection.
CVA (0:3)	Analog inputs that set the threshold for the corresponding Channel A comparators.
CVB (0:3)	Analog inputs that set the threshold for the corresponding Channel B comparators.
COMP HI	Supply voltage, unbuffered input that sets the high output level of all comparators. Must be greater than COMP LO.
COMP LO	Supply voltage, unbuffered input that sets the low output level of all comparators. Must be less than COMP HI.
V _{CC}	Positive power supply (5% tolerance).
V _{EE}	Negative power supply (5% tolerance).
V _{EXT}	External 5.5VDC power supply (5.5VDC to 6.0VDC as referenced to V_{EE} , NOT GND. Recommended V _{EXT} = 5.5V) for internal logic. Connect pin to V _{EE} when not using an external supply.
LOWSWING	Input that selects driver output configurations optimized to yield minimum overshoots for low level swings (VH < V _{EE} +5V), or optimized for large output swings. Connect LOWSWING to V _{EE} to select low swing circuitry, or connect it to V _{CC} to select high swing circuitry.

Truth Tables

DRIVERS		
INPUTS		OUTPUT
DATA	$\overline{\text{DRV EN}}$	DOUT
X	+ > -	Hi - Z
+ > -	+ < -	VH
+ < -	+ < -	VL

X = DON'T CARE

RECEIVERS			
INPUT		OUTPUTS	
VINP		QA	QB
<CVA	<CVB	0	0
<CVA	>CVB	0	1
>CVA	<CVB	1	0
>CVA	>CVB	1	1

Absolute Maximum Ratings

V_{CC} to V_{EE}	-0.5V to 19V
V_{EXT} to V_{EE}	-0.5V to 7V
Input Voltages	
DATA, DRV EN, CVX, VH, VL, VINP, COMPX, LOWSWING	($V_{EE} - 0.5V$) to ($V_{CC} + 0.5V$)
Output Voltages	
DOUT	($V_{EE} - 0.5V$) to ($V_{CC} + 0.5V$)
QX	(COMP LOW - 0.5V) to (COMP HIGH + 0.5V)

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
72 Ld QFN Package.	23	2.0
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range.	-65°C to +150°C	
Pb-Free Reflow Profile.	see link below	
http://www.intersil.com/pbfree/Pb-FreeReflow.asp		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 and Tech Brief TB389 for details. Device temperature is closely tied to data-rates, driver loads and overall pin activity. Review "Power Dissipation Considerations" on page 9 for more information.
2. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Device Power-($V_{EXT} = V_{EE}$) V_{EXT} not used	$V_{CC} - V_{EE}$	12 (Note 6)	15	18	V
Device Power-($V_{EXT} = V_{EE} + 5.5V$)	$V_{CC} - V_{EE}$	9 (Note 6)	15	18	V
V_{EXT} Optional External Logic Power	$V_{EXT} - V_{EE}$	5.5 (Note 6)	5.75	6.0	V
Driver Output High Rail	V_H	$V_{EE} + 1$	-	$V_{CC} - 0.5$	V
Driver Output Low Rail	V_L	$V_{EE} + 0.5$	-	$V_{EE} + 6$	V
Comparator Output High Rail	COMP-High	$V_{EE} + 1$	-	$V_{CC} - 0.5$	V
Comparator Output Low Rail	COMP-Low	$V_{EE} + 0.5$	-	$V_{EE} + 6$	V
Ambient Temperature	T_A	-40	-	+85	°C
Junction Temperature	T_J	-	-	+150	°C

Electrical Specifications Test Conditions: $V_{CC} = 12V$, $V_{EE} = -3V$, $V_H = 6V$, $V_L = 0V$, Comp-High = 5V, Comp Low = 0V, $V_{EXT} = V_{EE}$ and LOWSWING = V_{CC} , +25°C; Unless Otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER DC CHARACTERISTICS						
ISL55100B Output Resistance	R_{OUTD}	$I_O = \pm 125mA$, data not toggling	6	9	14	Ω
ISL55100B DC Output Current	$I_{out D}$	Per Individual driver	± 125	-	-	mA
ISL55100B AC Output Current (Note 3)	I_{OUTDAC}	Per Individual driver	-	600	-	mA
ISL55100A Minimum Output Swing	V_{OMIN}	$V_H = 200mV$, $V_L = 0V$	185	-	-	mV
Disabled HIZ Leakage Current	HIZ	$V_{OUT} = V_{CC}$ with $V_H = V_L + V_{EE}$ or $V_{OUT} = V_{EE}$ with $V_H = V_L = V_{CC}$	-1	0	1	μA
DRIVER TIMING CHARACTERISTICS						
Data± to DOUT Propagation Delay	t_{PD}	Lowswing Disabled (Note 5)	5	12	16	ns
		Lowswing Enabled (Note 5)	6	13	17	ns
Driver Timing Skew, All Edges (Note 3)			-	<1	-	ns
Disable (HIZ) Time	t_{DIS}	DVREN± Transition from Enable to Disable	15	18	26	ns
Enable Time	t_{EN}	DVREN± Transition from Disable to Enable: Lowswing Disabled (Note 5)	13	15	23	ns
		DVREN± Transition from Disable to Enable: Lowswing Enabled (Note 5)	13	18	23	ns

ISL55100B

Electrical Specifications Test Conditions: $V_{CC} = 12V$, $V_{EE} = -3V$, $V_H = 6V$, $V_L = 0V$, Comp-High = 5V, Comp Low = 0V, $V_{EXT} = V_{EE}$ and LOWSWING = V_{CC} , +25°C; Unless Otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
ISL55100B Rise/Fall Times (Note 3)	t_R, t_F	100pF Load	DV = 0.4V (20% to 80%)	-	2.5	-	ns
			DV = 1V (20% to 80%)	-	2.5	-	ns
			DV = 5V (10% to 90%)	-	3.0	-	ns
			DV = 10V (10% to 90%)	-	3.5	-	ns
			DV = 14V (10% to 90%)	-	3.5	-	ns
ISL55100B Rise/Fall Times (Note 3)	t_R, t_F	1000pF Load	DV = 1V (20% to 80%)	-	9	-	ns
			DV = 5V (10% to 90%)	-	11	-	ns
			DV = 10V (10% to 90%)	-	14	-	ns
ISL55100B Maximum Toggle Frequency	FMAXD	No Load, 50% Symmetry		50	65	-	MHz
ISL55100B Min Driver Pulse Width	t_{WIDD}	Standard Load, 1k/100pF (Note 4)		-	7.7	-	ns
ISL55100B Overshoot <u>Lowswing</u> Mode (Note 3)	OS	<u>Lowswing</u> Enabled, (VH-VL<2V)		-	20mV+ 10% of output swing	-	%+V
RECEIVER DC CHARACTERISTICS							
Input Offset Voltage	V _{OS}	CVA = CVB = 1.5V		-200	-	200	mV
Input Bias Current	I _{BIAS}	V _{INP} - CV _(A/B) = ±5V		-	10	30	nA
Output Resistance	RoutR			18	25	35	Ω
RECEIVER TIMING CHARACTERISTICS							
Propagation Delay	t _{PP}			7	12	18	ns
Maximum Operating Frequency	F _{MAXR}	Under No Load, PWOUT Symmetry 50%		50	65	-	MHz
Min Pulse Width	t _{WIDR}			-	7.7	-	ns
Rcvr Channel-to-Channel Skew (Note 3)				-	<1	-	ns
DIGITAL INPUTS							
Differential Input High Voltage	V _{DIFFH}	V _{DIG+} - V _{DIG-}		200	-	-	mV
Differential Input Low Voltage	V _{DIFFL}	V _{DIG+} - V _{DIG-}		-	-	-200	mV
Input Current	I _{IN}	V _{IN} = V _{CC} or V _{EE}		-50	0	50	nA
Common Mode Input Voltage Range	V _{CM}	V _{DIFFL} not greater than V _{DIFFH} - 0.2V				V _{CC} - 5V	V
		V _{DIFFH} not less than V _{DIFFL} + 0.2V		V _{EE} + 0.2V	-	-	V
POWER SUPPLIES, DRIVER/RECEIVER STATIC CONDITIONS V _{EXT} = V _{EE} , EXTERNAL LOGIC POWER OPTION NOT USED. (Note 7)							
Positive Supply Current	I _{CC}	V _{CC} = V _H = 12V, V _{EE} = V _L = -3V, V _{EXT} = V _{EE} , Outputs Unloaded		-	65	85	mA
Negative Supply Current	I _{EE}	V _{CC} = V _H = 12V, V _{EE} = V _L = -3V, V _{EXT} = V _{EE} , Outputs Unloaded		-85	-65	-	mA
V _{EXT} Supply Current	I _{EXT}	V _{CC} = V _H = 12, V _{EE} = V _L = -3V, V _{EXT} = V _{EE} , Outputs Unloaded		-	<1	-	mA

Electrical Specifications Test Conditions: $V_{CC} = 12V$, $V_{EE} = -3V$, $V_H = 6V$, $V_L = 0V$, Comp-High = 5V, Comp Low = 0V, $V_{EXT} = V_{EE}$ and $LOWSWING = V_{CC}$, +25°C; Unless Otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES, DRIVER/RECEIVER STATIC CONDITIONS $V_{EXT} = V_{EE} + 5.5V$, EXTERNAL LOGIC POWER OPTION USED. (Note 8)						
Positive Supply Current	I_{CC}	$V_{CC} = V_H = 12V$, $V_{EE} = V_L = -3V$, $V_{EXT} = V_{EE} + 5.5V$, Outputs Unloaded	-	35	50	mA
Negative Supply Current	I_{EE}	$V_{CC} = V_H = 12V$, $V_{EE} = V_L = -3V$, $V_{EXT} = V_{EE} + 5.5V$, Outputs Unloaded	-50	-35	-	mA
V_{EXT} Supply Current	I_{EXT}	$V_{CC} = V_H = 12V$, $V_{EE} = V_L = -3V$, $V_{EXT} = V_{EE} + 5.5V$, Outputs Unloaded	-	25	40	mA

NOTES:

- Lab characterization, room temp, Timing Parameters Matched Stimulus/Loads, Channel-to-Channel Skew < 500ps, 1ns Max by design.
- Measured across 100pF/1k lump sum load + 15pF PCB/Scope Probe. Cap and Resistor Surface Mount/Stacked ~0.5" from Pin.
- To Enable **LOWSWING**, connect **LOWSWING** to V_{EE} and keep $V_H < V_{EE} + 5$. To disable **LOWSWING**, connect it to V_{CC} .
- When V_{EXT} is connected to V_{EE} (External Device Power not used) then the Minimum $V_{CC} - V_{EE}$ is 12V. When V_{EXT} is connected to an external 5.5V supply, then the minimum $V_{CC} - V_{EE}$ voltage is 9V. Recommended $V_{EXT} = 5.5V$ as referenced to V_{EE} .
- I_{CC} and I_{EE} values are based on static conditions and will increase with pattern rates. I_{CC} and I_{EE} reach 400mA to 500mA at maximum data rates (provided sufficient device cooling is employed). These currents can be reduced by 1) Reducing the $V_{CC} - V_{EE}$ operating voltage 2) Utilizing the V_{EXT} option.
- When using $V_{EXT} = 5.5V$, current requirements of the V_{EXT} input can approach 100mA at maximum pattern rates.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

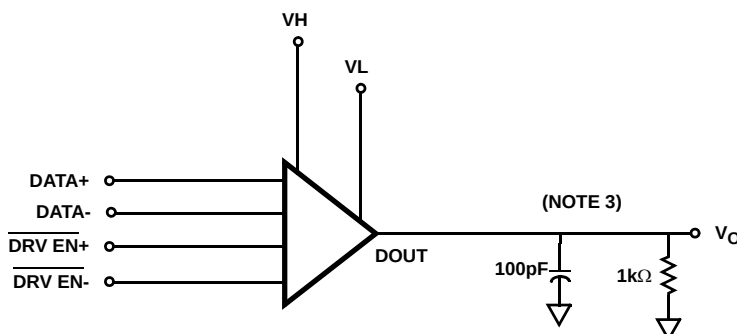


FIGURE 1. DRIVER SWITCHING TEST CIRCUIT

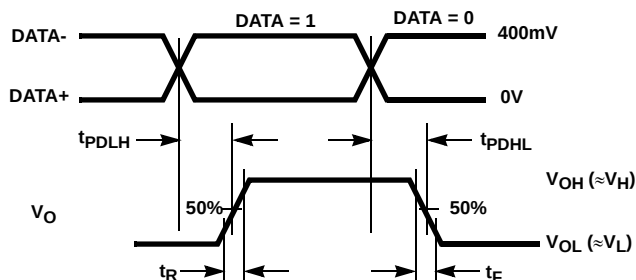


FIGURE 2. DRIVER PROPAGATION DELAY AND TRANSITION TIME MEASUREMENT POINTS

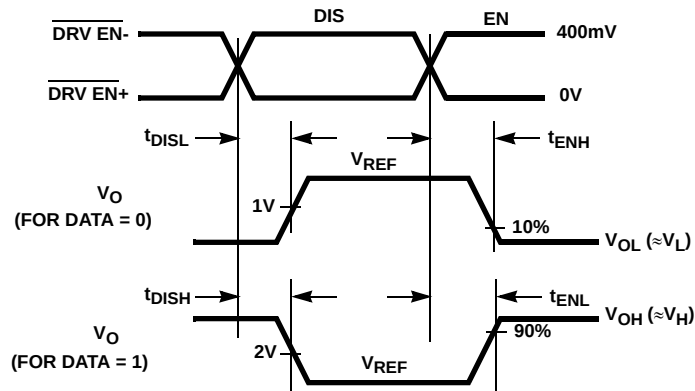
Test Circuits and Waveforms (Continued)

FIGURE 3. DRIVER ENABLE AND DISABLE TIME MEASUREMENT POINTS

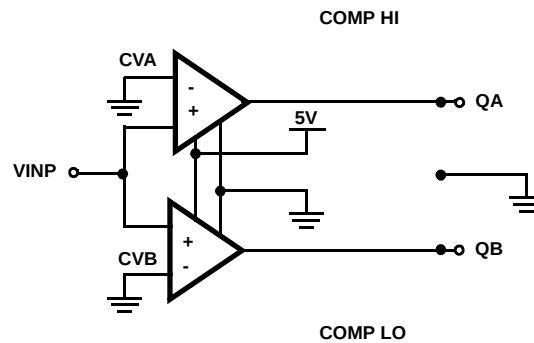


FIGURE 4. RECEIVER SWITCHING TEST CIRCUIT

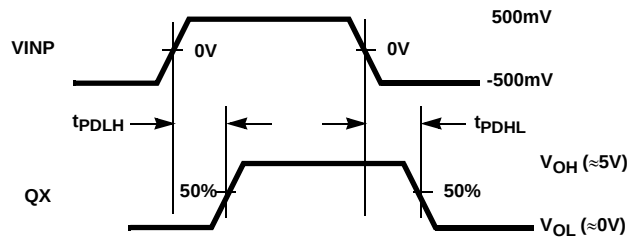


FIGURE 5. RECEIVER PROPAGATION DELAY MEASUREMENT POINTS

Application Information

The ISL55100B provides Quad pin drivers and Quad dual level comparator receivers in a small footprint. The four channels may be used as bidirectional or split channels. Drivers have per channel level, data, and high impedance controls, while comparators have per channel high and low threshold levels.

Receiver Features

The receivers are four independent window comparators that feature high output current capability, and user defined high and low output levels to interface with a wide variety of logic families. Each receiver comprises two comparators and each comparator has an independent threshold level input, making it easy to implement window comparator functions. The CVA and CVB pins set the threshold levels of the A and B

comparators respectively. COMP HIGH and COMP LOW set all the comparator output levels, and COMP HIGH must be more positive than COMP LOW. These two inputs are unbuffered supply pins, so the sources driving these pins must provide adequate current for the expected load. COMP HIGH and COMP LOW typically connect to the power supplies of the logic device driven by the comparator outputs. The truth table for the receivers is given on page 3. Receiver outputs cannot be placed in a HIZ state, and do not incorporate any on-chip short circuit current protection. Momentary short circuits to GND, or any supply voltage, won't cause permanent damage, but care must be taken to avoid longer duration short circuits. If tolerable to the application, current limiting resistors can be inserted in series with the QA(0-3) and QB(0-3) outputs to protect the receiver outputs from damage due to overcurrent conditions.

Driver Features

The drivers are single-ended outputs featuring a wide voltage range, an output stage capable of delivering 125mA while providing a low out resistance and HIZ capability. The driver output can be toggled to drive one of two user defined output levels High (VH) or Low (VL).

Driver waveforms are greatly affected by load characteristics. The ISL55100B actually double bonds the VH(0-3) and VL(0-3) supply pins for each channel. The Driver Output Pins (DOUT(0-3)) are triple bonded. Multiple bond wires help reduce the effects of Inductance between the IC Die (Wafer) and the packaging. Also the QFN style of packaging reduces inductance over other types of packaging.

While the inductance of a bond wire might seem insignificant, it can reduce high-frequency waveform fidelity. So this should be borne in mind when doing PCB layout and DUT interconnect. Lead lengths should be kept as short as possible, maintaining as much decoupling on the drive rails as possible and make sure scope measurements are made properly. Often the inductance of a scope probe ground can be the actual cause of the waveform distortion.

VH and VL (Driver Output Rails)

Sets of VH and VL pins are designated for each Driver. These are unbuffered analog inputs that determine the Drive High (VH) and Drive Low (VL) Voltages that the drivers will deliver. These inputs are double bonded to reduce inductance and decrease AC Impedance.

Each VH and VL should be decoupled with 4.7 μ F and 0.1 μ F capacitors to ground. If all four Driver VH/VLs are bussed, then one 4.7 μ F can be used. Layouts should also accommodate the placement of capacitance "across" VH and VL. So in addition to decoupling the VH/VL pins to ground, they are also decoupled to each other.

Logic Inputs

The ISL55100B uses differential mode digital inputs, and can therefore mate directly with LVDS or CML outputs. Single ended logic families are handled by connecting one of the digital input pins to an appropriate threshold voltage (e.g., 1.4V for TTL compatibility).

LOWSWING Circuit Option

The drivers include switchable circuitry that is optimized for either low (VH-VL < 3V) or high output swings. Configuring the part is accomplished via the LOWSWING pin. Connecting LOWSWING to V_{EE} selects the circuits optimized for low overshoots at low swing operation. Connecting the pin to V_{CC} enables the large signal circuitry (see Figure 6).

With LOWSWING = V_{EE}, the low swing circuitry activates whenever VH < V_{EE} + 5V. Set LOWSWING = V_{EE} only if the output swing (VH-VL) is less than 3V, and better than 10% overshoots are required.

For the best small (low swing) signal performance, the VH/VL common mode voltage [(VH + VL)/2] must be V_{EE} + 1.5V. So if V_{EE} = 0V, and the desired swing is 500mV, set VH = 1.75V, and VL = 1.25V.

Driver and Receiver Overload Protection

The ISL55100B is designed to provide minimum and balanced Driver R_{OUT}. Great care should be taken when making use of the ISL55100B low R_{OUT} drivers as there is no internal protection. There is no short circuit protection built into either the driver or the receiver/comparator outputs. Also there are no junction temperature monitors or thermal shutdown features.

The driver or receiver outputs may be damaged by more than a momentary short circuit directly to any low impedance voltage. Driver Protection can be obtained with a 50 Ω Series Termination Resistor that is properly rated.

External Logic Supply Option (V_{EXT})

Connection of the V_{EXT} Pin to a 5.5V DC Source (referenced to V_{EE}) will reduce the V_{CC}-V_{EE} current drain. Current drain is directly proportional to Data Rate. This option will help with Power Supply/Dissipation should heat distribution become an issue.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{EE} pin is connected to ground, one 0.1 μ F ceramic capacitor should be placed from the V_{CC} pin to ground. A 4.7 μ F tantalum capacitor should then be connected from the V_{CC} pin to

ground. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Power Dissipation Considerations

Specifying continuous data rates, driver loads and driver level amplitudes are key in determining power supply requirements as well as dissipation/cooling necessities. Driver Output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

Figures 17 and 18 address power consumption relative to frequency of operation. These graphs are based on driving 6.0/0.0V out into a 1k Ω load. Theta J_A for the device package is 23.0, 16.6 and 14.9°C/W based on Airflows of 0, 1 and 2.5 meters per second. The device is mounted per Note 1 under "Thermal Information" on page 4. With the high speed data rate capability of the ISL55100B, it is possible to exceed the +150°C "absolute maximum junction temperature" as operating conditions and frequencies increase. Therefore, it is important to calculate the maximum junction temperature for the application to determine if operating conditions need to be modified for the device to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (EQ. 1)$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on number of channels changing state, frequency of operation. The extent of continuous active pattern generation/reception will greatly effect dissipation requirements.

The power dissipation curves (Figure 17), provide a way to see if the device will overheat. The maximum safe power temperature vs operating frequency can be found graphically in Figure 18. This graph is based on the package type Theta J_A ratings and actual current/wattage requirements of the ISL55100B when driving a 1k load with a 6V High Level and a 0V Low Rail. The temperatures are indicated as calculated junction temperature over the ambient temperature of the user's system. Plots indicate temperature change as operating frequency increases (the graph assumes continuous operation). The user should evaluate various heat sink/cooling options in order to control

the ambient temperature part of the equation. This is especially true if the users applications require continuous, high speed operation.

The reader is cautioned against assuming the same level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted. Great care must be taken to ensure Die Temperature does not exceed the +150°C Absolute Maximum Thermal Limits.

Important Note: The ISL55100B package metal plane is used for heat sinking of the device. It is electrically connected to the negative supply potential (V_{EE}). If V_{EE} is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad (V_{EE}) must be isolated from other power planes.

Power Supply Sequencing

The ISL55100B references every supply with respect to V_{EE}. Therefore apply V_{EE}, then V_{CC} followed by the V_H, V_L busses, then the COMP High and Comp Low followed by the CVA and CVB Supplies. Digital Inputs should be set with a differential bias as soon as possible. In cases where V_{EXT} is being utilized (V_{EXT} = V_{EE} + 5.5V), it should be powered up immediately after V_{CC}. Basically, no pin should be biased above V_{CC} or below V_{EE}.

Data Rates

Please note that the Frequency (MHz) in Figures 17 and 18 contain two transitions within each period. A digital application that requires a new test pattern every 50ns would be running at a 20MHz Data Rate. Figure 19 reveals 100ns period, in 10MHz frequency parlance, results in two 50ns digital patterns.

ESD Protection

Figure 6 is the block diagram depicting the ESD protection networks and the V_{OH} upper FET body diode.

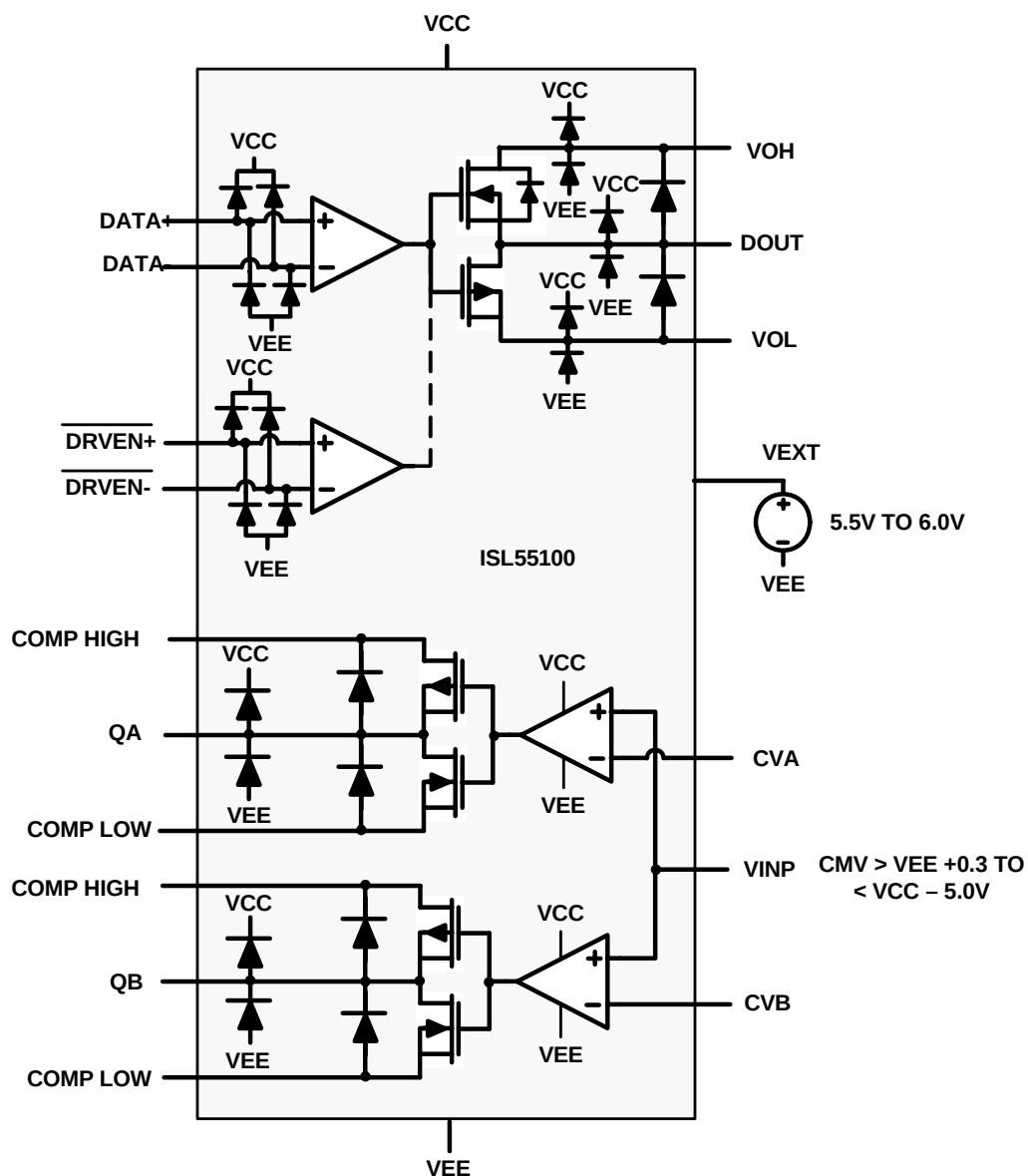


FIGURE 6. ESD STRUCTURE BLOCK DIAGRAM

Typical Performance Curves

Device installed on Intersil ISL55100B Evaluation Board.

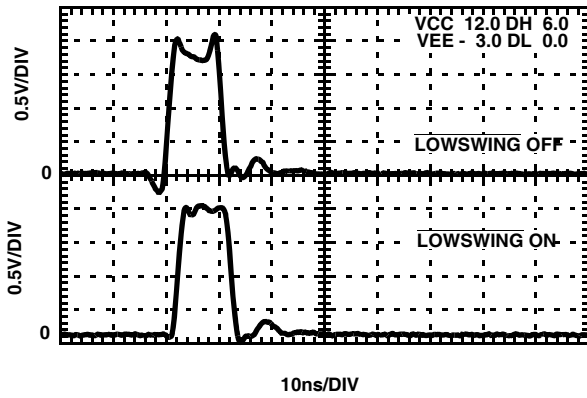


FIGURE 7. LOWSWING EFFECTS ON DRIVER SHAPE AND T_{PD} (100pF-1k LOAD)

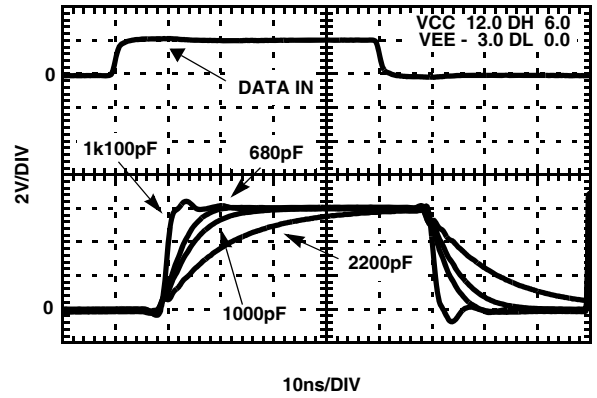


FIGURE 8. DRIVER WAVEFORMS UNDER VARIOUS LOADS

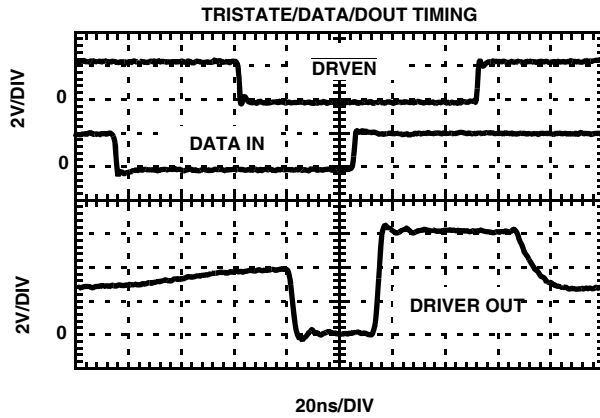


FIGURE 9. DATA/HIZ/DRIVER OUT TIMING

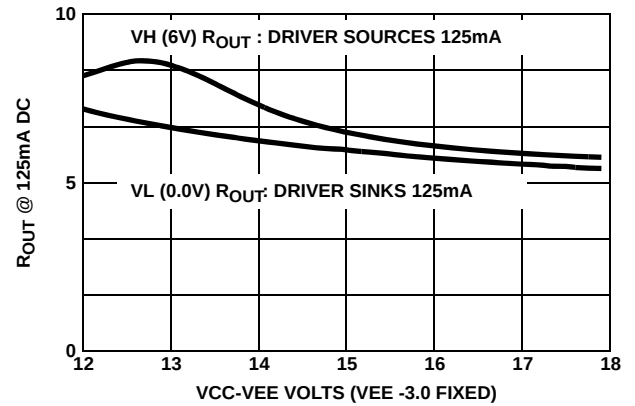


FIGURE 10. R_{OUT} vs DEVICE VOLTAGE

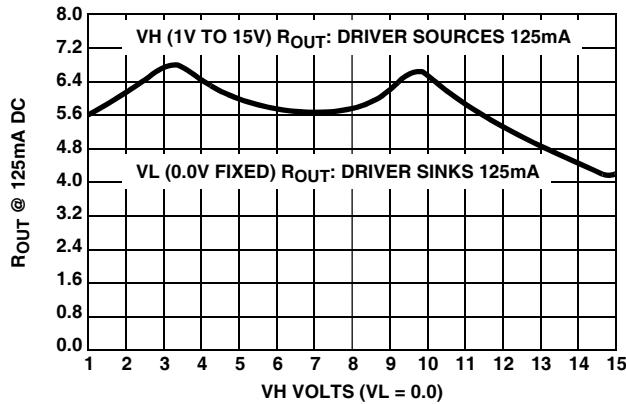


FIGURE 11. R_{OUT} vs VH RAIL

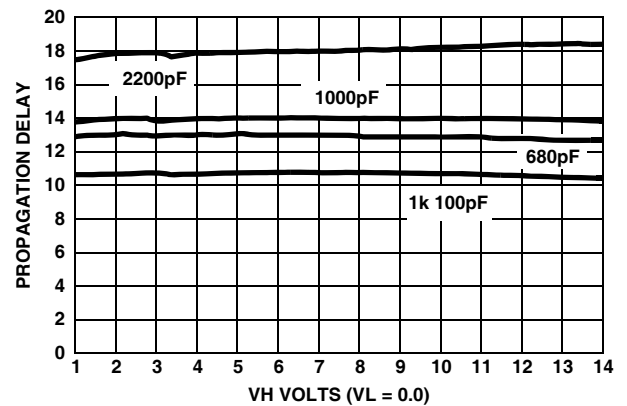


FIGURE 12. PROPAGATION DELAY vs VH RAIL, VARIOUS LOADS

Typical Performance Curves

Device installed on Intersil ISL55100B Evaluation Board. (Continued)

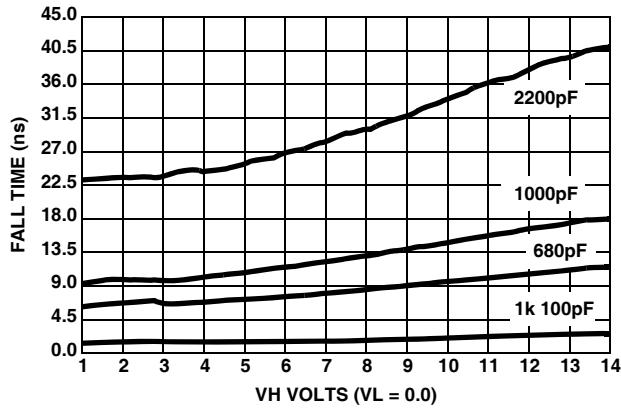


FIGURE 13. DRIVER FALL TIME vs VH RAIL, VARIOUS LOADS

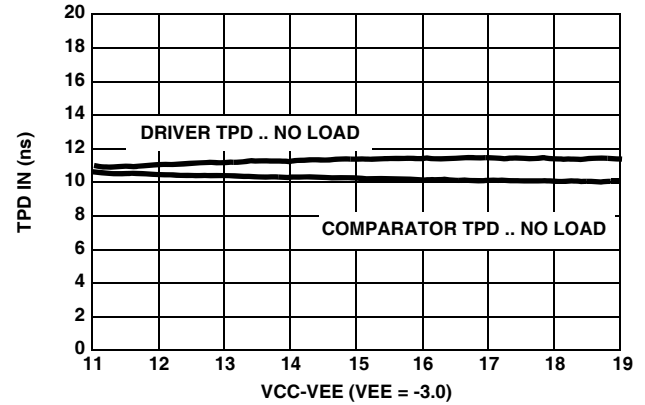
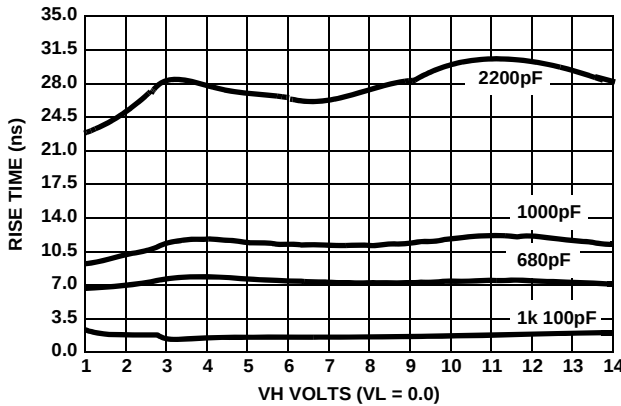
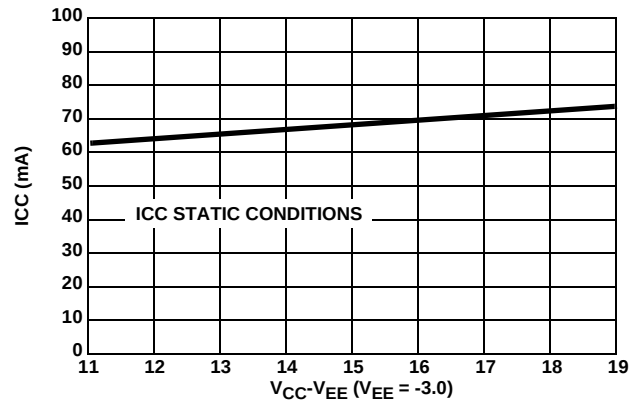
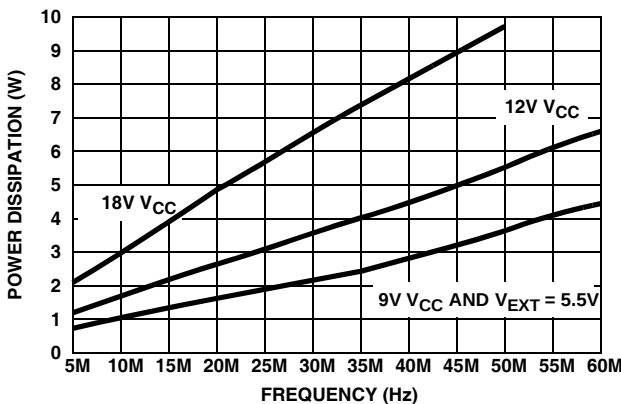
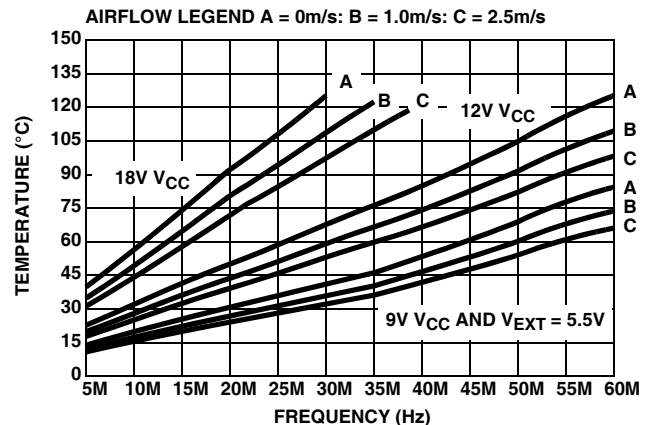
FIGURE 14. DRIVER AND RECEIVER TPD VARIANCE vs V_{CC} 

FIGURE 15. DRIVER RISE TIME vs VH RAIL, VARIOUS LOADS

FIGURE 16. STATIC I_{CC} vs V_{CC} FIGURE 17. DEVICE POWER DISSIPATION WITH $V_{CC}-V_{EE} = 18, 12$ AND 9.0 ($V_{EXT} = 5.5V$) VOLTS. ALL FOUR PINS MAKING TWO TRANSITIONS PER PERIODFIGURE 18. CALCULATED JUNCTION TEMP ABOVE AMBIENT WITH $V_{CC}-V_{EE} = 18, 12$ AND 9.0 ($V_{EXT} = 5.5V$) VOLTS. ALL FOUR PINS MAKING TWO TRANSITIONS PER PERIOD

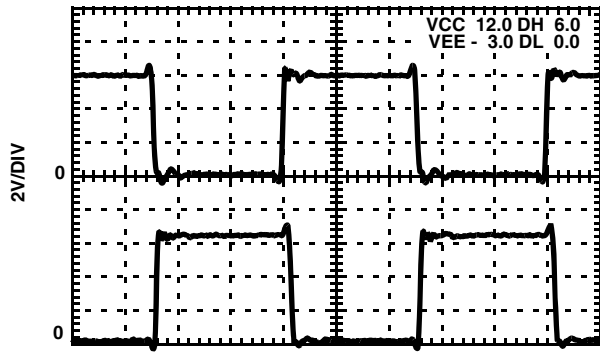
Typical Performance Curves Device installed on Intersil ISL55100B Evaluation Board. (Continued)

FIGURE 19. FREQUENCY OF 10MHz = 50ns PATTERN RATE

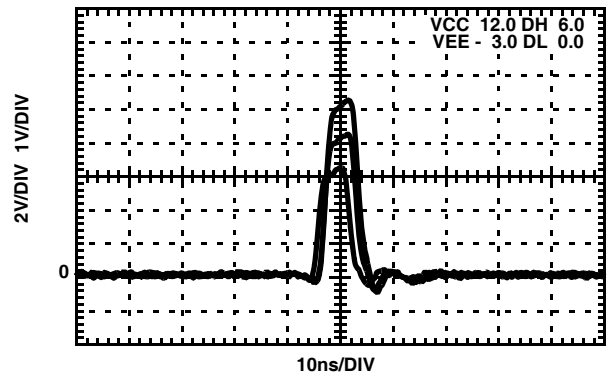
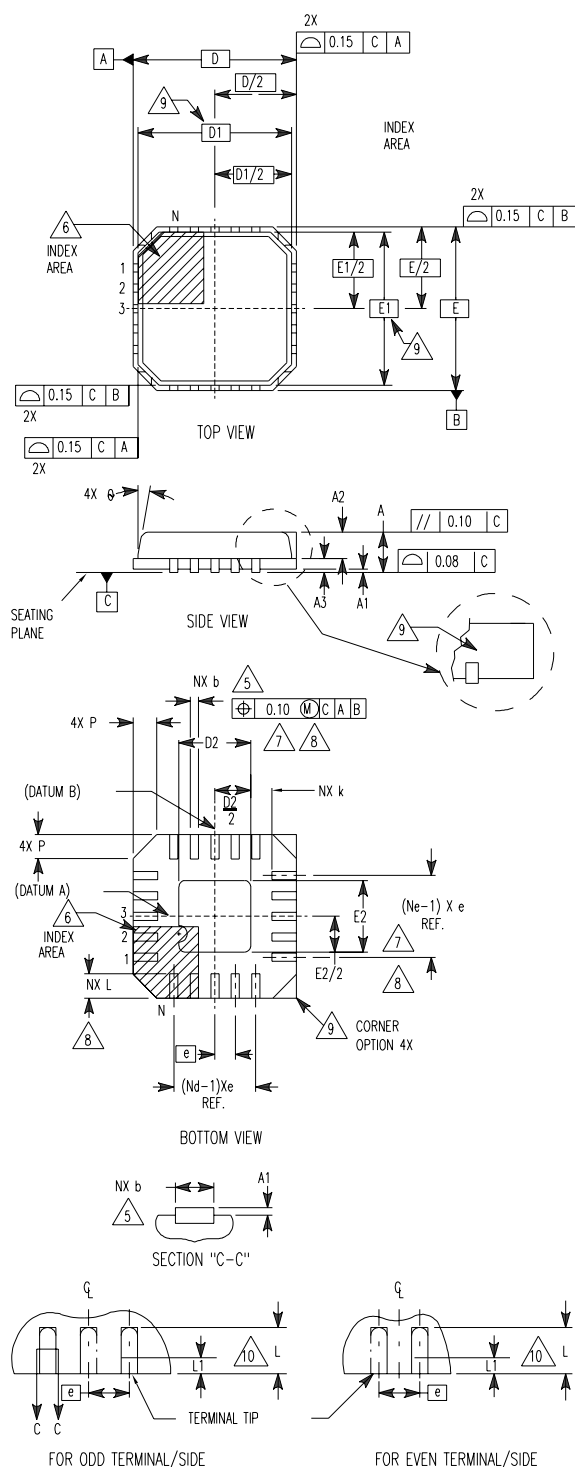


FIGURE 20. MINIMUM PULSE WIDTH VH 6/8/10V

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L72.10x10

72 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3	0.20 REF			9
b	0.18	0.25	0.30	5, 8
D	10.00 BSC			-
D1	9.75 BSC			9
D2	5.85	6.00	6.15	7, 8
E	10.00 BSC			-
E1	9.75 BSC			9
E2	5.85	6.00	6.15	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.30	0.40	0.50	8, 10
N	72			2
Nd	18			3
Ne	18			3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VNND-3 except for the "L" min dimension.

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