4-Mbit (256K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62147CV25, CY62147CV30, and CY62147CV33**
- **Ultra-low active power**
  - **Typical active current: 1.5 mA @ f = 1 MHz**
  - **Typical active current: 8 mA @ f = f_{max}**
- **Ultra low standby power**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered 48-ball BGA and 44-pin TSOPII**
- **Also available in Lead-Free packages**
- **Byte power-down feature**

Functional Description[1]

The CY62147DV30 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode reducing power consumption by more than 99% when deselected (CE HIGH or both BLE and BHE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation (CE LOW and WE LOW).

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147DV30 is available in a 48-ball VFBGA, 44 Pin TSOPII packages.

Logic Block Diagram
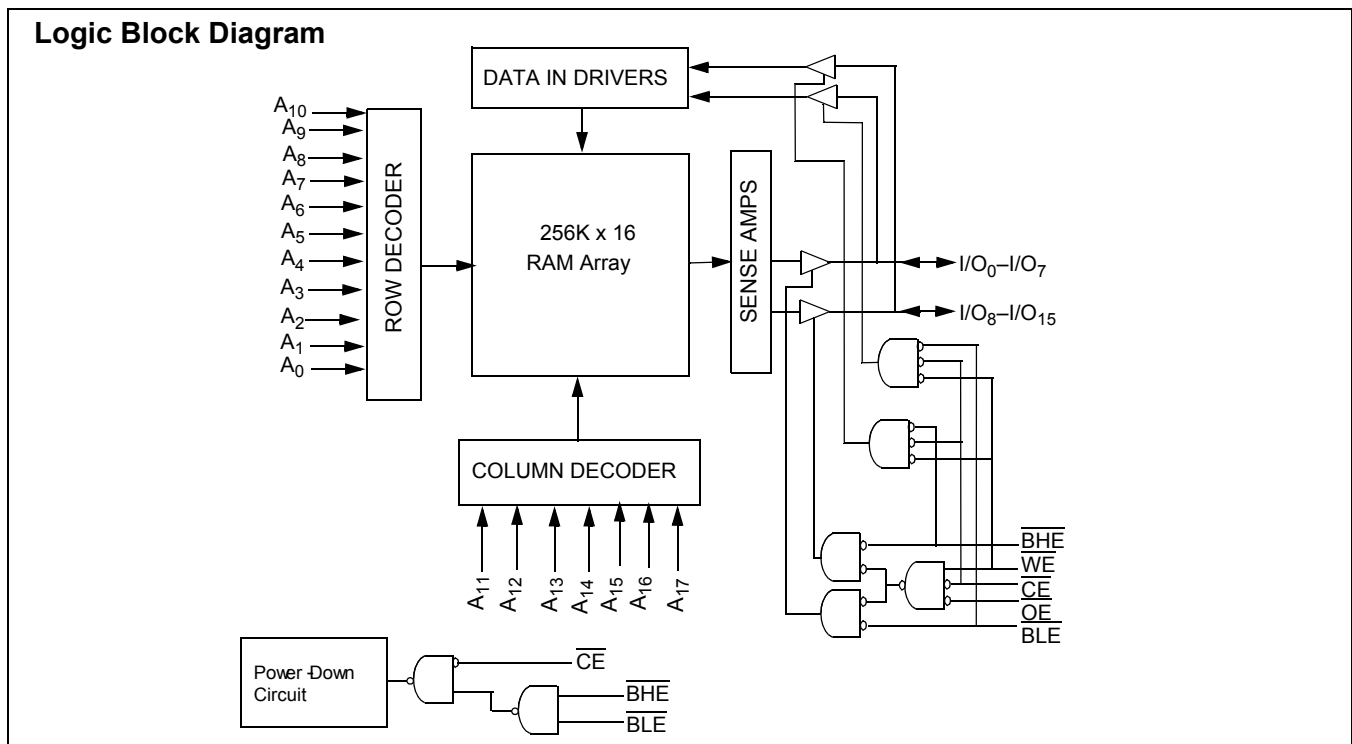
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configuration[2, 3, 4]

VFBGA (Top View)
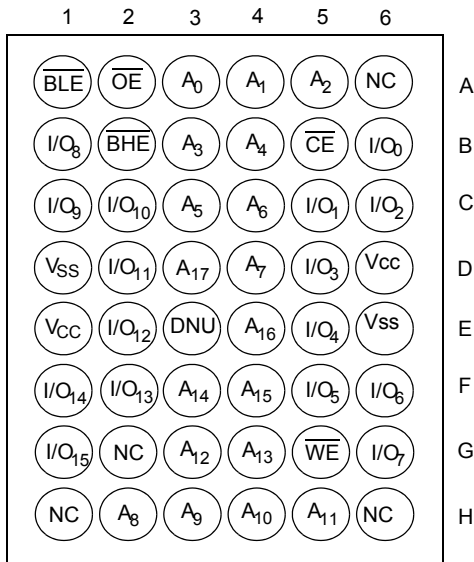
44 TSOP II (Top View)
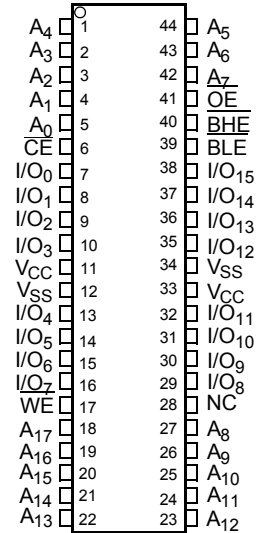
Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[5]	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ.[5]	Max.
CY62147DV30L	2.20V	3.0	3.60	45	1.5	3	10	20	2	12
CY62147DV30LL										8
CY62147DV30L	2.20V	3.0	3.60	55	1.5	3	8	15	2	12
CY62147DV30LL										8
CY62147DV30L	2.20V	3.0	3.60	70	1.5	3	8	15	2	12
CY62147DV30LL										8

Notes:
2. NC pins are not internally connected on the die.
3. DNU pins have to be left floating or tied to V_{SS} to ensure proper application.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground
Potential ....–0.3V to + $V_{CC(MAX)}$ + 0.3V

DC Voltage Applied to Outputs
in High-Z State[6,7]..........................–0.3V to $V_{CC(MAX)}$ + 0.3V

DC Input Voltage[6,7]......................–0.3V to $V_{CC(MAX)}$ + 0.3V

Output Current into Outputs (LOW)............................. 20 mA

Static Discharge Voltage.. >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. >200 mA

Device	Range	Ambient Temperature (T_A)	V_{CC}[8]
CY62147DV30L	Industrial	–40°C to +85°C	2.20V to 3.60V
CY62147DV30LL			

Electrical Characteristics (Over the Operating Range)

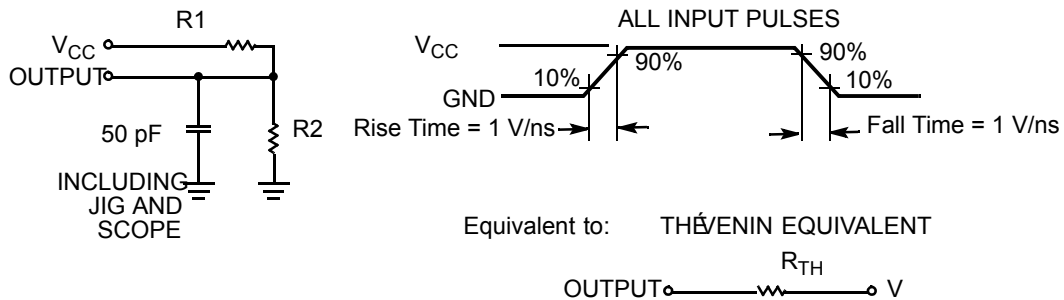| Parameter	Description	Test Conditions			CY62147DV30-45 Min.	CY62147DV30-45 Typ.[5]	CY62147DV30-45 Max.	CY62147DV30-55 Min.	CY62147DV30-55 Typ.[5]	CY62147DV30-55 Max.	CY62147DV30-70 Min.	CY62147DV30-70 Typ.[5]	CY62147DV30-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V		2.0			2.0			2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V				0.4			0.4			0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70V				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V			1.8		V_{CC} + 0.3V	1.8		V_{CC} + 0.3V	1.8		V_{CC} + 0.3V	V
		V_{CC} = 2.7V to 3.6V			2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V			–0.3		0.6	–0.3		0.6	–0.3		0.6	V
		V_{CC} = 2.7V to 3.6V			–0.3		0.8	–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$			–1		+1	–1		+1	–1		+1	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled			–1		+1	–1		+1	–1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC}=V_{CCmax} I_{OUT} = 0 mA CMOS levels			10	20		8	15		8	15	mA
		f = 1 MHz				1.5	3		1.5	3		1.5	3	mA
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	CE $\geq V_{CC}$–0.2V, $V_{IN} \geq V_{CC}$–0.2V, $V_{IN} \leq$ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC} = 3.60V	L			2	12		2	12		2	12	μA
			LL				8			8			8	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	CE $\geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, V_{CC} = 3.60V	L			2	12		2	12		2	12	μA
			LL				8			8			8	

Notes:
6. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
7. $V_{IH(max)}$=V_{CC} + 0.75V for pulse durations less than 20 ns.
8. Full device AC operation assumes a 100-μs ramp time from 0 to V_{CC}(min) and 200-μs wait time after V_{CC} stabilization.

Capacitance (for all packages)[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance[9]

Parameter	Description	Test Conditions	BGA	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	75.13	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		8.86	8.95	°C/W

AC Test Loads and Waveforms[10]

Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

| Parameter	Description	Conditions		Min.	Typ.[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC} = 1.5V $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq 0.2V$	L			9	μA
			LL			6	
t_{CDR}[9]	Chip Deselect to Data Retention Time			0			ns
t_R[11]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[12]
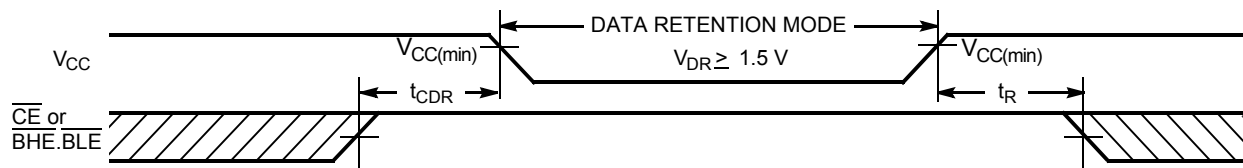
Notes:
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test condition for the 45 ns part is a load capacitance of 30 pF.
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ μs or stable at $V_{CC(min.)} \geq 100$ μs.
12. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics Over the Operating Range[13]

| Parameter	Description	45 ns[10]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[14]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[14, 15]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[14]	10		10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[14, 15]		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		45		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[14]	10		10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[14, 15]		15		20		25	ns
Write Cycle[16]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		40		60		ns
t_{AW}	Address Set-up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		45		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t_{SD}	Data Set-up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[14, 15]		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[14]	10		10		10		ns

Notes:
13. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
16. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[17, 18]
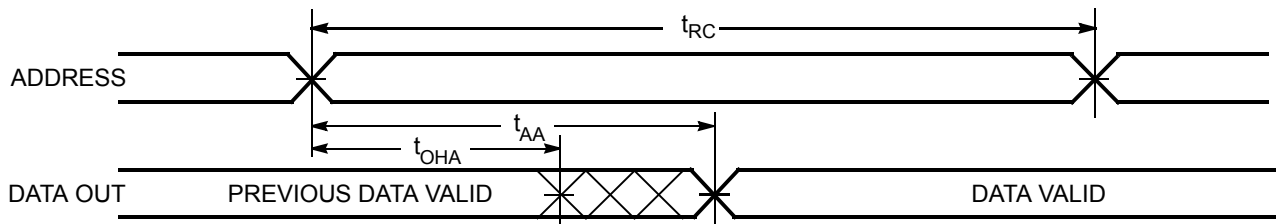
Read Cycle No. 2 (OE Controlled)[18, 19]
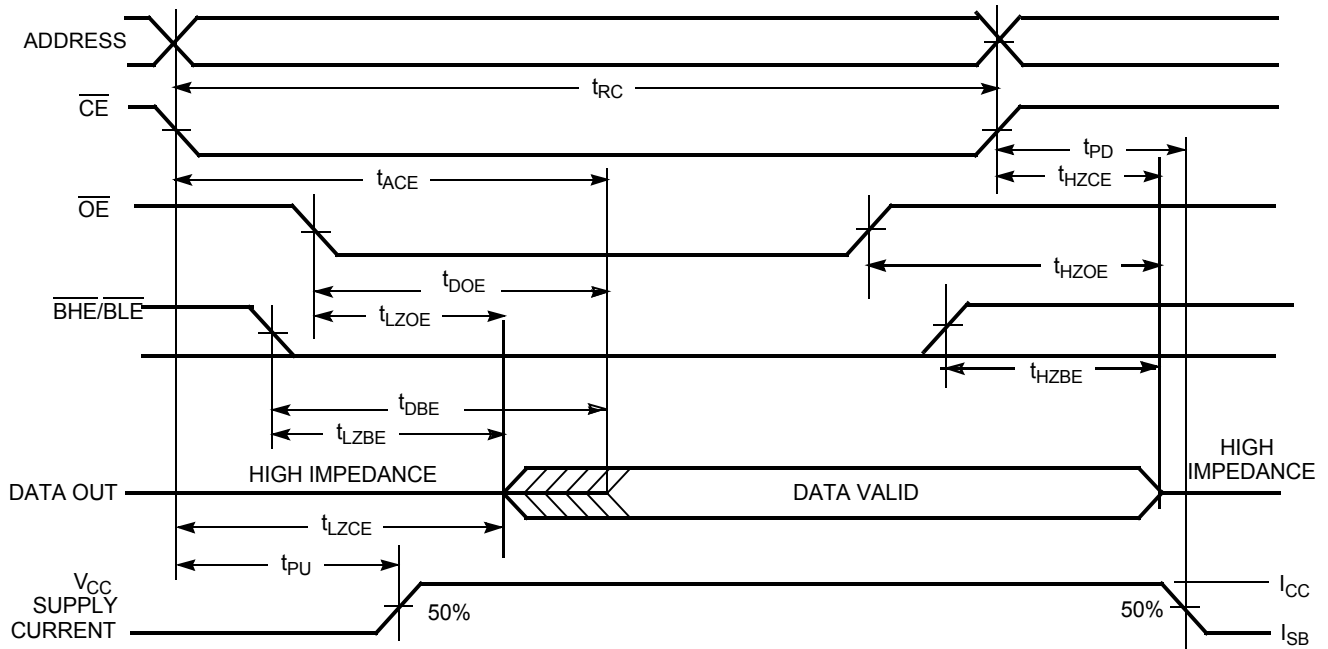
Notes:
17. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[16, 20, 21]
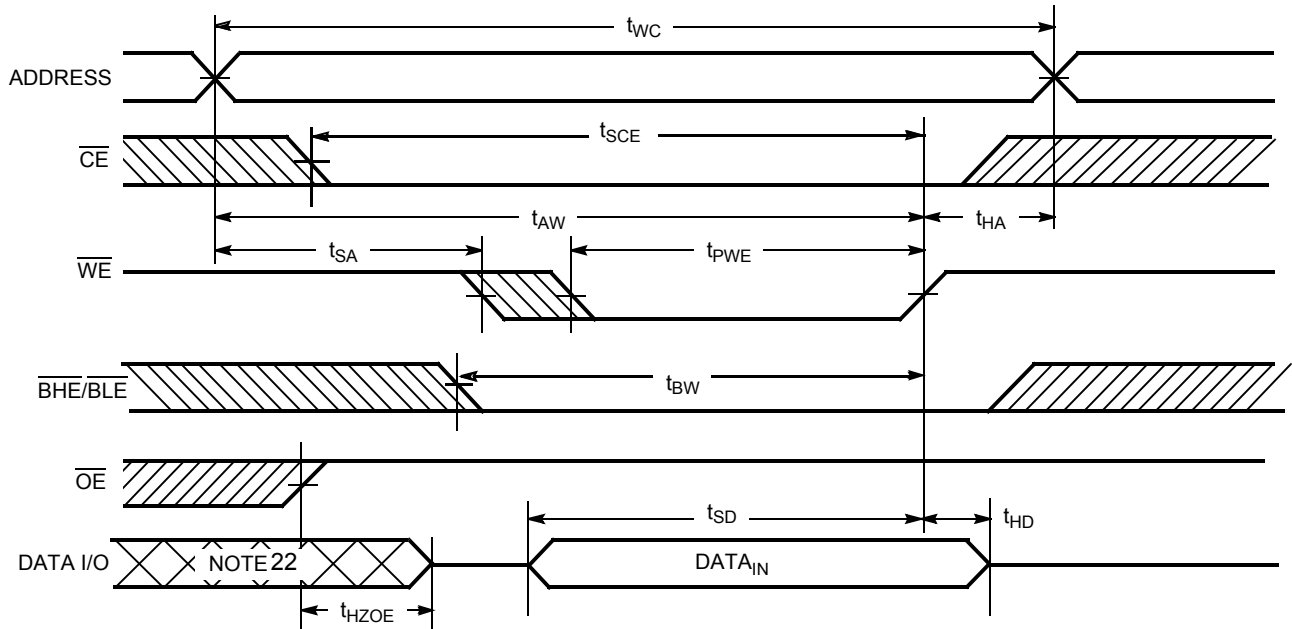
Write Cycle No. 2 ($\overline{CE}$ Controlled)[16, 20, 21]
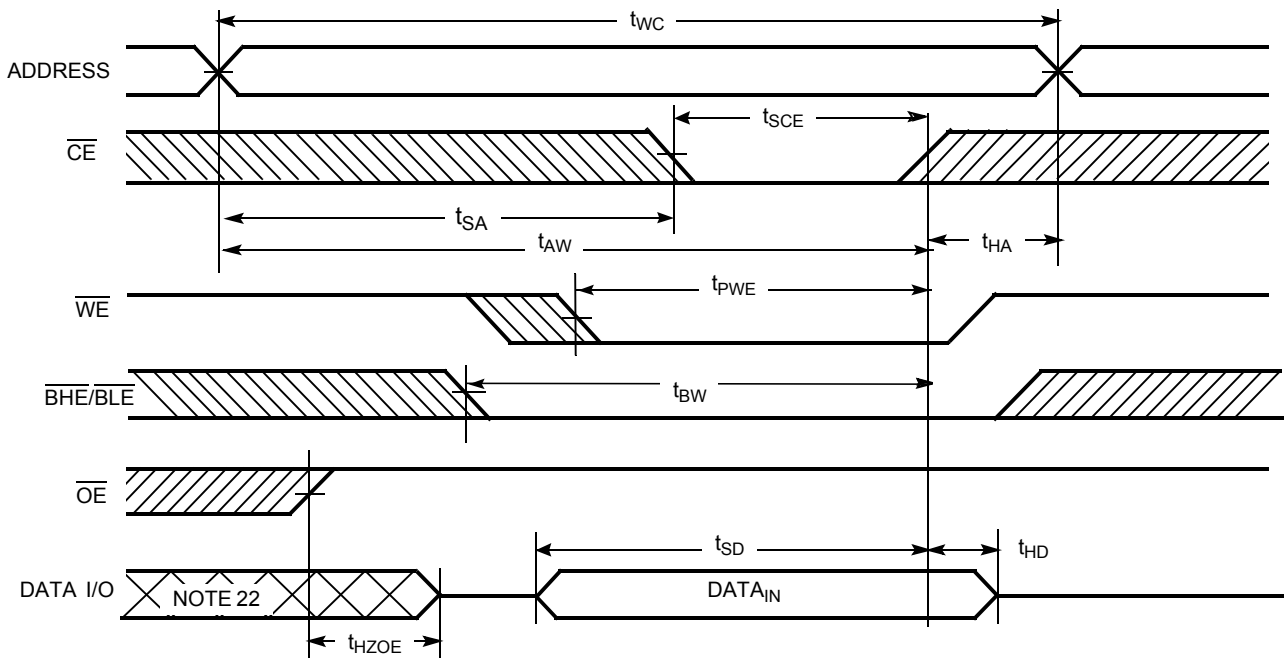
Notes:
20. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
22. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[21]
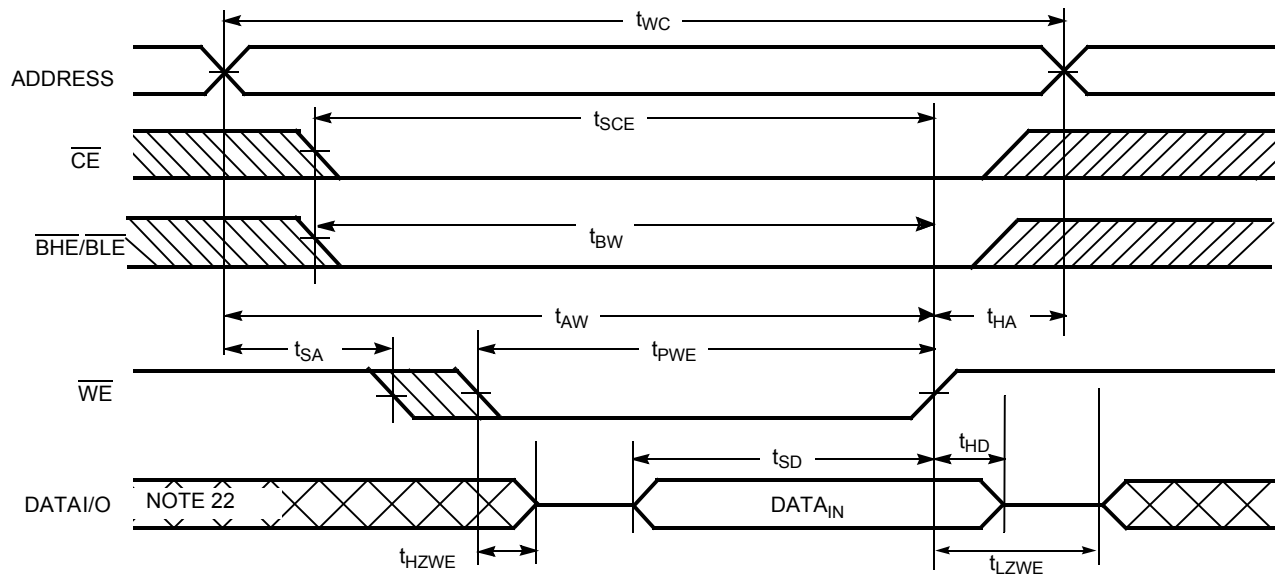
Write Cycle No. 4 ($\overline{\text{BHE}}$/$\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)[21]
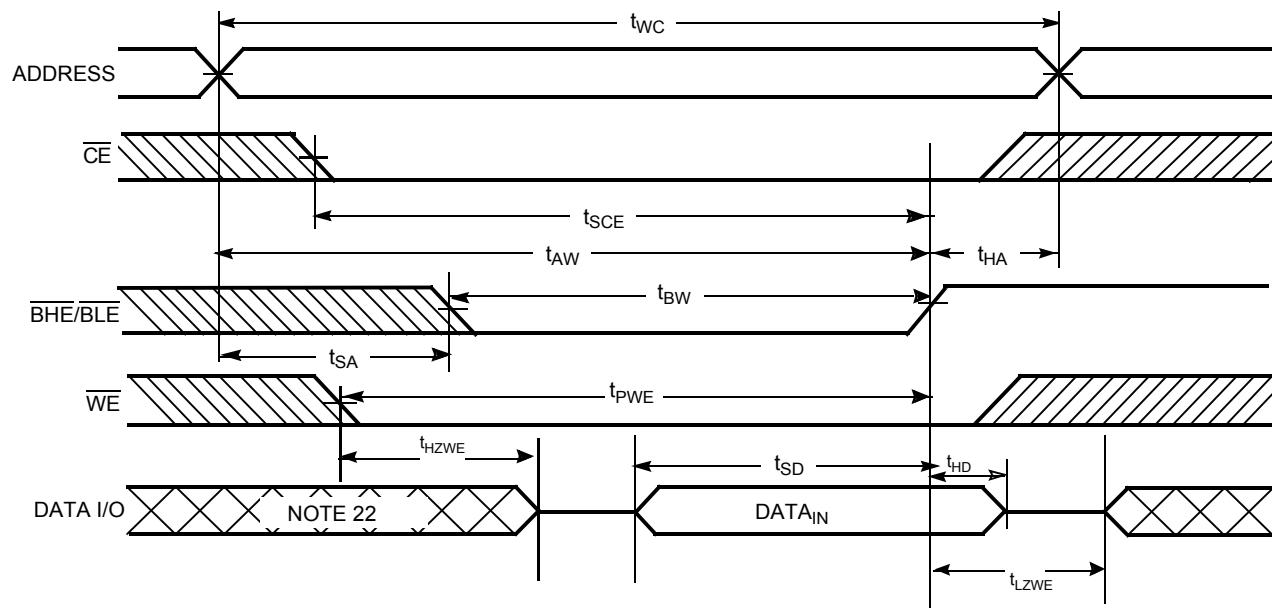
Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62147DV30LL-45BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV30LL-45BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62147DV30LL-45ZSXI	ZS-44	44-pin TSOP II (Pb-free)	
55	CY62147DV30L-55BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV30L-55BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62147DV30LL-55BVI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	
	CY62147DV30LL-55BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
55	CY62147DV30L-55ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62147DV30LL-55ZSXI			
70	CY62147DV30L-70BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV30L-70BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62147DV30LL-70BVI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	
	CY62147DV30LL-70BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
70	CY62147DV30L-70ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62147DV30LL-70ZSXI			

Package Diagram
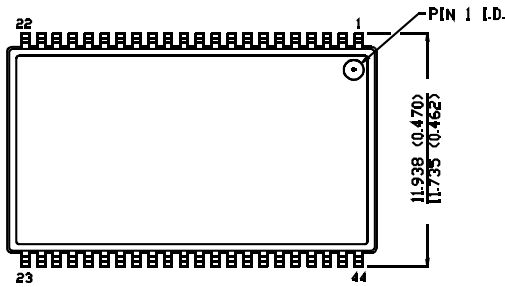
48-Lead VFBGA (6 x 8 x 1 mm) BV48A

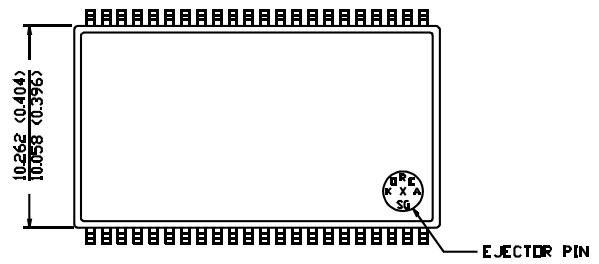TOP VIEW
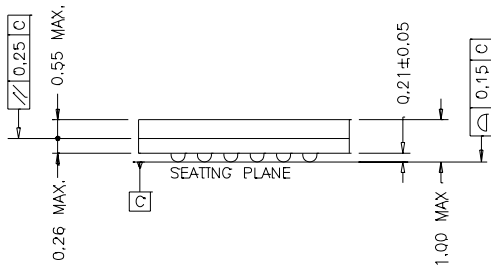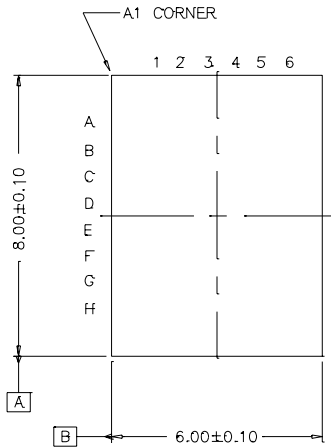
BOTTOM VIEW
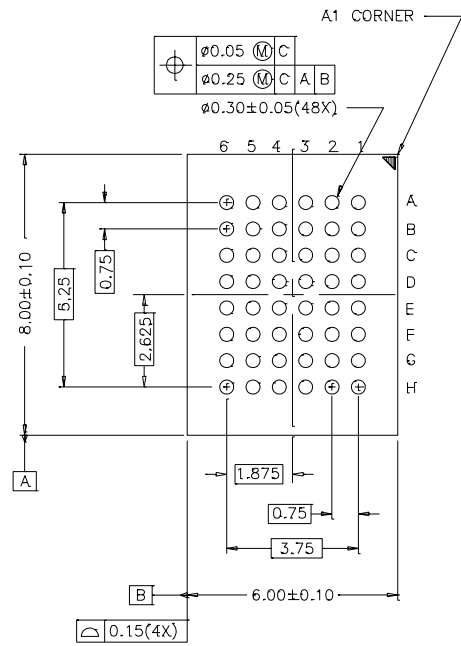
51-85150-*B

Package Diagram (continued)
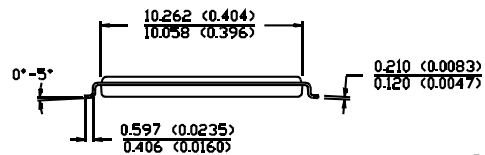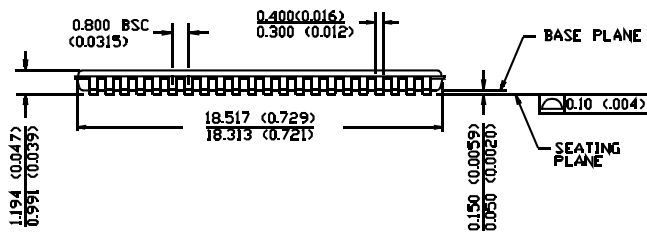
44-Pin TSOP II ZS44

DIMENSION IN MM (INCH)
MAX
MIN.

TOP VIEW

BOTTOM VIEW

51-85087-*A

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Document History Page

Document Title:CY62147DV30 MoBL® 4-Mbit (256K x 16) Static RAM				
Document Number: 38-05340				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	127481	06/17/03	HRT	New Data Sheet
*A	131010	01/23/04	CBD	Change from Advance to Preliminary
*B	213252	See ECN	AJU	Change from Preliminary to Final Added 70 ns speed bin Modified footnote 7 to include ramp time and wait time Modified input and output capacitance values to 10 pF Modified Thermal Resistance values on page 4 Added "Byte power-down feature" in the features section Modified Ordering Information for Pb-free parts
*C	257349	See ECN	PCI	Modified ordering information for 70-ns Speed Bin
*D	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #10 on page #4 Added Pb-free package ordering information on page # 9 Changed 44-lead TSOP-II package name on page 11 from Z44 to ZS44 Standardized Icc values across 'L' and 'LL' bins