ELPIDA

**PRELIMINARY DATA SHEET**

# 128MB 32-bit Direct Rambus DRAM RIMM™ Module

## EBR12EC8ABKD (32M words × 18 bits × 2 channels)

### Description

The 32-bit Direct Rambus RIMM module is a general-purpose high-performance lines of memory modules suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and latency are required.

The EBR12EC8ABKD consists of 4 pieces of 288Mb Direct Rambus DRAM (Direct RDRAM) devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits the use of conventional system and board design technologies. The 32-bit RIMM modules support 1066MHz or 800MHz transfer rate per pin, resulting in total module bandwidth of 3.2GB/s.

The 32-bit RIMM module provides two independent 18 bit memory channels to facilitate compact system design. The "Thru" Channel enters and exits the module to support a connection to or from a controller, memory slot, or termination. The "Term" Channel is terminated on the module and supports a connection from a controller or another memory slot.

The RDRAM® architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM device multi-bank architecture supports up to four simultaneous transactions per device.

### Features

- 128MB Direct RDRAM storage and 128 banks total on module
- 2 independent Direct RDRAM channels, 1 pass through and 1 terminated on 32-bit RIMM module
- High speed 1066MHz/800MHz Direct RDRAM devices
- 232 edge connector pads with 1mm pad spacing
  - Module PCB size: 133.35mm × 34.925mm × 1.27mm
  - Gold plated edge connector pads contacts
- Serial Presence Detect (SPD) support
- Operates from a 2.5V supply
- Low power and power down self refresh modes
- Separate Row and Column buses for higher efficiency
- RDRAMs uses Chip Scale Package (CSP)
  - FBGA package



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This product became EOL in April, 2004.

## Ordering Information

| Part number | Organization | I/O Freq. (MHz) | RAS access time (ns) | Package | Mounted devices |
|---|---|---|---|---|---|
| EBR12EC8ABKD-AEP | 32M x 18 x 2 | 1066 | 32 (32P) | 232 edge connector pads RIMM with heat spreader | EDR2518ABSE |
| EBR12EC8ABKD-AE | | | 32 | Edge connector: Gold plated | |
| EBR12EC8ABKD-AD | | | 35 | | |
| EBR12EC8ABKD-8C | | 800 | 40 | | |

## Module Pad Names

| Pad | Signal name | Pad | Signal name | Pad | Signal name | Pad | Signal name |
|---|---|---|---|---|---|---|---|
| A1 | GND | B1 | GND | A59 | GND | B59 | GND |
| A2 | SCK_THRU_L | B2 | CMD_THRU_L | A60 | VTERM | B60 | VTERM |
| A3 | GND | B3 | GND | A61 | VTERM | B61 | VTERM |
| A4 | DQA8_THRU_L | B4 | DQA7_THRU_L | A62 | GND | B62 | GND |
| A5 | GND | B5 | GND | A63 | DQA3_THRU_R | B63 | DQA4_THRU_R |
| A6 | DQA6_THRU_L | B6 | DQA5_THRU_L | A64 | GND | B64 | GND |
| A7 | GND | B7 | GND | A65 | DQA5_THRU_R | B65 | DQA6_THRU_R |
| A8 | DQA4_THRU_L | B8 | DQA3_THRU_L | A66 | GND | B66 | GND |
| A9 | GND | B9 | GND | A67 | DQA7_THRU_R | B67 | DQA8_THRU_R |
| A10 | DQA2_THRU_L | B10 | DQA1_THRU_L | A68 | GND | B68 | GND |
| A11 | GND | B11 | GND | A69 | VDD | B69 | VDD |
| A12 | DQA0_THRU_L | B12 | CTMN_THRU_L | A70 | GND | B70 | GND |
| A13 | GND | B13 | GND | A71 | SCK_THRU_R | B71 | CTMN_TERM_L |
| A14 | CFM_THRU_L | B14 | CTM_THRU_L | A72 | GND | B72 | GND |
| A15 | GND | B15 | GND | A73 | CMD_THRU_R | B73 | CTM_TERM_L |
| A16 | CFMN_THRU_L | B16 | ROW2_THRU_L | A74 | GND | B74 | GND |
| A17 | GND | B17 | GND | A75 | VREF | B75 | VCMOS |
| A18 | ROW1_THRU_L | B18 | ROW0_THRU_L | A76 | VDD | B76 | VDD |
| A19 | GND | B19 | GND | A77 | SVDD | B77 | SWP |
| A20 | COL4_THRU_L | B20 | COL3_THRU_L | A78 | VDD | B78 | VDD |
| A21 | GND | B21 | GND | A79 | SCL | B79 | SDA |
| A22 | COL2_THRU_L | B22 | COL1_THRU_L | A80 | VDD | B80 | VDD |
| A23 | GND | B23 | GND | A81 | SA0 | B81 | SA1 |
| A24 | COL0_THRU_L | B24 | DQB0_THRU_L | A82 | VDD | B82 | VDD |
| A25 | GND | B25 | GND | A83 | SA2 | B83 | SIN_TERM |
| A26 | DQB1_THRU_L | B26 | DQB2_THRU_L | A84 | GND | B84 | GND |
| A27 | GND | B27 | GND | A85 | DQB8_TERM | B85 | DQB7_TERM |
| A28 | DQB3_THRU_L | B28 | DQB4_THRU_L | A86 | GND | B86 | GND |
| A29 | GND | B29 | GND | A87 | DQB6_TERM | B87 | DQB5_TERM |
| A30 | DQB5_THRU_L | B30 | DQB6_THRU_L | A88 | GND | B88 | GND |
| A31 | GND | B31 | GND | A89 | DQB4_TERM | B89 | DQB3_TERM |
| A32 | DQB7_THRU_L | B32 | DQB8_THRU_L | A90 | GND | B90 | GND |
| A33 | GND | B33 | GND | A91 | DQB2_TERM | B91 | DQB1_TERM |

| Pad | Signal name | Pad | Signal name |
|---|---|---|---|
| A34 | SOUT_THRU | B34 | SIN_THRU |
| A35 | GND | B35 | GND |
| A36 | DQB8_THRU_R | B36 | DQB7_THRU_R |
| A37 | GND | B37 | GND |
| A38 | DQB6_THRU_R | B38 | DQB5_THRU_R |
| A39 | GND | B39 | GND |
| A40 | DQB4_THRU_R | B40 | DQB3_THRU_R |
| A41 | GND | B41 | GND |
| A42 | DQB2_THRU_R | B42 | DQB1_THRU_R |
| A43 | GND | B43 | GND |
| A44 | DQB0_THRU_R | B44 | COL0_THRU_R |
| A45 | GND | B45 | GND |
| A46 | COL1_THRU_R | B46 | COL2_THRU_R |
| A47 | GND | B47 | GND |
| A48 | COL3_THRU_R | B48 | COL4_THRU_R |
| A49 | GND | B49 | GND |
| A50 | ROW0_THRU_R | B50 | ROW1_THRU_R |
| A51 | GND | B51 | GND |
| A52 | ROW2_THRU_R | B52 | CFMN_THRU_R |
| A53 | GND | B53 | GND |
| A54 | CTM_THRU_R | B54 | CFM_THRU_R |
| A55 | GND | B55 | GND |
| A56 | CTMN_THRU_R | B56 | DQA0_THRU_R |
| A57 | GND | B57 | GND |
| A58 | DQA1_THRU_R | B58 | DQA2_THRU_R |

| Pad | Signal name | Pad | Signal name |
|---|---|---|---|
| A92 | GND | B92 | GND |
| A93 | DQB0_TERM | B93 | COL0_TERM |
| A94 | GND | B94 | GND |
| A95 | COL1_TERM | B95 | COL2_TERM |
| A96 | GND | B96 | GND |
| A97 | COL3_TERM | B97 | COL4_TERM |
| A98 | GND | B98 | GND |
| A99 | ROW0_TERM | B99 | ROW1_TERM |
| A100 | GND | B100 | GND |
| A101 | ROW2_TERM | B101 | CFMN_TERM |
| A102 | GND | B102 | GND |
| A103 | CTM_TERM_R | B103 | CFM_TERM |
| A104 | GND | B104 | GND |
| A105 | CTMN_TERM_R | B105 | DQA0_TERM |
| A106 | GND | B106 | GND |
| A107 | DQA1_TERM | B107 | DQA2_TERM |
| A108 | GND | B108 | GND |
| A109 | DQA3_TERM | B109 | DQA4_TERM |
| A110 | GND | B110 | GND |
| A111 | DQA5_TERM | B111 | DQA6_TERM |
| A112 | GND | B112 | GND |
| A113 | DQA7_TERM | B113 | DQA8_TERM |
| A114 | GND | B114 | GND |
| A115 | CMD_TERM | B115 | SCK_TERM |
| A116 | GND | B116 | GND |

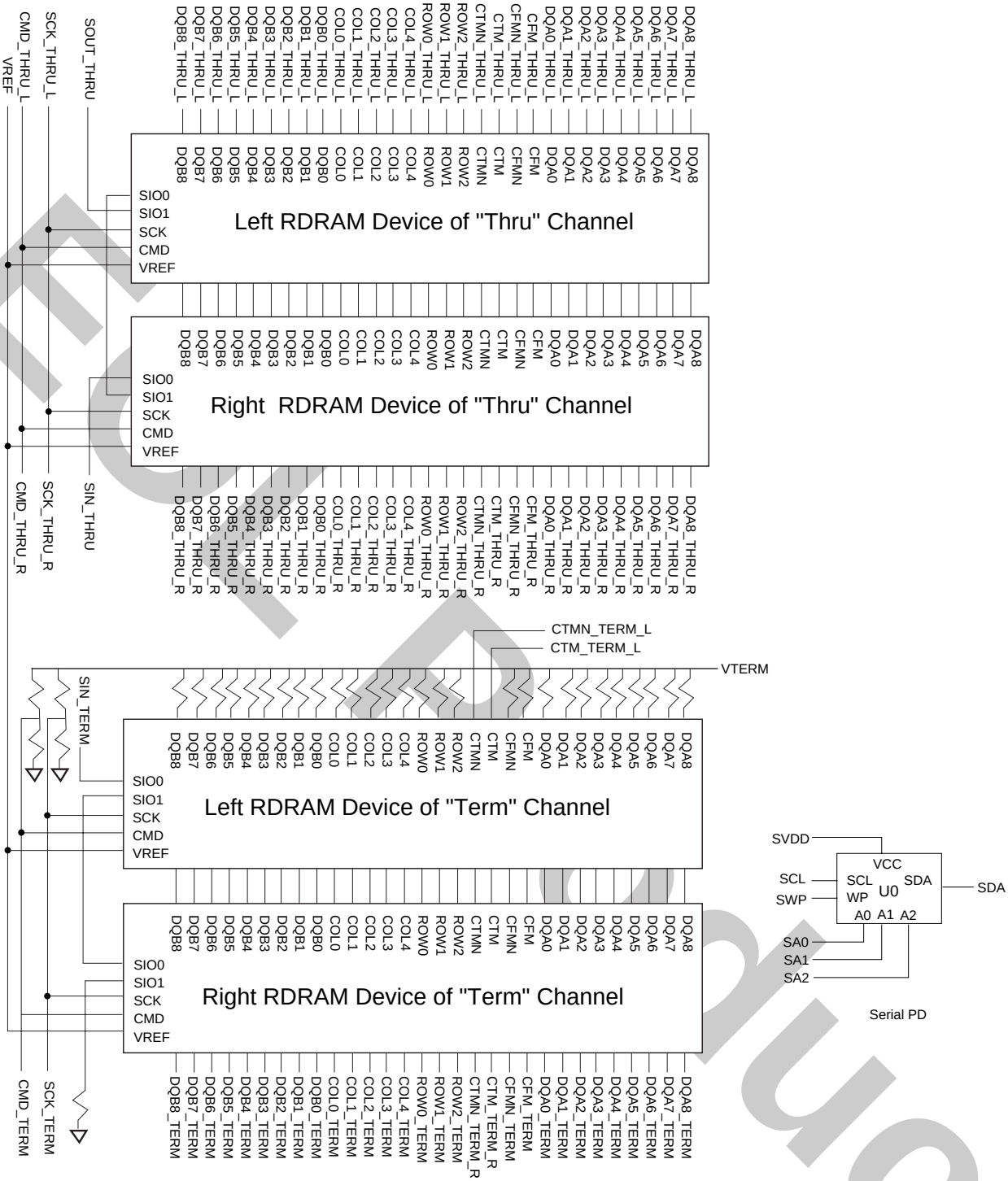
## Module Connector Pad Description

| Signal | Module connector pads | I/O | Type | Description |
|---|---|---|---|---|
| CFM_THRU_L | A14 | I | RSL | Clock From Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity. |
| CFM_THRU_R | B54 | I | RSL | Clock From Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity. |
| CFMN_THRU_L | A16 | I | RSL | Clock From Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity. |
| CFMN_THRU_R | B52 | I | RSL | Clock From Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity. |
| CMD_THRU_L | B2 | I | VCMOS | Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to left RDRAM device on "Thru" Channel. |
| CMD_THRU_R | A73 | I | VCMOS | Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to right RDRAM device on "Thru" Channel. |
| COL4_THRU_L.. COL0_THRU_L | A20, B20, A22, B22, A24 | I | RSL | "Thru" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to left RDRAM device on "Thru" Channel. |
| COL4_THRU_R.. COL0_THRU_R | B48, A48, B46, A46, B44 | I | RSL | "Thru" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to right RDRAM device on "Thru" Channel. |
| CTM_THRU_L | B14 | I | RSL | Clock To Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity. |
| CTM_THRU_R | A54 | I | RSL | Clock To Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity. |
| CTMN_THRU_L | B12 | I | RSL | Clock To Master. Connects to left RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity. |
| CTMN_THRU_R | A56 | I | RSL | Clock To Master. Connects to right RDRAM device on "Thru" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity. |
| DQA8_THRU_L.. DQA0_THRU_L | A4, B4, A6, B6, A8, B8, A10, B10, A12 | I/O | RSL | "Thru" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to left RDRAM device on "Thru" Channel. |
| DQA8_THRU_R.. DQA0_THRU_R | B67, A67, B65, A65, B63, A63, B58, A58, B56 | I/O | RSL | "Thru" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to right RDRAM device on "Thru" Channel. |
| DQB8_THRU_L.. DQB0_THRU_L | B32, A32, B30, A30, B28, A28, B26, A26, B24 | I/O | RSL | "Thru" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to left RDRAM device on "Thru" Channel. |
| DQB8_THRU_R.. DQB0_THRU_R | A36, B36, A38, B38, A40, B40, A42, B42, A44 | I/O | RSL | "Thru" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Thru” Channel. Connects to right RDRAM device on "Thru" Channel. |
| ROW2_THRU_L.. ROW0_THRU_L | B16, A18, B18 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. Connects to left RDRAM device on "Thru" Channel. |
| ROW2_THRU_R.. ROW0_THRU_R | A52, B50, A50 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. Connects to right RDRAM device on "Thru" Channel. |

| Signal | Module connector pads | I/O | Type | Description |
|---|---|---|---|---|
| SCK_THRU_L | A2 | I | VCMOS | Serial Clock input. Clock source used to read from and write to "Thru" Channel RDRAM control registers. Connects to left RDRAM device on "Thru" Channel. |
| SCK_THRU_R | A71 | I | VCMOS | Serial Clock input. Clock source used to read from and write to "Thru" Channel RDRAM control registers. Connects to right RDRAM device on "Thru" Channel. |
| SIN_THRU | B34 | I/O | VCMOS | "Thru" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of right RDRAM device on "Thru" Channel. |
| SOUT_THRU | A34 | I/O | VCMOS | "Thru" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of left RDRAM device on "Thru" Channel. |
| CFM_TERM | B103 | I | RSL | Clock from master. Connects to right RDRAM device on "Term" Channel. Interface clock used for receiving RSL signals from the controller. Positive polarity. |
| CFMN_TERM | B101 | I | RSL | Clock from master. Connects to right RDRAM device on "Term" Channel. Interface clock used for receiving RSL signals from the controller. Negative polarity. |
| CMD_TERM | A115 | I | VCMOS | Serial Command Input used to read from and write to the control registers. Also used for power management. Connects to right RDRAM device on "Term" Channel. |
| COL4_TERM.. COL0_TERM | B97, A97, B95, A95, B93 | I | RSL | "Term" Channel Column bus. 5-bit bus containing control and address information for column accesses. Connects to right RDRAM device on "Term" Channel. |
| CTM_TERM_L | B73 | I | RSL | Clock To Master. Connects to left RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity. |
| CTM_TERM_R | A103 | I | RSL | Clock To Master. Connects to right RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Positive polarity. |
| CTMN_TERM_L | B71 | I | RSL | Clock To Master. Connects to left RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity. |
| CTMN_TERM_R | A105 | I | RSL | Clock To Master. Connects to right RDRAM device on "Term" Channel. Interface clock used for transmitting RSL signals to the controller. Negative polarity. |
| DQA8_TERM.. DQA0_TERM | B113, A113, B111, A111, B109, A109, B107, A107, B105 | I/O | RSL | "Term" Channel Data bus A. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Term” Channel. Connects to right RDRAM device on "Term" Channel. |
| DQB8_TERM.. DQB0_TERM | A85, B85, A87, B87, A89, B89, A91, B91, A93 | I/O | RSL | "Term" Channel Data bus B. A 9-bit bus carrying a byte of read or write data between the controller and RDRAM devices on “Term” Channel. Connects to right RDRAM device on "Term" Channel. |
| ROW2_TERM.. ROW0_TERM | A101, B99, A99 | I | RSL | "Term" Channel Row bus. 3-bit bus containing control and address information for row accesses. Connects to right RDRAM device on "Term" Channel. |
| SCK_TERM | B115 | I | VCMOS | Serial Clock input. Clock source used to read from and write to "Term" Channel RDRAM control registers. Connects to right RDRAM device on "Term" Channel. |
| SIN_TERM | B83 | I/O | VCMOS | "Term" Channel Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of left RDRAM device on "Term" Channel. |
| VTERM | A60, B60, A61, B61 | | | "Term" Channel Termination voltage. |

| Signal | Module connector pads | I/O | Type | Description |
|---|---|---|---|---|
| GND | A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A35, A37, A39, A41, A43, A45, A47, A49, A51, A53, A55, A57, A59, A62, A64, A66, A68, A70, A72, A74, A84, A86, A88, A90, A92, A94, A96, A98, A100, A102, A104, A106, A108, A110, A112, A114, A116, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B35, B37, B39, B41, B43, B45, B47, B49, B51, B53, B55, B57, B59, B62, B64, B66, B68, B70, B72, B74, B84, B86, B88, B90, B92, B94, B96, B98, B100, B102, B104, B106, B108, B110, B112, B114, B116 | | | Ground reference for RDRAM core and interface. |
| SA0 | A81 | I | SVDD | Serial Presence Detect Address 0 |
| SA1 | B81 | I | SVDD | Serial Presence Detect Address 1. |
| SA2 | A83 | I | SVDD | Serial Presence Detect Address 2. |
| SCL | A79 | I | SVDD | Serial Presence Detect Clock. |
| SDA | B79 | I/O | SVDD | Serial Presence Detect Data (Open Collector I/O). |
| SVDD | A77 | | | SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2. |
| SWP | B77 | I | SVDD | Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read. |
| VCMOS | B75 | | | CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT. |
| VDD | A69, B69, A76, B76, A78, B78, A80, B80, A82, B82 | | | Supply voltage for the RDRAM core and interface logic. |
| VREF | A75 | | | Logic threshold reference voltage for both "Thru" Channel and "Term" Channel RSL signals. |

## Block Diagram



## Electrical Specifications

### Absolute Maximum Ratings

| Symbol | Parameter | min. | max. | Unit |
|---|---|---|---|---|
| VI,ABS | Voltage applied to any RSL or CMOS signal pad with respect to GND | –0.3 | VDD + 0.3 | V |
| VDD,ABS | Voltage on VDD with respect to GND | –0.5 | VDD + 1.0 | V |
| TSTORE | Storage temperature | –50 | +100 | °C |

**Caution**

**Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### DC Recommended Electrical Conditions

| Symbol | Parameter and conditions | min. | max. | Unit |
|---|---|---|---|---|
| VDD | Supply voltage[*1] | 2.50 – 0.13 | 2.50 + 0.13 | V |
| VCMOS | CMOS I/O power supply at pad<br>2.5V controllers | 2.50 – 0.13 | 2.50 + 0.25 | V |
| | 1.8V controllers | 1.8 – 0.1 | 1.8 + 0.2 | V |
| VREF | Reference voltage[*1] | 1.4 – 0.2 | 1.4 + 0.2 | V |
| SVDD | Serial Presence Detector- positive power supply | 2.2 | 3.6 | V |
| VTERM | Termination Voltage | 1.89 – 0.09 | 1.89 + 0.09 | V |

Note: 1. See Direct RDRAM datasheet for more details.

**AC Electrical Specifications**

| Symbol | Parameter and Conditions[*1] | Grade | min. | typ. | max. | Unit |
|---|---|---|---|---|---|---|
| Z | Module Impedance of RSL signals | | 25.2 | 28.0 | 30.8 | Ω |
| | Module Impedance of SCK and CMD signals | | 23.8 | 28.0 | 32.2 | Ω |
| TPD | Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN,CFM, and CFMN) [*2] | | — | — | TBD | ns |
| ΔTPD | Propagation delay variation of RSL signals with respect to TPD [*1, 3] | | TBD | — | TBD | ps |
| ΔTPD-CMOS | Propagation delay variation of SCK signal with respect to an average clock delay [*1] | | TBD | — | TBD | ps |
| ΔTPD- SCK,CMD | Propagation delay variation of CMD signal with respect to SCK signal | | TBD | — | TBD | ps |
| Vα/VIN | Attenuation Limit | -AEP<br>-AE<br>-AD<br>-8C | — | — | TBD | % |
| VXF/VIN | Forward crosstalk coefficient (300ps input rise time 20% - 80%) | -AEP<br>-AE<br>-AD<br>-8C | — | — | TBD | % |
| VXB/VIN | Backward crosstalk coefficient (300ps input rise time 20% - 80%) | -AEP<br>-AE<br>-AD<br>-8C | — | — | TBD | % |
| RDC | DC Resistance Limit | -AEP<br>-AE<br>-AD<br>-8C | — | — | TBD | Ω |

Notes 1. Specifications apply per channel.

2. TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

3. If the RIMM module meets the following specification, then it is compliant to the specification. If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔTPD Specification" table.

**Adjusted ΔTPD Specification**

| Symbol | Parameter and conditions | Adjusted min./max. | Absolute min. | Absolute max. | Unit |
|---|---|---|---|---|---|
| ΔTPD | Propagation delay variation of RSL signals with respect to TPD | +/– [17+(18*N*ΔZ0)] [*1] | TBD | TBD | ps |

Note N = Number of RDRAM devices installed on the RIMM module.

ΔZ0 = delta Z0% = (max. Z0 - min. Z0) / (min. Z0)

(max. Z0 and min. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

**RIMM Module Current Profile**

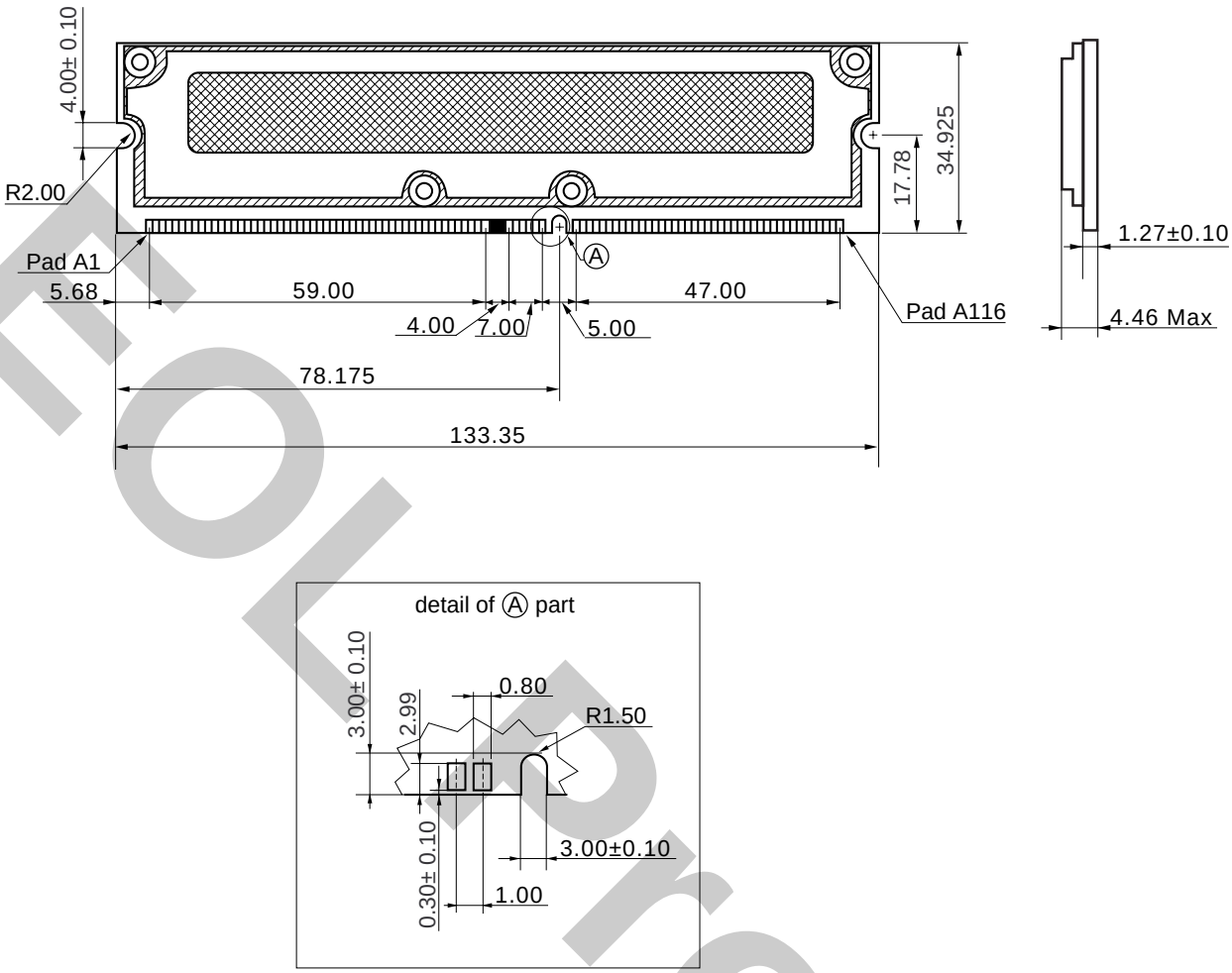
| IDD | RIMM module power conditions [*1] | Grade | max. | Unit |
|---|---|---|---|---|
| IDD1 | One RDRAM device per channel in Read [*2], balance in NAP mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |
| IDD2 | One RDRAM device per channel in Read [*2], balance in Standby mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |
| IDD3 | One RDRAM device per channel in Read [*2], balance in Active mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |
| IDD4 | One RDRAM device per channel in Write, balance in NAP mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |
| IDD5 | One RDRAM device per channel in Write, balance in Standby mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |
| IDD6 | One RDRAM device per channel in Write, balance in Active mode | -AEP<br>-AE<br>-AD<br>-8C | TBD | mA |

Notes 1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x18 need to add 276mA for the following : VDD = 2.5V, VTERM = 1.8V, VREF = 1.4V and VDIL = VREF – 0.5V.

**Physical Outline**

Unit: mm




Note: The dimensions without tolerance specification use the default tolerance of ± 0.13.

ECA-TS2-0083-01

## CAUTION FOR HANDLING MEMORY MODULES

**When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.**
**In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.**

**When re-packing memory modules, be sure the modules are not touching each other.**
**Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.**

MDE0202

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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