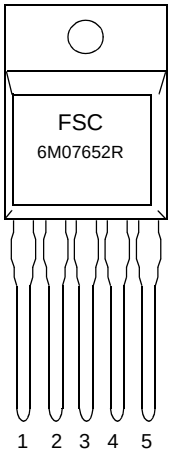
Application Note 4116

A Fairchild Power Switch (FPS) based on Switched Mode Power Supply for LCD Monitor Use

1. Introduction

This application note describes a complete flyback switched mode power supply that uses a Fairchild Power Switch. The MOSFET and its control IC are built into one package. The MOSFET is in fact a SenseFET. Various protection features are also included. Fairchild Power Switch can enhance the reliability and productivity of the system when compared to other designs. The FS6M series has a more avalanche rugged SenseFET than the previous Fairchild Power Switch series. The FS6M series features include burst mode operation for low power consumption in DPMS mode. This application note describes the features and design considerations of the FS6M series for the LCD monitor power supply and adaptor, which improves upon the existing KA5X-series.

FS6Mxx652RT has one package type: TO-220F-5L as shown below. Fairchild Power Switch is classified according to the voltage and current rating of the internal SenseFET. The FS6M series parts with absolute voltage and absolute current ratings of 650V/7A and 650V/12A. When in power saving mode, the FS6M series pulls down the output voltages to a predetermined level and enters burst mode with a switching frequency of 70kHz.



TO-220F-5L

Figure 1-1. Package Line-Up

Table 1: Product Line-up (LCD Monitor Application)

Product	Rating	Package
FS6M07652RTC	7A/650V	TO-220F-5L
FS6M12653RTC	12A/650V	TO-220F-5L

©2002 Fairchild Semiconductor Corporation

2. Internal Block and Important Features

2.1 Internal Block and Features

- Pulse by pulse current limiting
- Fixed frequency(70kHz)
- Internal Burst Mode Controller for DPMS
- Internal high voltage SenseFET (QFET)
- World wide Input voltage
- Optimum Gate Driver
- Low Standby Power Consumption (Low start-up current & low operating current)
- Various Internal Protection Circuits
  - Over Voltage Protection (OVP) (Auto-restart)
  - Over Load Protection (OLP) (Auto-restart)
  - Over Current Latch (OCL) (Auto-restart)
  - Thermal Shutdown Protection (TSD) (Latch)
- Soft start

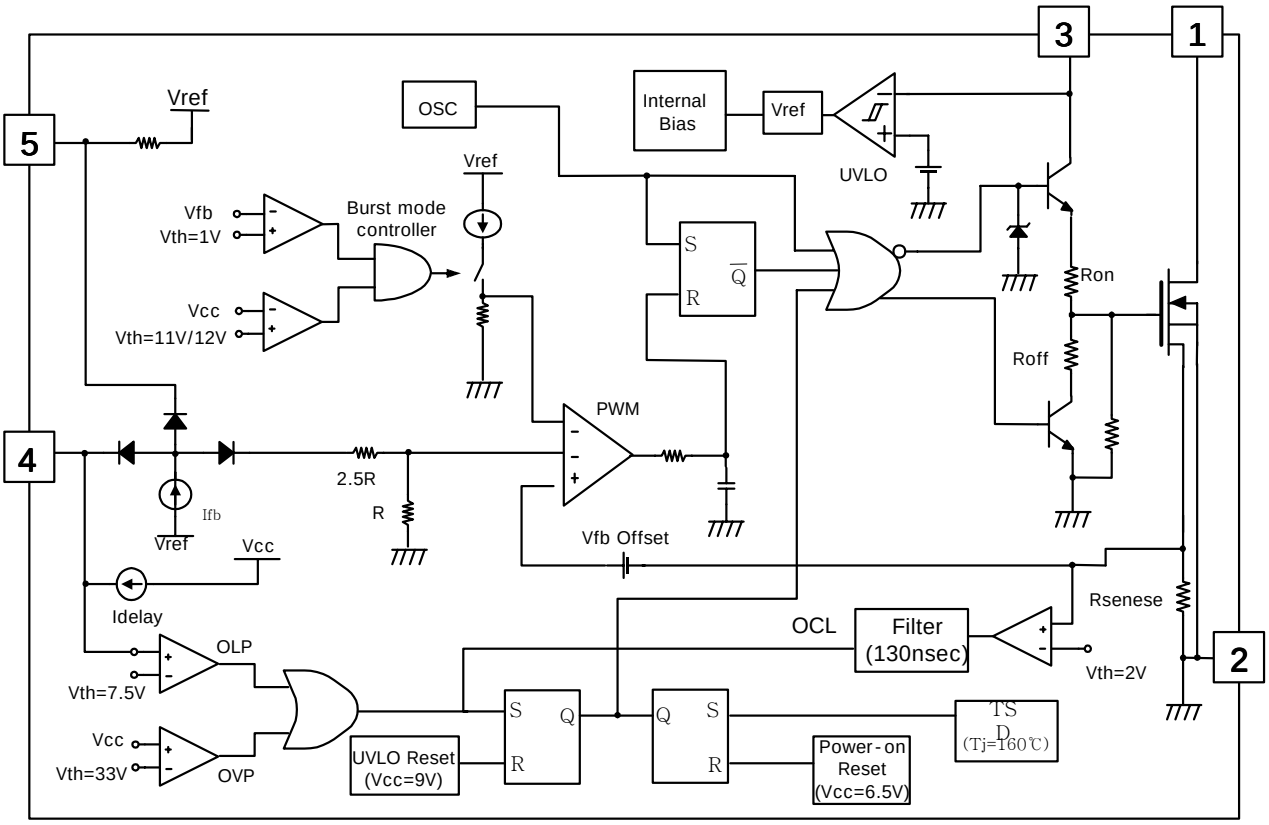


Figure 2-1. Internal Block Diagram

©2002 Fairchild Semiconductor Corporation

2.2 Starting Resistance Design And UVLO

Input voltage range: 80 ~ 265V (Ac)
At Minimum Input Voltage Va(dc), the starting resistance is

$$Va(dc) = 113V \ (Vp = 80\sqrt{2})$$
$$Rstart = 113 \div 200\mu A = 565K$$

and, at Maximum Input Voltage Va(dc), the power loss is

$$Va(dc) \cong 373V \qquad (Vp=265\sqrt{2})$$
$$P(loss) = \frac{Vac(dc)^2}{Rstart} = 0.246W$$
$$\text{Select: } Rstart = 565K\Omega \ /0.5W$$

At the minimum voltage, the starting resistance is set to ensure that the current through it is larger than the maximum start up current for the Fairchild Power Switch (170μA). The starting resistor produces a starting current, which charges the V_{CC} capacitor. The Fairchild Power Switch starts switching the internal SenseFET when the V_{CC} voltage becomes greater than 15V (the start voltage).
Once it starts to operate, the current drawn by the control IC suddenly increases to 10mA. The starting resistor cannot source this and consequently, the transformer auxiliary winding supplies most of the IC current after start up. The start time will be delayed if the V_{CC} capacitor is too large, so a moderate size capacitor should be used. Generally, 22~47μF capacitor values are considered good. This operation is described in Figure 2-2. V_{CC} only needs to be maintained above 9V after starting, but should be set so that OVP (Min. V_{CC} voltage above 30V) is not triggered. Approximately 24V is appropriate for the V_{CC} voltage.

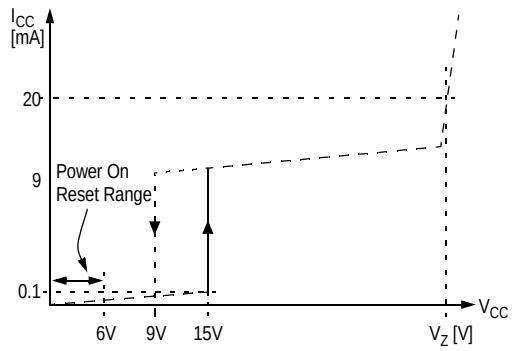


Figure 2-2. Start-up Waveform

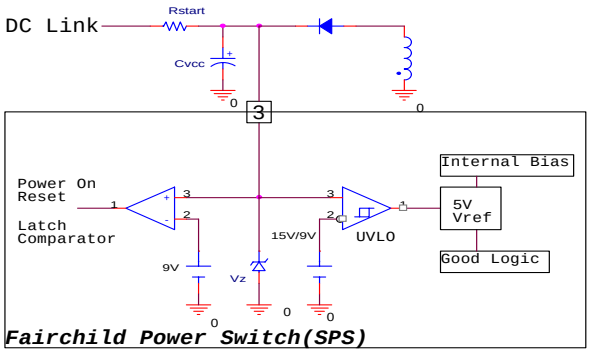


Figure 2-3. UVLO Block

2.3 Fairchlid Power Switch Protection Circuit

The Fairchild Power Switch has several self-protection circuits, which can be used without adding external components, thus providing system reliability without increasing cost.
Under auto restart mode, protection circuits become deactivated when V_{CC} falls below 9V (stop voltage), after which Fairchild Power Switch tries to restart. Under latch mode, protection circuits become deactivated only when V_{CC} falls to 6.5V (reset voltage), then Fairchild Power Switch tries to restart. When V_{CC} drops to 9V due to latch protection, the operating current of the IC drops from 10mA to 100μA. Therefore the V_{CC} capacitor starts to charge towards 15V through the starting resistor. For V_{CC} to fall to 6.5V (reset voltage), the input voltage must be removed.

2.3.1 Over Load Protection (OLP)

Overload as described here is different from a load short circuit. It is a condition where a load becomes greater than the preset level, though it is operating normally. Essentially, the overload protection circuit forces the Fairchild Power Switch to stop its operation if the load draws a higher current then the predetermined maximum value.
A problem associated with this type of protection circuit is that it can trigger erroneously on load transients. As a security measure, the Fairchild Power Switch triggers the protection circuit after a specific time delay. This avoids false triggering on short load transients. The above operations are executed as follows. Since the Fairchild Power Switch uses current mode control, maximum switch current is limited internally.
For a fixed input voltage, this limits the power. Therefore, if the power at the output exceeds this maximum, V_O shown in figure 2-4 becomes less than the set voltage, and the KA431(LM431) can draw only the allowed minimum current. As a result, the photo-transistor's current becomes zero. If all the current of the 0.9mA current source flows through the internal resistor (2.5R+R= 3.3K), Vfb becomes approximately 3V. At this time the 2μA current source starts to charge Cfb. Because the photo transistor's current is zero, Vfb continues to increase. The Fairchild Power Switch shuts down when Vfb reaches 7.5V. The shutdown delay time can be easily determined as the time required to increase the Cfb

©2002 Fairchild Semiconductor Corporation

by 4.5V (from 3V to 7.5V) using 2μA. When Cfb is 47nF, delay time is approximately 100ms. Fairchild Power Switch will not shut down within this time. Increasing Cfb to get a longer delay time can become a problem, because Cfb is an important parameter in determining the SMPS dynamic response time.

One method to delay the shutdown time is to add a resistor between the F/B pin and GND and to subtract the amount of the delay current. When the 4. 7MΩ resistor was used experimentally with Cfb of 47nF, shutdown time was almost doubled to 180~200ms. When Vfb voltage is 7.5V, the current flowing to the 4.7MΩ resistor is approximately 1.6μA.

To obtain the same results, a zener diode (approx. 3.9V) can be series connected to a capacitor (47nF) which can then be parallel connected to Cfb as shown in Figure 2.4.

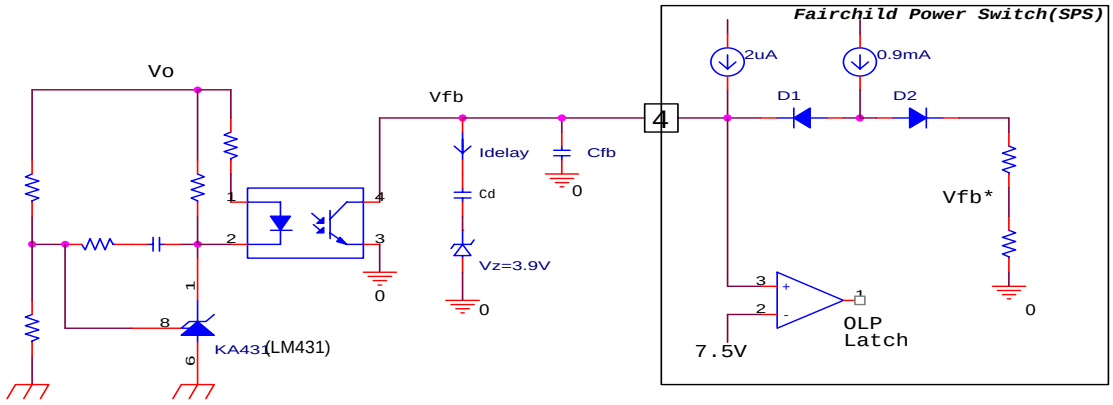


Figure 2-4. Fairchild Power Switch (FPS) Long Delayed Shutdown

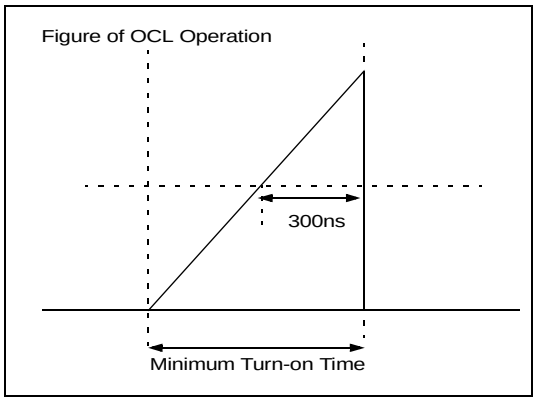
2.3.2 Over Voltage Protection

Fairchild Power Switch has self protection features that function even when abnormal states occur such as an open or short circuits in the feedback loop. When the feedback terminal shorts as viewed from the primary side, the feedback terminal voltage becomes zero and prevents switching from starting. If it opens, the protection circuit acts as an over voltage protection circuit. When there is an abnormal state or a possibility of opening due to improper soldering etc. in the secondary side feedback circuit, the primary side continues to switch using the maximum set current until the protection circuit starts to operate. In such instances, it is common for the secondary side voltage to become greater than the rated voltage, which can lead to a fuse blowing or, more seriously, a fire if a protection circuit is not in place. Even if this was not the case, ICs immediately connected to the secondary output without a regulator can be destroyed. Therefore, the Fairchild Power Switch employs the over voltage protection circuit to protect against feedback anomalies. The Fairchild Power Switch V_{CC} is proportional to the output voltage. When the Fairchild Power Switch V_{CC} exceeds 33V, the over voltage protection feature is triggered. Therefore, V_{CC} must be maintained at less than 30V during normal operation.

2.3.3 Over Current Protection (OCP).

The existing concept of Ipeak control does not go beyond limiting the amount of current during normal operation. The OCP block prevents damage to Fairchild Power Switch from abnormal states, such as a diode or a load short. A diode or a load short causes a large current to flow through the SenseFet for a short time. This can be tens of amperes. The leading edge blanking circuit sets the minimum turn on time at 600nS. Tens of amperes for 600nS could destroy the Fairchild Power Switch and so the OCL block senses this instantaneous current and latches like the existing protection circuit.

©2002 Fairchild Semiconductor Corporation



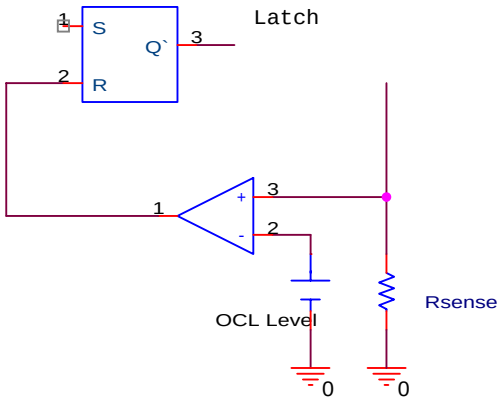


Figure 2-5. Over Current Latch (OCL)

3. Display Power Management Signalling (DPMS) Design Method

With high interest in power management recently, much effort has been concentrated in implementing the DPMS mode. The FS6S series uses burst mode for DPMS in order to achieve cost effectiveness and minimize the power consumption.

3.1 Burst Mode Operation

The FS6S-series has a particularly useful function for the DPMS mode: burst mode operation. Normally, customers use an auxiliary power system for DPMS in large monitors. This method can lower power consumption but increases costs. The FS6S-series can drop the output voltage with only minimal external components by using burst mode.
This reduces power loss in DPMS mode.
In the DPMS mode, Vfb is pulled low by the external micro-controller.

3.2 Implementation of the Burst Mode

The required circuit for implementing the burst mode is shown in Figure 4-1. Q1, D1, Rx, R5 and R6 are added to the secondary feedback network. During normal operation, Q1 is on, which isolates Rx from the feedback network.
Vo2 is sensed and the amplified error is transferred to the primary side through the photo coupler. By turning off Q1, Rx is connected to the feedback network.
The error amplifier increases the current through the photo coupler, and thus Vfb of the FS6S-series drops to zero. Therefore no additional opto coupler is required to switch into burst mode. Rx can be calculated by the following equation when KA431(LM431) is used as an error amp.

$$Rx < \frac{R7 \times R8(Vol - 2.5 - V_{D1})}{2.5(R7 + R8) - R8 \cdot Vo2}$$

where Vo1 and Vo2 are the reduced voltages in burst mode.

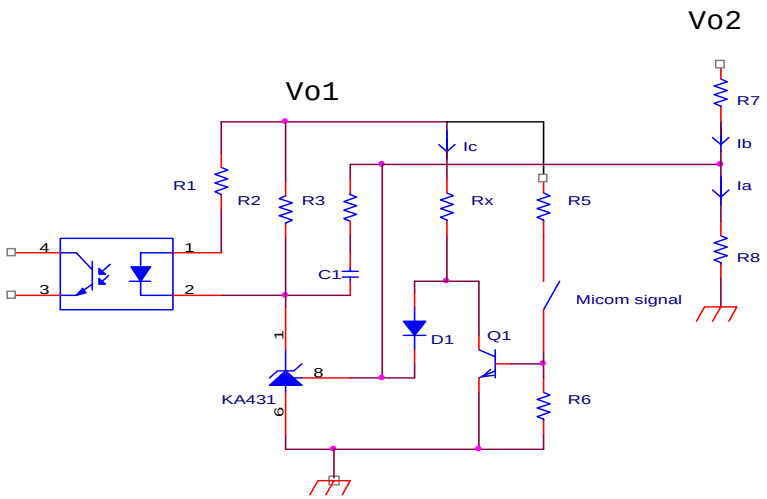


Figure 3-1. Rx Setting circuit for Burst mode operation

©2002 Fairchild Semiconductor Corporation

3.3 Experiment of the Burst mode operation

3.3.1 Vcc/Vds/ Vregin/Vregout waveform at the Burst Mode operation

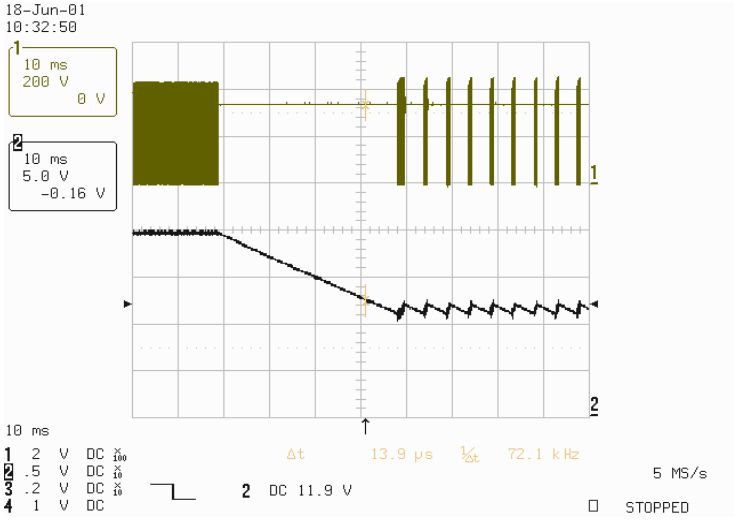


Figure 3-2. Vcc / Vds at the Burst mode operation

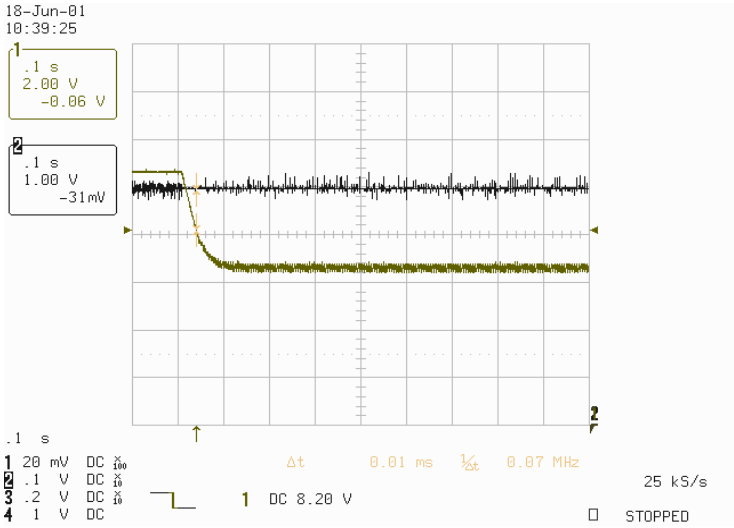


Figure 3-3. Vregin / Vregout at the Burst mode operation

Experimental results are shown in, Figure 4-2 and Figure 4-3. With minimum load and normal operation: Vac = 240V, Pin = 4.82W, V_{CC} = 18V, Vo = 12.24V. When Fairchild Power Switch operates Burst Mode: Pin = 2.72W, V_{CC} = 11~12V, Vo = 6.7V.

©2002 Fairchild Semiconductor Corporation

4. Application for the LCD Monitor

4.1 Flyback converter demo circuit for LCD Monitor

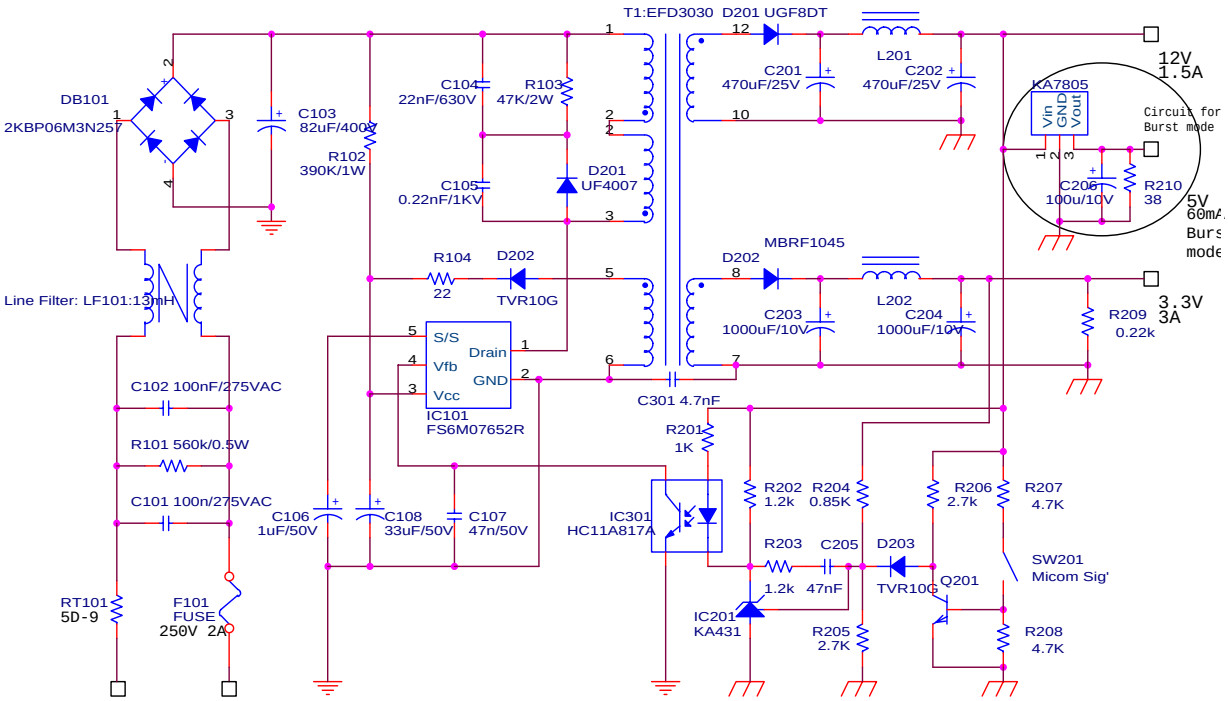


Figure 4-1. Fairchild Power Switch (FPS) Flyback Converter DEMO BOARD for the LCD Monitor

©2002 Fairchild Semiconductor Corporation

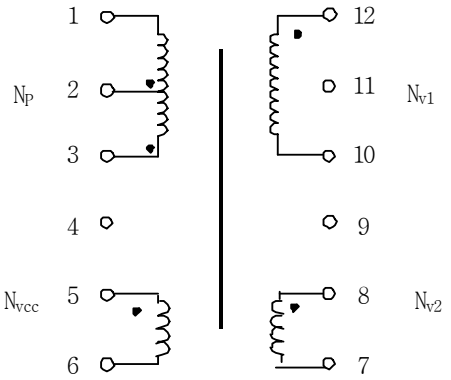
4.2 Part List for Fairchild Power Switch (FPS) Flyback Converter DEMO BOARD for the LCD Monitor

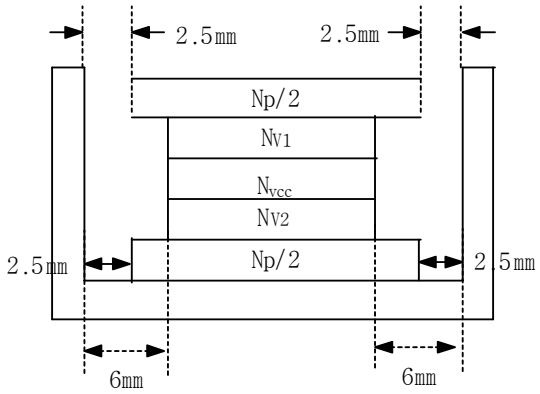
Part	Value	Note	Part	Value	Note
Fuse			C204	1000μF 10V	Electrolytic Capacitor
F101	250V/2A	-	C205	47nF 50V	Electrolytic Capacitor
NTC			C206	100μF 10V	Electrolytic Capacitor
RT101	5D-9	-	C301	4.7nF	Polyester Film Cap
Resistor			-	-	-
R101	560K	1/2W	-	-	-
R102	390K	1W	-	-	-
R103	47K	2W	-	-	-
R104	22	1/4W	-	-	-
R201	1K	1/4W	**Diode**		
R202	1.2K	1/4W	D101	UF4007	-
R203	1.2K	1/4W	D102	TVR10G	-
R204	0.9K	1/4W	D201	UGF8DT	-
R205	2.7K	1/4W	D202	MBRF1045	-
R206	2.7K	1/4W	D203	TVR10G	-
R207	4.7K	1/4W	-	-	-
R208	4.7K	1/4W	-	-	-
R209	0.22K	1/4W	-	-	-
R210	38	1/4W	**Bridge Diode**		
Capacitor			BD1	2KBP06M 3N257	-
C101	100nF 275VAC	Box Capacitor	**Inductor**		
C102	100nF 275VAC	Box Capacitor	L201 L202	5μH 6μH	-
C103	82μF 400V	Electrolytic Capacitor Film Capacitor			-
C104	22nF 630V		**Line Filter**		
C105	0.22nF 1KV	Ceramic Capacitor	LF101	13mH	-
C106	1μF 50V	Electrolytic Capacitor	**IC**		
C107	47nF 50V	Electrolytic Capacitor	IC101	FS6S07652RT	FPSFPS(2A 650V): Fairchild
C108	33μF 50V	Electrolytic Capacitor	IC201	KA431 (LM431)	Voltage reference Fairchild
-	-	-	IC202	KA7805	Voltage regulator Fairchild
-	-	-	IC301	HC11A817A	Photo Coupler/QT
C201	470μF 25V	Electrolytic Capacitor	Q201	KSC945	Transistor Fairchild
C202	470μF 25V	Electrolytic Capacitor	-	-	-
C203	1000μF 10V	Electrolytic Capacitor	-	-	-

©2002 Fairchild Semiconductor Corporation

4.3 Transformer Specification

1. SCHEMATIC DIAGRAM. (TOP VIEW)





* REMOVED PIN NO. : #4
* THE '●' MARKS ARE START POINT.

2. WINDING SPECIFICATION

NO.	PIN(S → F)	WIRE	TURNS	WINDING METHOD
Np/2	2 → 1	0.3φ× 1	40	SOLENOID WINDING
INSULATION : POLYESTER TAPE t=0.050mm, 2Layer				
Nv2	8 → 7	0.3φ× 4	4	CENTER WINDING
INSULATION : POLYESTER TAPE t=0.050mm, 2Layers				
Nvcc	5 → 6	0.2φ× 1	24	CENTER WINDING
INSULATION : POLYESTER TAPE t=0.050mm, 2Layers				
Nv1	12 → 10	0.3φ× 2	13	CENTER WINDING
INSULATION : POLYESTER TAPE t=0.050mm, 2Layers				
Np/2	3 → 2	0.3φ× 1	40	SOLENOID WINDING
OUTER INSULATION : POLYESTER TAPE t=0.050mm, 2Layers				

3. ELECTICAL CHARACTERISTIC

CLOSURE	PIN	SPEC.	REMARKS
INDUCTANCE	1 - 3	650uH ± 10%	100KHz, 1V
LEAKAGE L	1 - 3	10uH MAX.	2nd ALL SHORT

4. CORE & BOBBIN

CORE : EFD3030
BOBBIN : EFD3030

Figure 4-2. FS6M07652RT Transformer Spec for LCD Monitor

©2002 Fairchild Semiconductor Corporation

5. Example Transformer Design for a Monitor SMPS

When designing the transformer for a LCD monitor SMPS several parameters should be taken into account. Input and output voltages will determine the windings. Consideration should be given to the switching frequency range, continuous and discontinuous current modes and core size. A typical design sequence is as follows:

5-1. Determine System Specifications:

Output Power, P_O = 30W (at 12 and 3.3V) Vac input range = 85 to 265Vac (universal input), 60Hz
Efficiency $\eta \geq 70\%$

5-2. Determine Minimum Dc Input Voltage (V_{min}), Primary Peak Current (I_{peak}) And Primary Rms Current (I_{rms}).

When the SMPS operates at the same output power for all ac inputs, the maximum peak drain current occurs at the minimum input voltage (V_{min}). Also, V_{min} will exhibit the largest ripple voltage (ΔV) at that time. The dc link capacitor C_{in} is charged and discharged at 120Hz (Figure 5-1).

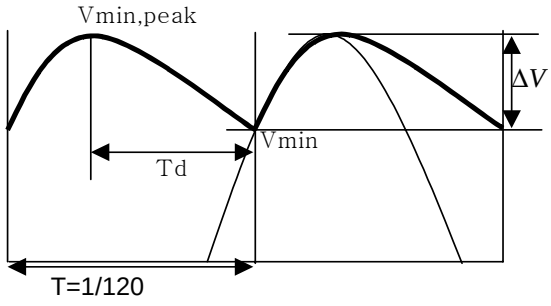


Figure 5-1. If power output stays constant as the ac input varies, peak current drain will occur at V_{min}. Also, the largest ripple on V_{min} occurs at this point; dc link capacitor C_{in} charges/discharges at 120Hz.

a. Calculate energy discharge time, T_d:

$$Td = \frac{1}{fs} \times \frac{1}{4} \times \left(1 + \frac{\arcsin \frac{Vmin}{Vmin,peak}}{\frac{\pi}{2}} \right)$$

b. Calculate dc link capacitor, C_{in}:

$$Win = Pin \times Td \left(\begin{matrix} Win = \text{input energy during discharge} \\ Pin = \text{input power} \end{matrix} \right.$$

$$Win = \frac{1}{2} \cdot Cin \cdot (V^2 min,peak - V^2 min)$$

c. For this charger:

$$Td = 6.78ms (V_{min},peak = 85\sqrt{2}, V_{min} = 85\sqrt{2} - 20)$$

$$Win = \frac{Pout}{\eta} \cdot Td = \frac{30}{0.7} \times 6.78ms = 0.29J$$

d. Assume 20Vac of ripple, from which:

$$Cin = \frac{2Win}{V^2 min,peak - V^2 min}$$

$$= \frac{2 \times 0.29}{(\sqrt{2} \times 85)^2 - (\sqrt{2} \times 85 - 20)^2} = 132\mu F$$

However, 132µF is not a standard value of capacitor. Hence, to calculate the true V_{min}, select the nearest standard value for C_{in} (82µF) and substitute it above, solving for V_{min} = 86V.

e. Primary current reaches its I_{peak} value at V_{min} and maximum duty (D_{max}). Also in most current mode SMPSs, D_{max} should be kept below 50% to eliminate any possibility of sub harmonic instabilities.

$$I_{peak} = \frac{2 \times P_o}{\eta \times V_{min} \times D_{max}} = \frac{2 \times 30}{0.7 \times 86 \times 0.45} \cong 2.2A$$

Primary I_{rms} can be derived from I_{peak} :

$$I_{rms} = I_{peak} \times \sqrt{\frac{D_{max}}{3}} = 2.2 \times \sqrt{\frac{0.45}{3}} = 0.85A$$

5-3. Determine Primary Inductance, Lp :

This is the primary inductance needed to transfer the required power from primary to secondary.

$$L_P = \frac{D_{max} \times V_{min}}{\Delta I \times f_s} = \frac{0.45 \times 86}{0.85 \times 70 \times 10^3} = 650\mu H$$

It is recommended to select the minimum synchronous frequency as the switching frequency, f_s, of the monitor application.

5-4. Determine Core Size:

The core used must be able to store the required peak energy in a small gap without saturation and with acceptable core losses. The following equation is commonly used to ensure proper core size (area product) in a saturation limited case.

$$AP = A_e \cdot A_w = \left[\frac{L_p \cdot I_p \cdot I_{rms} \cdot 10^8}{420 \cdot K \cdot B_m} \right]^{1.31} cm^2$$

where, A_w = magnetic window area, cm^2
A_e = magnetic cross section area, cm^2
K = core utilization factor, 0.2
B_m = maximum flux density, Teasel; therefore,

$$AP = \left(\frac{650 \times 10^{-6} \times 1.52 \times 0.85 \times 10^4}{420 \times 0.2 \times 0.1} \right)^{1.31} = 2.47 cm^2$$

©2002 Fairchild Semiconductor Corporation

From the catalog data, select the smallest ferrite core available with an area product, AP, that exceeds the calculated value. The specifications of the selected core, EFD3030 are AP = 2.47 cm^2
A_w = 2.23cm^2,
A_e = 1.07cm^2

5-5. Determine Primary Turns, N_P:

$$Ton(max) = \frac{1}{fs} \times D_{max}$$
$$= \frac{1}{70 \times 10^3} \times 0.45$$
$$= 6.43\mu S$$

From Faraday's law, the minimum number of primary turns can be expressed as

$$N_{P(min)} = \frac{V_{min} \times T_{on(max)}}{\Delta B_m \times A_e} = \frac{86 \times 6.43 \times 10^{-6}}{0.1 \times 69 \times 10^{-6}} = 80[turns]$$

where, $T_{on(max)}$ is maximum turn on time, and ΔB_m is maximum peak to peak flux density swing

5-6. Determine Secondary Turns, N_S:

Using the Volt-seconds equation, the turns ratio n = N_p/N_s can be calculated at maximum duty ratio, as

$$n = \frac{V_{min} \times Duty_{max}}{(V_o + V_d) \times (1 - Duty_{max})} = 6$$

where, V_o = output voltage, and V_d = diode forward voltage drop; hence,

$$N_s = \frac{N_p}{n} = \frac{80}{6} = 13[turns]$$

5-7. Determine Bias Turns, N_b, And Auxiliary Turns, N_a:

Secondary side calculation in volts per turn units is

$$Secondary\ Volt/turn = \frac{V_s}{N_s} = \frac{12}{13} = 1[V/turn]$$

The bias side must have same volts-per turn value as the secondary side and so can be calculated as

$$N_b = \frac{V_b}{V/N} = \frac{24}{1} = 24[turns]$$

Auxiliary turns are calculated using the same volts per unit.

Author: FAIRCHILD Wonsob Lee
Experience: Participated in the development of Fairchild Power Switch(FPS) in 1998.
Presently, responsible for the development and application of IC for the monitor.
E-mail: sobi@fairchildsemi.co.kr
Tel: 82-32-680-1834
Fax: 82-32-680-1317

©2002 Fairchild Semiconductor Corporation

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2002 Fairchild Semiconductor Corporation