WM9001

1W Dual-Mode Class AB/D Speaker Driver

DESCRIPTION

The WM9001 is a powerful, high quality speaker driver which can operate in class D or AB mode, providing total flexibility to the system designer. Low leakage, high PSRR and pop/click suppression enable direct battery connection to the speaker supply. RF noise suppression techniques and differential design are used to suppress undesired noise. A single-ended input option has been included for complete system flexibility.

The device is enabled by setting a logic '1' on the EN pin. The class D clock can be generated by an internal oscillator, or supplied from an external clock source.

Flexible speaker boost options (requiring no additional components) allow output volume to be maximised for various SPKVDD/AVDD combinations while minimising internal power consumption.

The WM9001 is available in a 3x3mm QFN package, ideal for portable systems such as mobile phones, portable navigation devices, media players, laptop computers and electronic dictionaries.

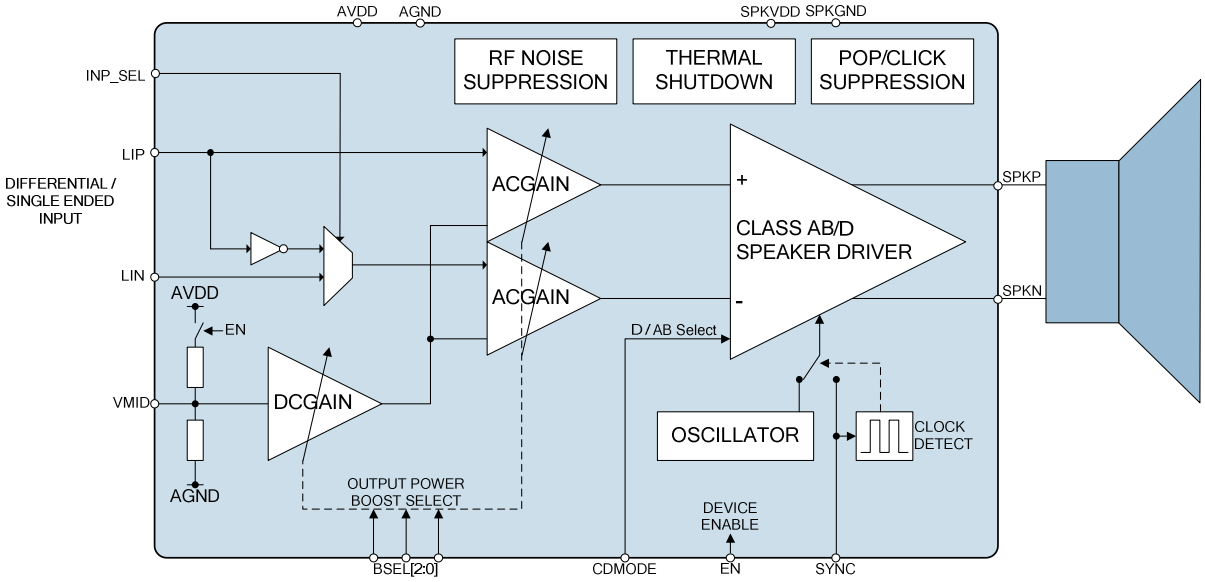
FEATURES

- Class D and AB speaker driver modes for flexibility
- Speaker driver provides 1W into 8Ω at <0.1% THD
- SNR 102dB (Class AB), 97dB (Class D)
- Differential and single-ended input modes
- >80dB PSRR @ 217Hz (SPKVDD)
- <1µA typical leakage with direct battery connection
- Filterless speaker connection
- Fully differential architecture (differential mode)
- Pop/click suppression
- RF noise suppression
- Fully compatible with Wolfson CODECs including WM8990 / WM8991
- Internal oscillator or external clock source
- Thermal shutdown protection
- 3x3mm QFN package

APPLICATIONS

- Mobile phones
- Portable navigation devices
- Portable media players
- Laptop computers and portable gaming devices
- Electronic dictionaries
- General-purpose high quality speaker amplifier

BLOCK DIAGRAM



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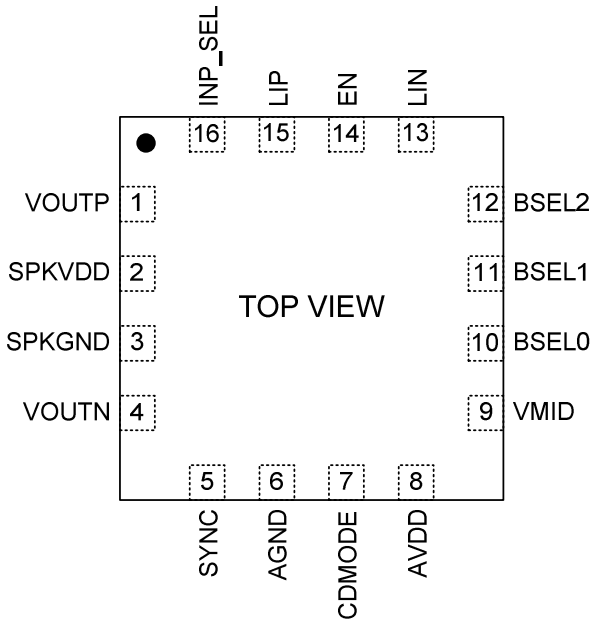
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PIN CONFIGURATION

The WM9001 is supplied in a 3mm x 3mm 16 pin QFN package

QFN



ORDERING INFORMATION

DEVICE	MINIMUM ORDER QUANTITY	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
QFN WM9001GEFL	164	-40°C to 85°C	QFN	MSL 1	260°C
QFN WM9001GEFL/R	3500	-40°C to 85°C	QFN	MSL 1	260°C

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
16	INP_SEL	Digital Input	Audio Input Mode Select
15	LIP	Analogue Input	Positive differential input
14	EN	Enable	Device Enable input
13	LIN	Analogue Input	Negative differential input
12	BSEL2	Digital Input	Signal Boost Control[2]
11	BSEL1	Digital Input	Signal Boost Control[1]
10	BSEL0	Digital Input	Signal Boost Control[0]
9	VMID	Analogue Output	Midrail voltage decoupling capacitor
8	AVDD	Supply	Analogue supply
7	CDMODE	Digital In	Class AB/D Mode select
6	AGND	Supply	Analogue supply ground
5	SYNC	Digital Input	Class D clock input
4	VOUTN	Analogue Output	Speaker negative output
3	SPKGND	Supply	Speaker driver supply ground
2	SPKVDD	Supply	Speaker driver supply
1	VOUTP	Analogue Output	Speaker positive output

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD	-0.3V	+4.5V
SPKVDD	-0.3V	+7V
Digital Inputs voltage range	AGND -0.3V	AVDD +0.3V
Analogue Inputs voltage range	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analogue supply	AVDD	2.7		3.6	V
Speaker supply	SPKVDD	2.7		5.5	V
Ground	AGND, SPKGND		0		V

Notes:

1. Analogue and speaker grounds must always be within 0.3V of each other.
2. All supplies are completely independent from each other (i.e. not internally connected).
3. AVDD must be less than or equal to SPKVDD.
4. SPKVDD must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is AVDD*(DCGAIN+ACGAIN)/2.
5. The EN and SYNC pins are compatible with low voltage (eg. 1.8v) logic levels from external devices, and can accept logic 1 digital inputs as low as 1.6V, even though the WM9001 AVDD supply minimum is 2.7V. This provides compatibility with a low voltage DVDD on a controlling device such as the WM8991 CODEC.

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM9001 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND pins/paddle through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package pins/paddle/balls to PCB (conduction).

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		100	°C
Thermal Resistance	Θ_{JA}		52		°C/W

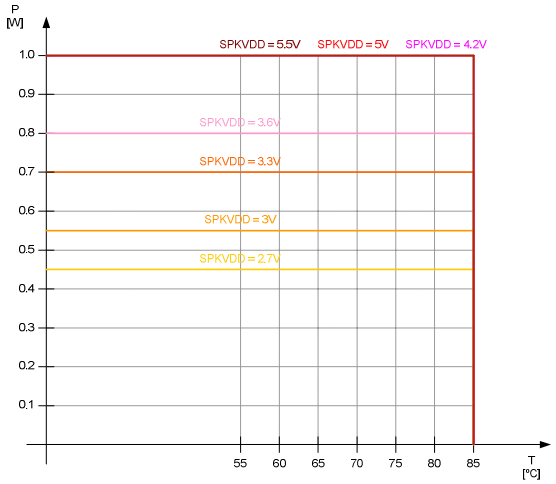
POWER DE-RATING

The speaker driver has been designed to drive a maximum of 1W into 8Ω with a 5V supply. However, thermal restrictions defined by the package Θ_{JA} limit the amount of power that can be safely dissipated in the device without exceeding the maximum operating junction temperature. Power dissipated in the device correlates directly with speaker efficiency, hence there are separate de-rating curves for class D and class AB operation.

Under no circumstances should the recommended maximum powers be exceeded.

The de-rating curves in Figure 1 are based on a sinusoidal input signal delivering a maximum output power of 1W into 8Ω.

CLASS D



CLASS AB

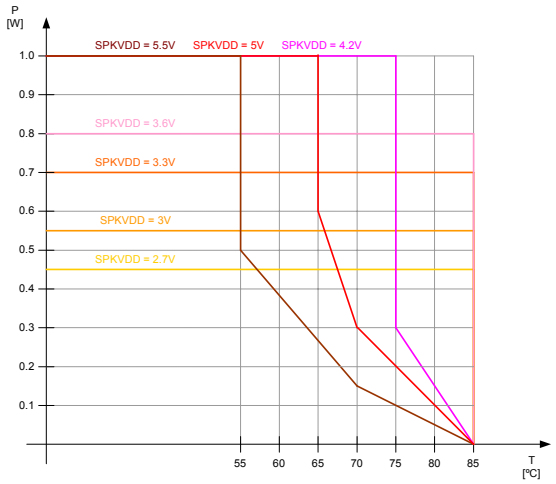


Figure 1 Speaker Power De-Rating Curves

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 3.3V; SPKVDD = 5V, T_A = +25°C, 1kHz input signal, BSEL[2:0] = 000 unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pins (LIN, LIP)					
Maximum Full-Scale Input Signal Level Differential Mode (INP_SEL=0): This is the maximum on each input pin; the total differential input is 2x this figure. Single-Ended Mode (INP_SEL=1): This is the maximum on LIP. Note that the maximum signal level scales in proportion to AVDD (AVDD/3.3).			1.0 0		Vrms dBV
Input Resistance – Differential Mode (INP_SEL=0)	Gain=0dB (BSEL[2:0]=000)		160		kΩ
	Gain=2.1dB (BSEL[2:0]=001)		123		kΩ
	Gain=2.9dB (BSEL[2:0]=010)		112		kΩ
	Gain=3.6dB (BSEL[2:0]=011)		103		kΩ
	Gain=4.5dB (BSEL[2:0]=100)		94		kΩ
	Gain=5.1dB (BSEL[2:0]=101)		87		kΩ
Input Resistance – Single-Ended Mode (INP_SEL=1)	All gain settings		20		kΩ
Input Capacitance			10		pF
Speaker Driver Performance					
SNR (A-weighted)	BSEL[2:0] = 011 (1.52x) 8Ω Bridge Tied Load Class D Mode Differential and Single-Ended Input Modes	90	97		dB
THD (P_O=0.5W)			-92	-81	dB
THD+N (P_O=0.5W)			-87	-79	dB
THD (P_O=1.0W)			-83	-73	dB
THD+N (P_O=1.0W)			-78	-68	dB
SNR (A-weighted)	BSEL[2:0] = 011 (1.52x) 8Ω Bridge Tied Load Class AB Mode Differential and Single-Ended Input Modes	94	102		dB
THD (P_O=0.5W)			-79	-70	dB
THD+N (P_O=0.5W)			-77	-68	dB
THD (P_O=1.0W)			-77	-70	dB
THD+N (P_O=1.0W)			-75	-68	dB
Mute Attenuation	Device disabled (EN=0)		100		dB
Common Mode Rejection Ratio	Differential Mode		50		dB
Bandwidth		0		22	kHz
AVDD PSRR	100mV pk-pk ripple, 217Hz		60		dB
SPKVDD PSRR			83		dB
DC Offset at load			5		mV
SPKVDD Leakage Current	EN=0		0.3		µA
AVDD Leakage Current	EN=0		9		µA
Reference Levels					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V
Output Common Mode Voltage (Note: BSEL[2:0]=110 and BSEL[2:0]=111 are reserved settings)	BSEL[2:0] = 000		1.00 x VMID		V
	BSEL[2:0] = 001		1.27 x VMID		
	BSEL[2:0] = 010		1.40 x VMID		
	BSEL[2:0] = 011		1.52 x VMID		
	BSEL[2:0] = 100		1.67 x VMID		
	BSEL[2:0] = 101		1.80 x VMID		

Test Conditions

AVDD = 3.3V; SPKVDD = 5V, T_A = +25°C, 1kHz input signal, BSEL[2:0] = 000 unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input / Output (for hardware control)					
Input HIGH Level (BSEL, CDMODE)		0.7×AVDD			V
Input HIGH Level (EN, SYNC)		1.6			V
Input LOW Level				0.3×AVDD	V
Input capacitance			10		pF
Input leakage		-0.9		0.9	uA
Oscillator					
Free-running oscillator frequency		600	800	950	kHz
External clock frequency range		600	800	950	kHz
Power-Up Time (Based on recommended Vmid capacitor value; these times will vary with different capacitors)					
Class AB Enable time	Vmid capacitor = 4.7µF		400		ms
Class D Enable time	Vmid capacitor = 4.7µF		100		ms

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

TYPICAL POWER CONSUMPTION

MODE	GAIN	EN	CDMODE	SYNC	INP_SEL	AVDD		SPKVDD		TOTAL
BATTERY LEAKAGE						(V)	(uA)	(V)	(uA)	(uW)
OFF	0dB	0	0	0	0	0	0	2.7	0.02	0.054
EN=0, AVDD=0V	0dB	0	0	0	0	0	0	3.7	0.06	0.222
	0dB	0	0	0	0	0	0	4.2	0.11	0.462
	0dB	0	0	0	0	0	0	5	0.14	0.7
	0dB	0	0	0	0	0	0	5.5	0.17	0.935
STANDBY LEAKAGE						(V)	(uA)	(V)	(uA)	(uW)
OFF Standby	0dB	0	0	0	0	2.7	7.67	2.7	0.02	20.763
EN=0, AVDD enabled	2.1dB	0	0	0	0	3	8.16	3.7	0.07	24.739
	2.1dB	0	0	0	0	3.3	8.91	4.2	0.1	29.823
	3.6dB	0	0	0	0	3.3	8.93	5	0.37	31.319
	3.6dB	0	0	0	0	3.6	9.75	5.5	0.64	38.62
QUIESCENT						(V)	(mA)	(V)	(mA)	(mW)
Class AB Speaker Mode	0dB	1	1	0	0	2.7	0.3	2.7	3.45	10.12
8Ω	2.1dB	1	1	0	0	3	0.33	3.7	4.69	18.35
	2.1dB	1	1	0	0	3.3	0.35	4.2	5.6	24.71
	3.6dB	1	1	0	0	3.3	0.35	5	6.37	33
	3.6dB	1	1	0	0	3.6	0.38	5.5	7.42	42.16
Class D Speaker Mode	0dB	1	0	0	0	2.7	1.09	2.7	1.08	5.84
8Ω	2.1dB	1	0	0	0	3	1.22	3.7	1.52	9.3
Internal Oscillator	2.1dB	1	0	0	0	3.3	1.36	4.2	1.8	12.06
	3.6dB	1	0	0	0	3.3	1.36	5	2.15	15.23
	3.6dB	1	0	0	0	3.6	1.5	5.5	2.42	18.74
Class D Speaker Mode	0dB	1	0	800kHz	0	2.7	1.08	2.7	1.13	5.97
8Ω	2.1dB	1	0	800kHz	0	3	1.23	3.7	1.54	9.4
External Oscillator	2.1dB	1	0	800kHz	0	3.3	1.37	4.2	1.76	11.91
	3.6dB	1	0	800kHz	0	3.3	1.37	5	2.19	15.45
	3.6dB	1	0	800kHz	0	3.6	1.52	5.5	2.47	19.06
ACTIVE						(V)	(mA)	(V)	(mA)	(mW)
Class AB Speaker Mode 0.45W into 8Ω	3.6dB	1	1	0	0	3.3	0.35	5	211.63	1059.3
Class AB Speaker Mode 0.2W into 8Ω	3.6dB	1	1	0	0	3.3	0.35	5	144.22	722.26
Class D Speaker Mode 1W into 8Ω	3.6dB	1	0	0	0	3.3	1.34	5	235.15	1180.18
Class D Speaker Mode 0.5W into 8Ω	3.6dB	1	0	0	0	3.3	1.36	5	120.45	606.73

Note that the Gain settings are determined by the BSEL[2:0] values as follows:

Gain (dB)	Gain (v)	BSEL[2]	BSEL[1]	BSEL[0]
0dB	1.00x	0	0	0
2.1dB	1.27x	0	0	1
2.9dB	1.40x	0	1	0
3.6dB	1.52x	0	1	1
4.5dB	1.67x	1	0	0
5.1dB	1.80x	1	0	1

SPEAKER DRIVER PERFORMANCE

The THD+N performance of the Speaker Driver is shown below for Class AB mode and for Class D mode.

Load R_L = 8Ω + 22μH, Frequency = 1kHz.

Data is provided for four typical Power Supply /Gain combinations:

AVDD	SPKVDD	GAIN
2.7V	2.7V	0 dB (x1.0)
3.0V	3.7V	2.1 dB (x1.27)
3.3V	4.2V	2.1 dB (x1.27)
3.3V	5.0V	3.6 dB (x1.52)

CLASS D MODE

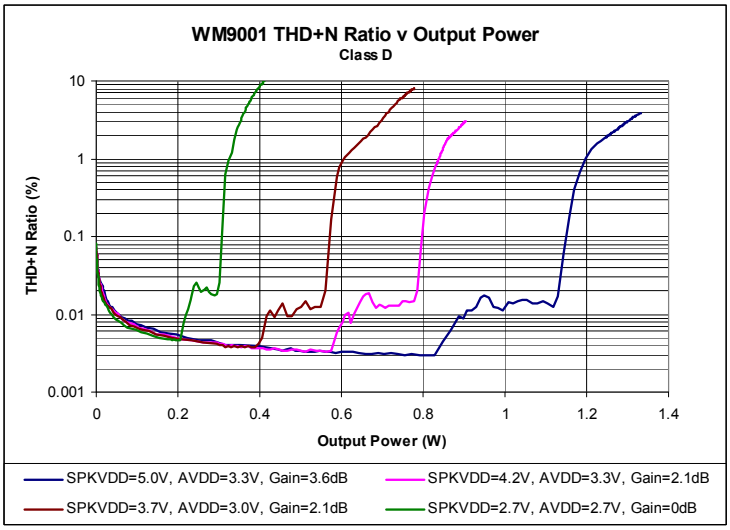


Figure 2 Class D Speaker Performance

CLASS AB MODE

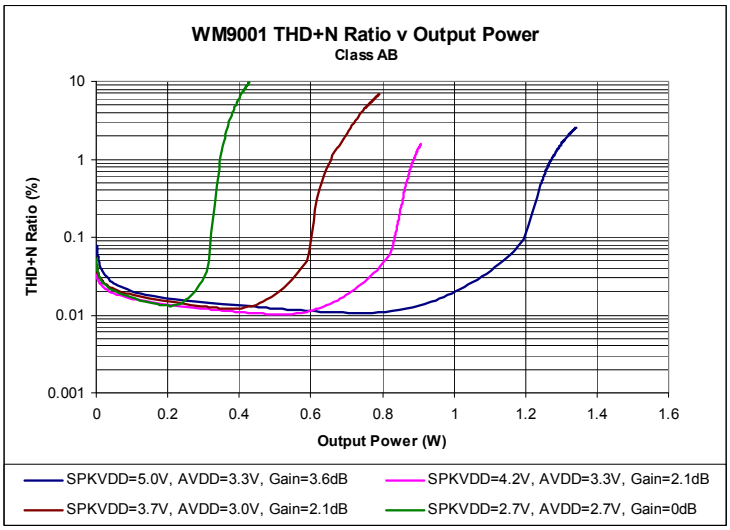
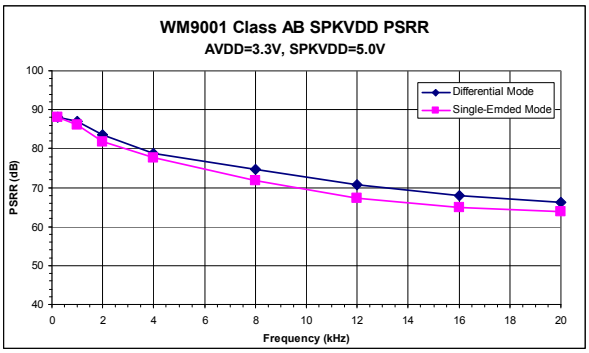


Figure 3 Class AB Speaker Performance

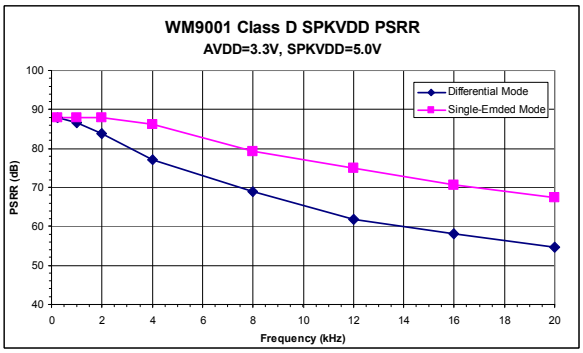
PSRR PERFORMANCE

Typical PSRR versus frequency curves are provided below. The curves were produced by superimposing a 100mV pk-pk ripple onto a DC level at the supply pin and measuring rejection of this signal at the output.

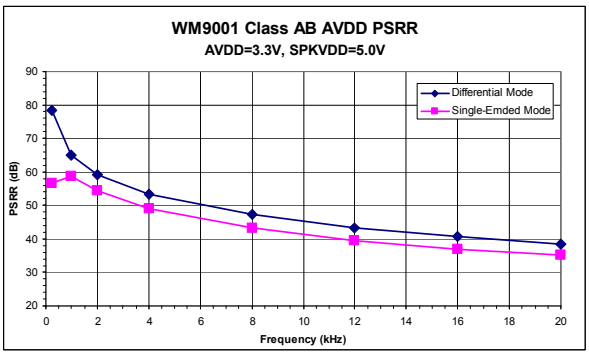
CLASS AB SPKVDD PSRR



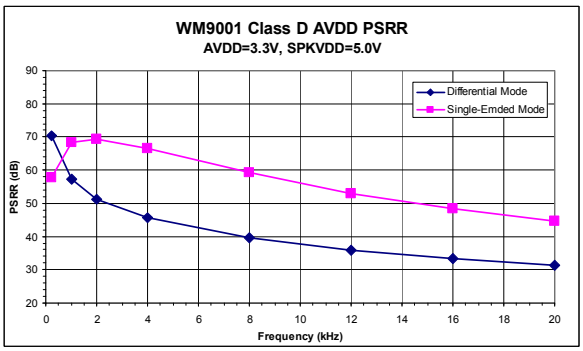
CLASS D SPKVDD PSRR



CLASS AB AVDD PSRR



CLASS D AVDD PSRR



Note: The measurement noise floor is at approximately 88dB

EFFICIENCY

Typical Efficiency versus output power curves are provided below for both class AB and class D modes.

CLASS AB



CLASS D



AUDIO SIGNAL PATHS

The WM9001 speaker driver can operate in two modes:

1. INP_SEL=0: Takes a differential audio input and produces a differential class AB or class D output. The audio signal path is illustrated below.

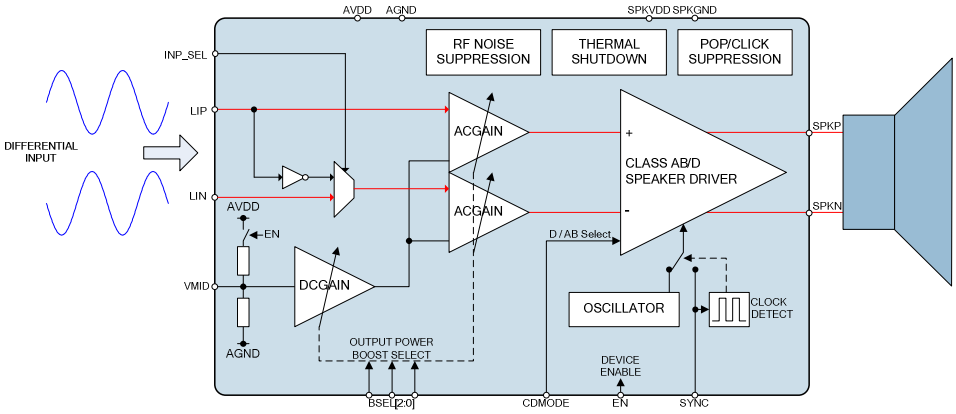


Figure 4 Differential Mode Audio Signal Paths

2. INP_SEL=1: Takes a single-ended audio input and produces a differential class AB or class D output. The audio signal path is illustrated below.

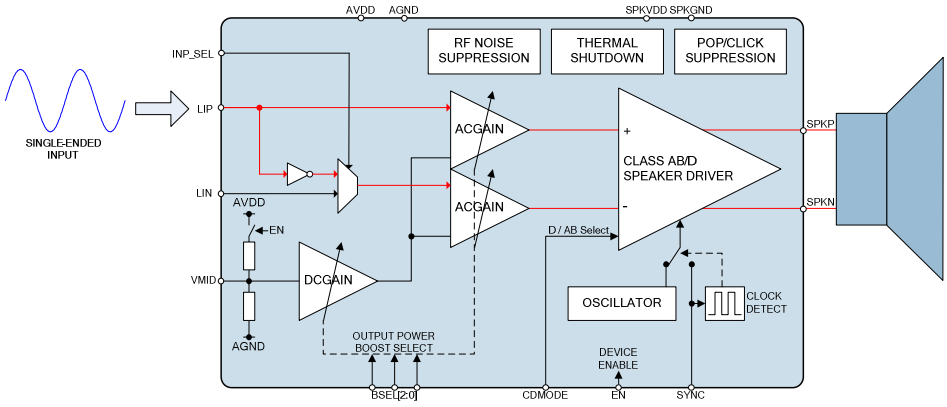


Figure 5 Single-Ended Mode Audio Signal Paths

DEVICE DESCRIPTION

INTRODUCTION

The WM9001 is a powerful mono speaker driver, which can operate in class D or AB mode, providing total flexibility to the system designer. The WM9001 can deliver 1W in class D mode, Figure 2 , or in class AB mode, Figure 3, into an 8Ω load. The input can be configured either as a single channel differential line output offering good noise rejection characteristics, or as a single-ended line output for systems where there is no differential option.

It can be used as a stand-alone device, or in conjunction with a CODEC such as the WM8991 or WM8990 to provide a complete stereo solution. The gain settings and speaker driver mode are configurable via the hardware control pins BSEL[2:0] and CDMODE. For stand-alone operation these pins are tied to logic 1/0.

The class D amplifier requires a clock signal. An internal oscillator can be used for stand alone operation by tying the SYNC pin to logic 1/0. Alternatively an external clock can be used by applying this signal to the SYNC pin. The EN (Enable) pin provides a controllable method for switching ON/OFF the speaker outputs.

The very small 3 x 3mm QFN packages make the WM9001 ideal for portable systems, such as mobile phones, portable navigation devices, media players, laptop computers and electronic dictionaries.

POWER ON RESET

The WM9001 includes an internal Power-On Reset (POR) circuit which is used to reset the device into a default state at power up. The POR circuit is controlled by the AVDD power supply. Note that there is no POR on the SPKVDD supply.

When the chip is powered down, the speaker driver outputs, SPKP and SPKN, become tri-state.

ENABLE

The chip is enabled by a logic '1' on the EN pin.

PIN	NAME	DESCRIPTION
14	EN	Device Enable input 0 = Device Disabled 1 = Device Enabled

Table 1 Device Enable Control

The EN pin should be used to disable the device prior to removing the audio or clock (removing an external clock will not disable the output). When the chip is disabled, the speaker driver outputs become tri-state.

The EN pin is compatible with low voltage (eg. 1.8v) logic levels from external devices, and can accept logic 1 digital inputs as low as 1.6V, even though the WM9001 AVDD supply minimum is 2.7V. This provides compatibility with a low voltage DVDD on a controlling device such as the WM8991 CODEC.

Ultra low quiescent current in the disabled state minimises extends battery life in this condition. The typical values of SPKVDD current and AVDD current in the disabled (Standby) state are described in the Electrical Characteristics section.

INPUT SIGNAL PATH

The line inputs to the WM9001 are identified as LIP and LIN on the pin diagram. These are a fully balanced differential input pair, with matched impedances on both terminals. The input stage of the WM9001 is driven by the voltage difference between these two pins. This results in a very low noise amplifier stage, as any common mode noise (unwanted signals that are present in equal amplitude on both pins) are cancelled out at the input and are not reproduced at the output.

The LIP input can also be configured as a single-ended line input – see Table 2 below. Single-ended to differential conversion is carried out internally with the N channel input (normally LIN) connected to an inverted version of the P channel (LIP). In this configuration the LIN pin should be connected to analogue ground.

PIN	NAME	DESCRIPTION
16	INP_SEL	Input Mode Select 0 = Differential Mode (LIP/LIN) 1 = Single-Ended Mode (LIP only)

Table 2 Input Mode Control

WM9001 inputs LIP and LIN are biased to Vmid (equal to AVDD/2) therefore DC-blocking capacitors are required when connecting non Vmid reference input signals. The Vmid pin must be decoupled externally – see 'Applications Information' for more detail.

SYNC

In Class D operation the WM9001 may be clocked using one of two methods.

- Externally supplied clock to the SYNC pin (800kHz typical).
- Internal oscillator, allowing stand-alone operation of the device.

The Clock source selection is determined automatically by the WM9001 according to the status of the SYNC pin. If a clock signal is present on the SYNC pin, then this signal is automatically selected as the WM9001 clock source. If the clock signal is interrupted and this pin is pulled high or low, then the internal oscillator will be selected. It is not recommended to interrupt or change clock sources whilst the device is enabled.

PIN	NAME	DESCRIPTION
5	SYNC	Class D PWM clock input Constant 0 / 1 – Internal Oscillator enabled Clock – Clock used to sync PWM class D

Table 3 Sync Clock Control

The SYNC pin is compatible with low voltage (eg. 1.8v) logic levels from external devices, and can accept logic 1 digital inputs as low as 1.6V, even though the WM9001 AVDD supply minimum is 2.7V. This provides compatibility with a low voltage DVDD on a controlling device such as the WM8991 CODEC.

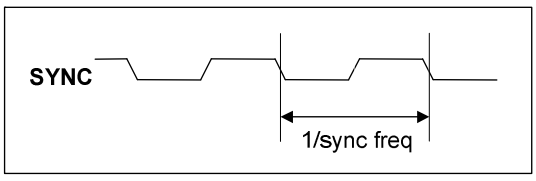


Figure 6 System Clock Timing Requirements

Please refer to the Electrical Characteristics for minimum and maximum SYNC frequencies.

SPEAKER DRIVER MODE SELECT

The speaker outputs operate in a BTL configuration, in either class AB or class D mode. The speaker driver mode is selected using the CDMODE pin.

PIN	NAME	DESCRIPTION
7	CDMODE	Class AB/D Mode Select 0 = Class D mode 1 = Class AB mode

Table 4 Class AB / D Mode Control

SIGNAL BOOST CONTROL

Six levels of signal boost are available to provide maximum output power for many commonly used SPKVDD/AVDD combinations. These boost options are available in class AB and class D modes.

AC and DC gain levels from 1.0x to 1.8x are selected using the BSEL[2:0] input pins. Note that ACGAIN = DCGAIN for all settings.

An appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when signal boost is used.

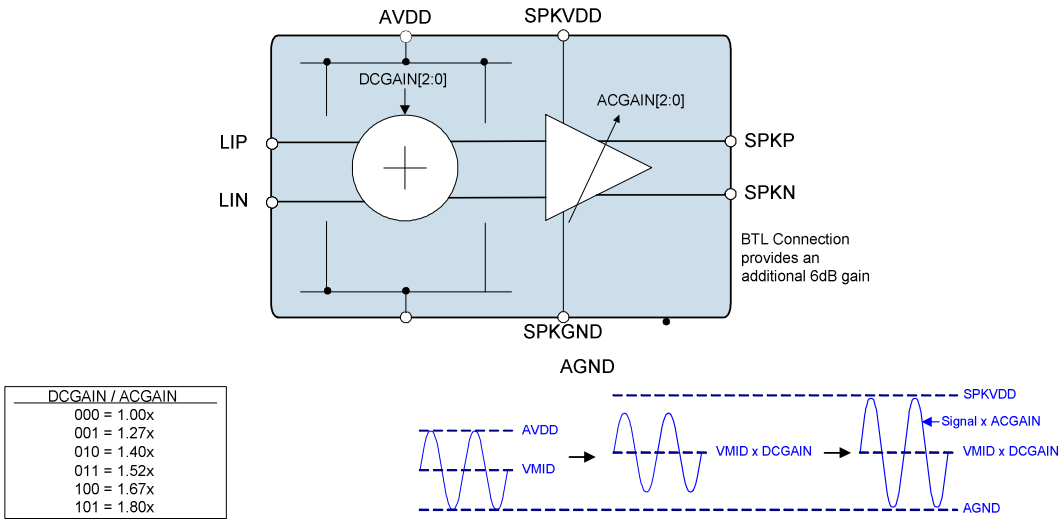


Figure 7 Signal Boost Operation

PIN	NAME	DESCRIPTION
12,11,10	BSEL[2:0]	Signal Boost Control 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 = Reserved 111 = Reserved

Table 5 Signal Boost Control

To prevent pop noise, the BSEL[2:0] settings should not be modified while the speaker outputs are enabled. Note that ACGAIN = DCGAIN for all settings.

THERMAL SHUTDOWN

To protect the WM9001 from damage due to overheating, a thermal shutdown circuit is included. If the junction temperature exceeds approximately 150ºC, then the WM9001 will be disabled.

Note that the internal power dissipation of the WM9001 is significantly higher in class AB mode than in class D mode – see “Power De-Rating” section.

It is not possible to disable the thermal shutdown function.

RF NOISE SUPPRESSION

The WM9001 provides internal RF filtering which minimises the impact of high frequency noise in the system.

POPS / CLICK SUPPRESSION

The WM9001 incorporates mechanisms that reduce audible pops/clicks at the speaker outputs.

To prevent pop noise, it is recommended that the BSEL, SYNC, CDMODE and INP_SEL settings should not be modified while the speaker outputs are enabled. Muting the device (setting EN = 0) during any update to these settings is recommended.

APPLICATIONS INFORMATION

TYPICAL STAND-ALONE USAGE

The WM9001 may be used as a differential speaker amplifier, as illustrated in Figure 8, or as a single-ended speaker amplifier in Figure 9.

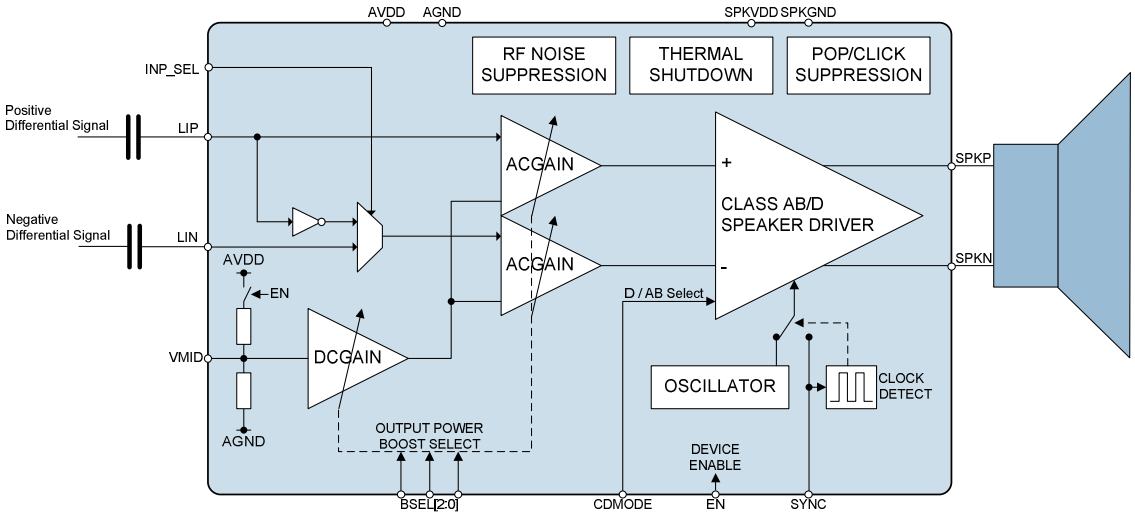


Figure 8 Operation of WM9001 as Stand-alone Differential Amplifier

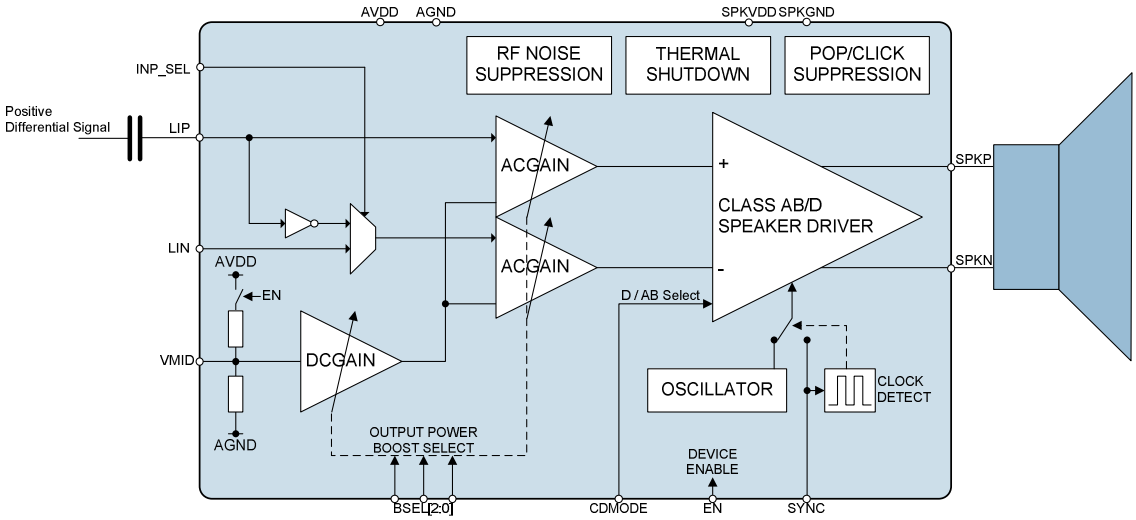


Figure 9 Operation of WM9001 as a Stand-alone Single-ended Amplifier

In the both configurations DC blocking capacitors are required on the input paths. A typical application might use 1uF capacitors for this purpose, providing a high pass cut-off frequency of less than 20Hz.

In single-ended mode it is recommend that the unused LIN input is connected to analogue ground.

TYPICAL USAGE WITH WM8991 CODEC

The WM9001 may be used in conjunction with a CODEC such as the WM8991 to provide a complete stereo solution. Such a solution allows the left and right drivers to be positioned separately as close to the speakers as possible, minimising EMI emissions from long speaker cables.

In this configuration the EN & SYNC pins may be driven from GPIO outputs from the WM8991, and, providing that the WM8991 and WM9001 are connected to the same analogue supply (AVDD), then DC blocking capacitors are not required on the LIP and LIN inputs to WM9001.

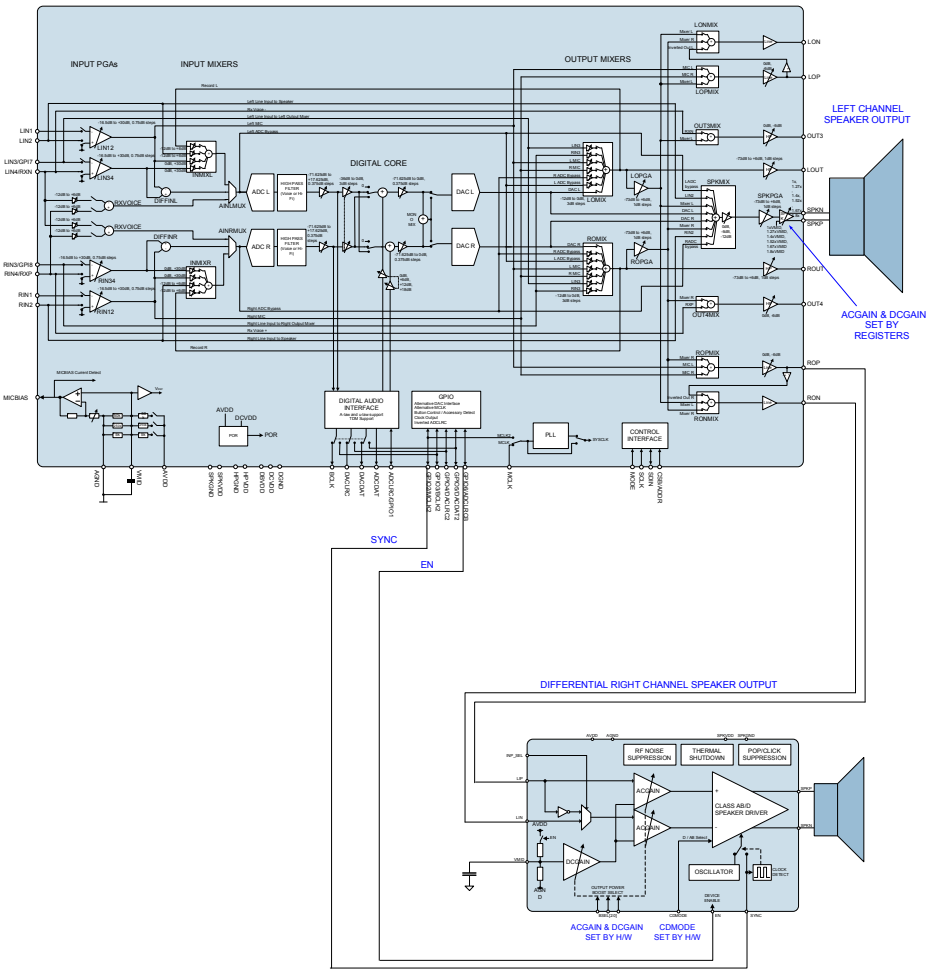


Figure 10 Operation of WM9001 in Conjunction with WM8991

The EN and SYNC pins are compatible with low voltage (eg. 1.8v) logic levels from external devices, and can accept logic 1 digital inputs as low as 1.6V, even though the WM9001 AVDD supply minimum is 2.7V. This provides compatibility with a low voltage DVDD on a controlling device such as the WM8991 CODEC.

SPEAKER SELECTION

In Class D driver mode, the WM9001 output contains high frequency signals resulting from the switched PWM operation. To avoid the need for specific filter components, it is important to make an appropriate choice of loudspeaker. Note that, for Class AB mode usage, the choice of speaker is not so important as there are no high frequency harmonics in the WM9001 output.

The speaker inductance and load resistance create a low-pass filter which, ideally, will attenuate the high frequency Class D switching harmonics whilst passing the desired audio frequencies. The 3dB cut-off frequency of the speaker inductance and resistance may be calculated as follows:

$$f_c = R_L / 2\pi L$$

Therefore, for an 8Ω speaker and a desired 3dB cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20kHz = 64\mu H$$

8Ω speakers for portable applications typically have an inductance in the range 20µH to 100µH. If the inductance is higher than value calculated above, then the cut-off frequency will be reduced, limiting the audio bandwidth. Lower values of inductance will result in a higher cut-off frequency. The Class D outputs contain harmonics at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter must therefore be low enough to protect the speaker.

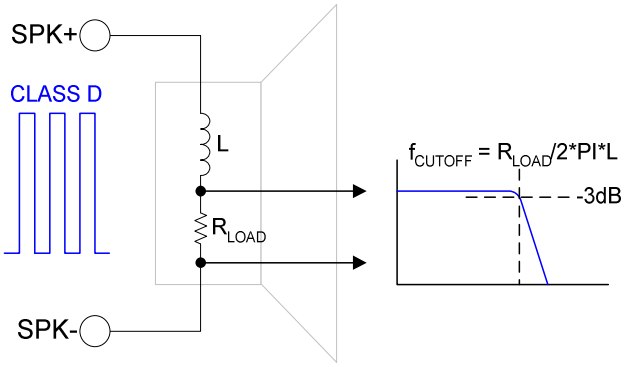


Figure 11 Speaker Equivalent Circuit

PCB LAYOUT CONSIDERATIONS

The efficiency of the speaker drivers is affected by the series resistance between the WM9001 and the speaker (e.g. inductor ESR) as shown in Figure 12. This resistance should be as low as possible to aximizi efficiency.

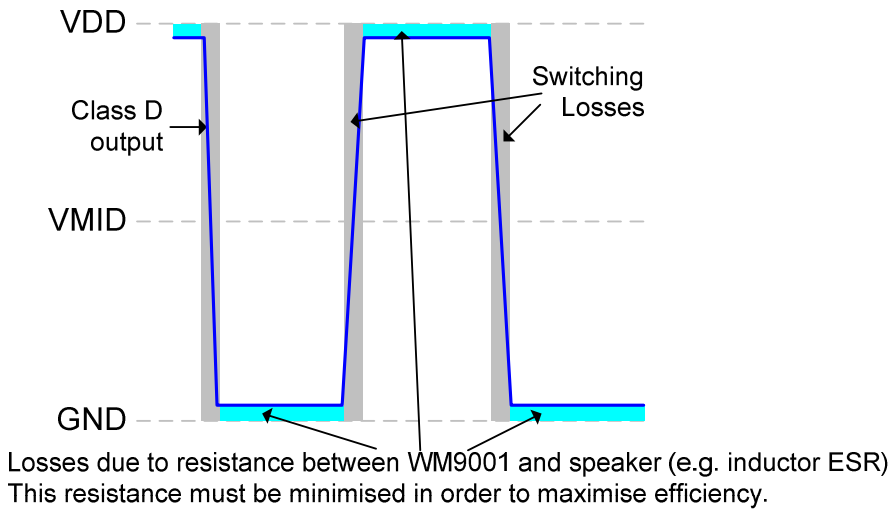


Figure 12 Speaker Connection Losses

The distance between the WM9001 and the speakers should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 13. When additional passive filtering is used, low ESR components should be chosen to aximizi series resistance between the WM9001 and the speaker, aximizing efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.

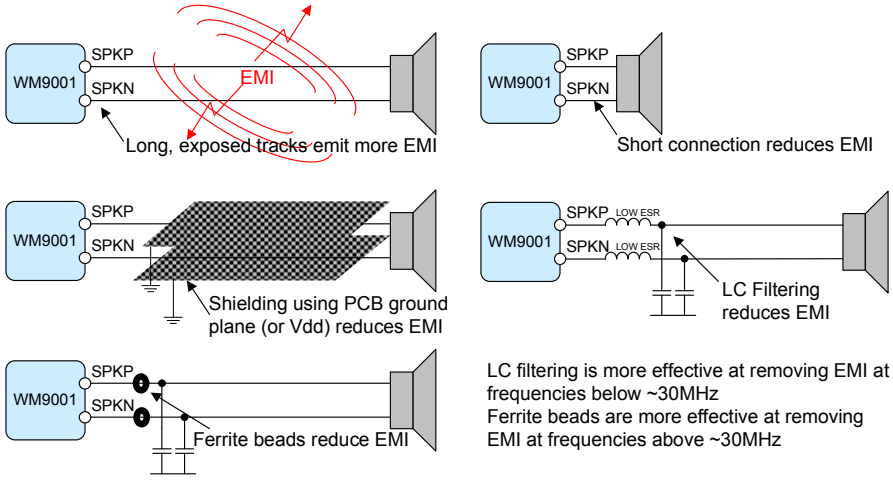
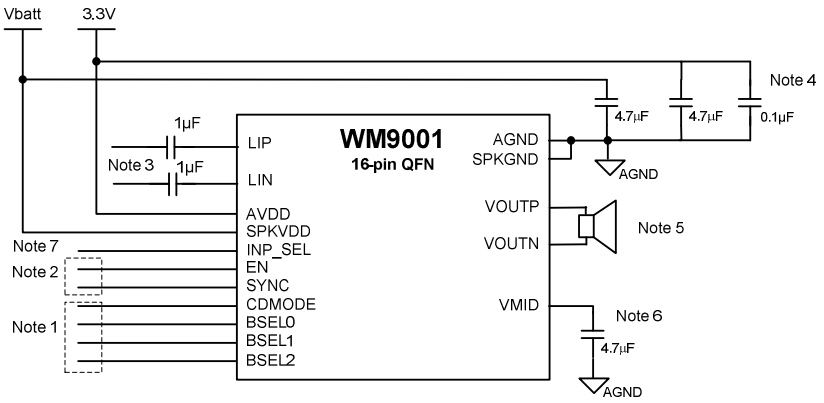


Figure 13 EMI Reduction Techniques

RECOMMENDED EXTERNAL COMPONENTS



Notes

Note 1: BSEL[2:0] set the AC and DC gain and CDMODE selects the speaker mode. These can either be driven high or low by external GPIO lines or directly wired to AVDD or GND. Connecting CDMODE to logic 1 = class AB operation. Connecting CDMODE to logic 0 = class D operation.

Note 2: EN and SYNC enable the device and set the PWM clock respectively. These pins can accept logic 1 digital signals as low as 1.6V

Note 3: LIP and LIN pins are biased to VMID (AVDD/2). 1uF capacitors remove DC bias from line inputs. If operating with another Wolfson device (e.g. 8991) which operates from the same AVDD, then these capacitors are not necessary as VMID levels will be matched. Note that the LIN input capacitor is only required for differential mode.

Note 4: Supply decoupling capacitors on AVDD and SPKVDD should be positioned as close to the WM9001 as possible. Values indicated are minimum requirements. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

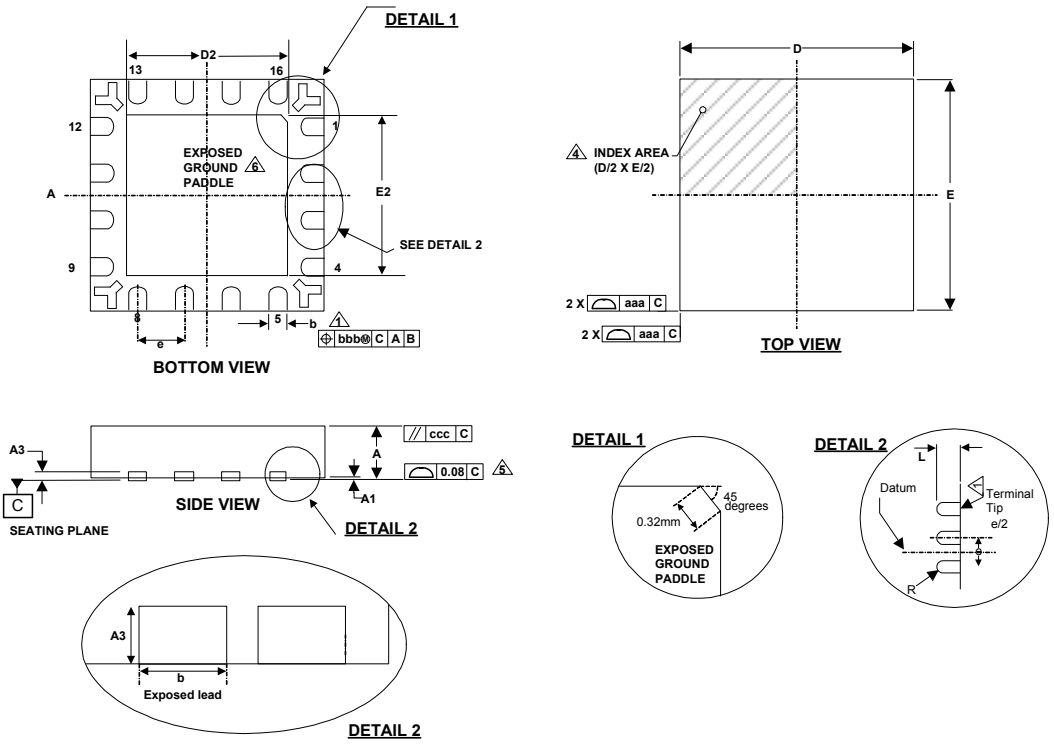
Note 5: The loudspeaker should be connected as close as possible to the WM9001. When this is not possible, filtering should be placed on the speaker outputs close to the WM9001.

Note 6: Supply decoupling capacitors on VMID should be positioned as close to the WM9001 as possible. Value indicated is the recommended value.

Note 7: INP_SEL should be tied to AGND for differential mode and to AVDD for single-ended mode.

PACKAGE DIMENSIONS

FL: 16 PIN QFN PLASTIC PACKAGE 3 x 3 x 0.75 mm BODY, 0.50 mm LEAD PITCH **DM053.C**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.20	0.25	0.30	1
D		3.00 BSC		
D2	1.65	1.70	1.75	2
E		3.00 BSC		
E2	1.65	1.70	1.75	2
e		0.50 BSC		
L	0.325	0.375	0.425	
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VGGD-2.			

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VGGD-2.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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