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Spec No: 001-10179

Spec Title: CY2X014, LOW JITTER LVPECL CRYSTAL OSCILLATOR

Sunset Owner: Amitava Banerjee (TAVA)

Replaced by: 001-88287

CY2X014

Low Jitter LVPECL Crystal Oscillator

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Features

- Low jitter crystal oscillator (XO)
- Less than 1 ps typical root mean square (RMS) phase jitter
- Differential low-voltage positive emitter coupled logic (LVPECL) output
- Output frequency from 50 MHz to 690 MHz
- Factory-configured or field-programmable
- Integrated phase-locked loop (PLL)
- Output enable or power-down function
- Supply voltage: 3.3 V or 2.5 V
- Pb-free package: 5.0 x 3.2 mm leadless chip carrier (LCC)
- Commercial and industrial temperature ranges

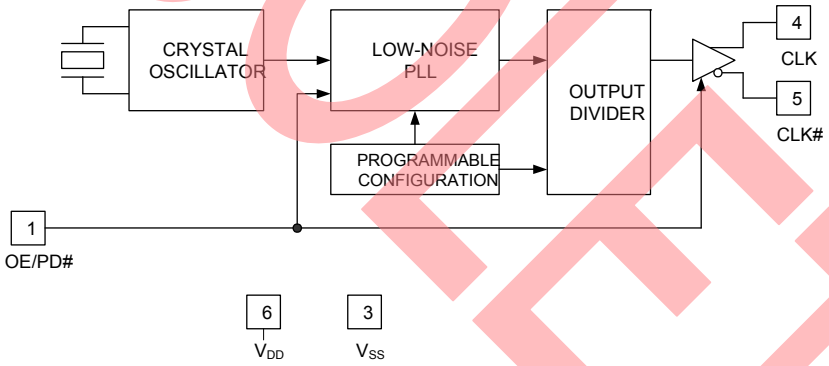
Functional Description

The CY2X014 is a high-performance and high-frequency XO. The device uses a Cypress proprietary low-noise PLL to synthesize the frequency from an embedded crystal.

The CY2X014 is available as a factory-configured device or as a field-programmable device. Factory-configured devices are configured for general use or they can be customer specific.

For a complete list of related documentation, click here.

Logic Block Diagram



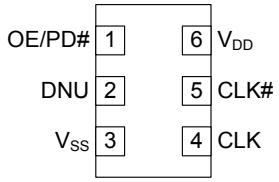
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Pin Configurations

Figure 1. 6-pin Ceramic LCC pinout



Pin Definitions

Pin	Name	I/O Type	Description
1	OE/PD#	CMOS input	**Output enable pin**: Active HIGH. If OE = 1, CLK is enabled. **Power-down pin**: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. The functionality of this pin is programmable.
4, 5	CLK, CLK#	LVPECL output	**Differential output clock**
2	DNU	–	**Do not use**: DNU pins are electrically connected, but perform no function
6	V_{DD}	Power	**Supply voltage**: 2.5 V or 3.3 V
3	V_{SS}	Power	**Ground**

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Programming Description

The CY2X014 is a programmable device. Prior to being used in an application, it must be programmed with the output frequency and other variables described in Programming Variables. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field-programmable CY2X014

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyClockWizard™ software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using the CyClockWizard software along with a CY3675-CLKMAKER1 CyClockMaker Clock Programmer Kit with a CY3675-LCC6A socket adapter. Cypress's value-added distribution partners also provide programming services. Field-programmable devices are designated with an 'F' in the part number. They are intended for quick prototyping and inventory reduction.

The software and programmer kit hardware can be downloaded from www.cypress.com by clicking the hyperlinks in the previous paragraph.

Factory-configured CY2X014

For ready-to-use devices, the CY2X014 is available with no field programming required. A request for a custom configuration can be made. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders. The CY2X014 is one-time programmable (OTP).

Programming Variables

Output Frequency

The CY2X014 can synthesize a frequency to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2X014 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2X014 cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Pin 1: Output Enable (OE) or Power Down (PD#)

Pin 1 is programmed as either OE or PD#. The OE function is used to enable or disable the CLK output quickly, but it does not reduce core power consumption. The PD# function puts the device into a low power state, but the wake-up takes longer because the PLL must reacquire the lock.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. They have a potentially significant impact on performance levels for applications requiring the lowest-possible phase noise. CyClockWIzard software allows the user to select between and view the expected performance of both options.

Table 1. Device Programming Variables

Variable
Output frequency
Pin 1 function (OE or PD#)
Temperature range (commercial or industrial)

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Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[1]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, storage	Non operating	–55	135	°C
T_J	Temperature, junction		–40	135	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection human body model (HBM)	JEDEC STD 22-A114-B	2000	–	V
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3-V supply voltage range	3.0	3.3	3.6	V
	2.5-V supply voltage range	2.375	2.5	2.625	V
T_{PU}	Power-up time for V_{DD} to reach minimum specified voltage (power ramp is monotonic)	0.05	–	500	ms
T_A	Ambient temperature (commercial)	0	–	70	°C
	Ambient temperature (industrial)	–40	–	85	°C

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Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[3]	Operating supply current	V_{DD} = 3.6 V, CLK = 150 MHz, OE/PD# = V_{DD}, output terminated	–	–	150	mA
		V_{DD} = 2.625 V, CLK = 150 MHz, OE/PD# = V_{DD}, output terminated	–	–	145	mA
I_{SB}	Standby supply current	PD# = V_{SS}	–	–	200	µA
V_{OH}	LVPECL high output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} – 1.15	–	V_{DD} – 0.75	V
V_{OL}	LVPECL low output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} – 2.0	–	V_{DD} – 1.625	V
V_{OD1}	LVPECL output voltage swing (V_{OH} – V_{OL})	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	600	–	1000	mV
V_{OD2}	LVPECL output voltage swing (V_{OH} – V_{OL})	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	500	–	1000	mV
V_{OCM}	LVPECL output common mode voltage (V_{OH} + V_{OL})/2	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	1.2	–	–	V
I_{OZ}	LVPECL output leakage current	PD#/OE = V_{SS}	–35	–	35	µA
V_{IH}	Input high voltage		0.7 × V_{DD}	–	–	V
V_{IL}	Input low voltage		–	–	0.3 × V_{DD}	V
I_{IH}	Input high current	Input = V_{DD}	–	–	115	µA
I_{IL}	Input low current	Input = V_{SS}	–	–	50	µA
C_{IN}	Input capacitance		–	15	–	pF

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Note
3. I_{DD} includes ~24 mA of current that is dissipated externally in the output termination resistors.

AC Electrical Characteristics

The following table lists the AC electrical specifications for this device.

Parameter [4]	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output frequency [5]		50	–	690	MHz
FSC	Frequency stability, commercial devices [6]	V_{DD} = min to max, T_A = 0 °C to 70 °C	–	–	±35	ppm
FSI	Frequency stability, industrial devices [6]	V_{DD} = min to max, T_A = –40 °C to 85 °C	–	–	±55	ppm
AG	Aging, 10 years		–	–	±15	ppm
T_{DC}	Output duty cycle	F ≤ 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output rise and fall time	20% and 80% of full output swing	0.2	0.4	1.0	ns
T_{OHZ}	Output disable time	Time from falling edge on OE to stopped outputs (asynchronous)	–	–	100	ns
T_{OE}	Output enable time	Time from rising edge on OE to outputs at a valid frequency (asynchronous)	–	–	100	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD} (min.) or from PD# rising edge	–	–	10	ms
$T_{Jitter(\phi)}$	RMS phase jitter (random)	F_{OUT} = 106.25 MHz (12 kHz to 20 MHz)	–	1	–	ps
		Pre-defined factory configurations		–		ps

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Notes
4. Not 100% tested, guaranteed by design and characterization.
5. This parameter is specified in the CyClockWizard software.
6. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, and variation from temperature and supply voltage.

Typical Output Characteristics

Figure 2. 2.5-V Supply and Termination to V_{DD} – 1.5 V, Minimum V_{DD} and Maximum T_A

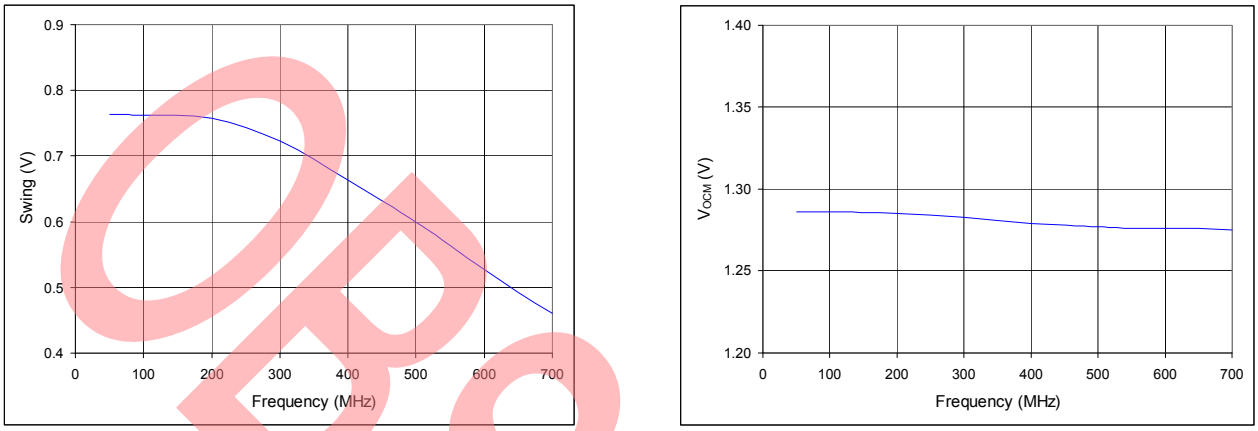


Figure 3. 2.5-V Supply and Termination to V_{DD} – 2 V, Minimum V_{DD} and Maximum T_A

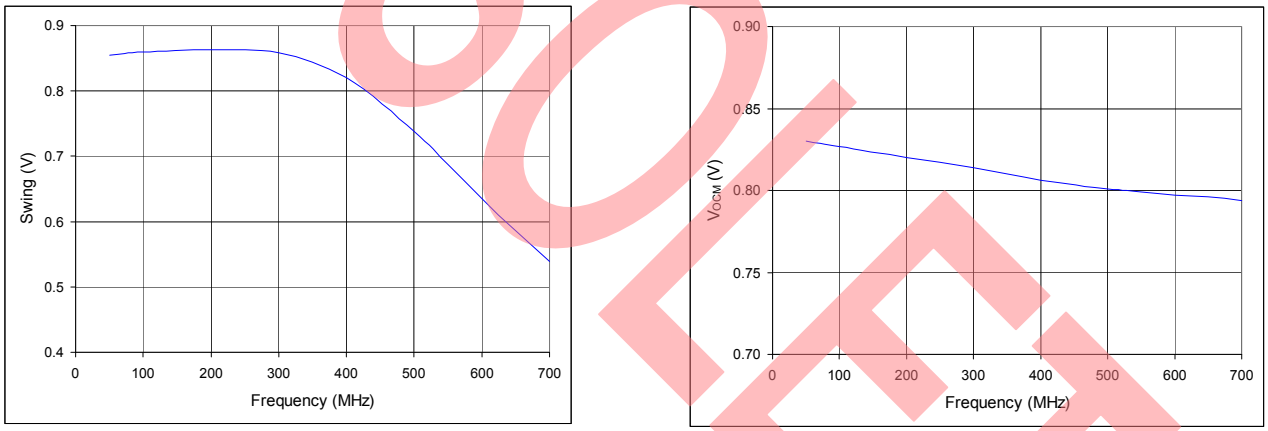
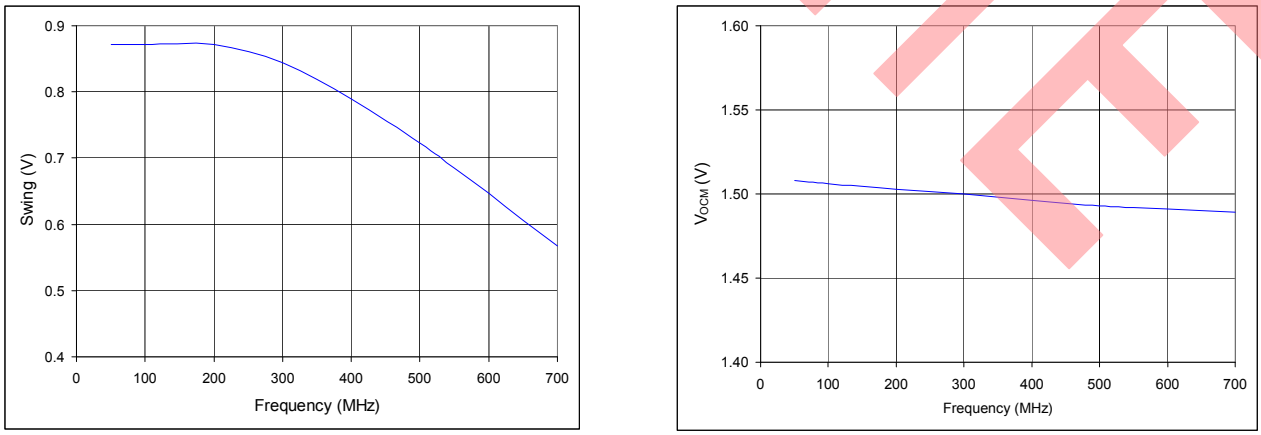


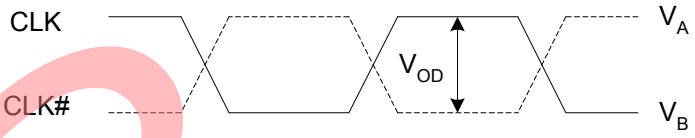
Figure 4. 3.3-V Supply and Termination to V_{DD} – 2 V, Minimum V_{DD} and Maximum T_A



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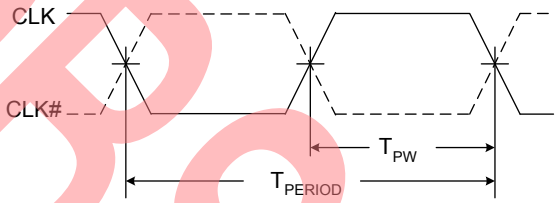
Switching Waveforms

Figure 5. Output DC Parameters



$$V_{OCM} = (V_A + V_B)/2$$

Figure 6. Duty Cycle Timing



$$T_{DC} = \frac{T_{PW}}{T_{PERIOD}}$$

Figure 7. Output Rise and Fall Time

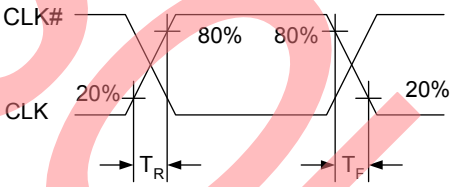
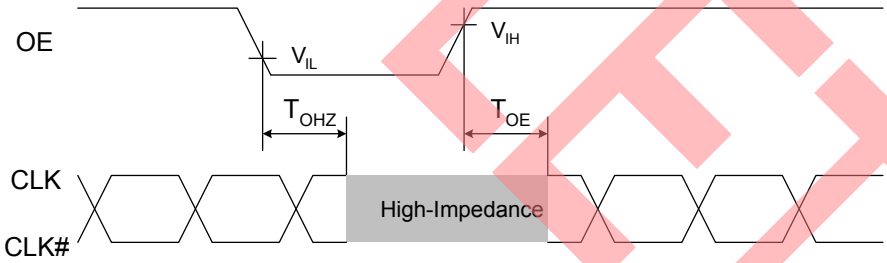


Figure 8. Output Enable and Disable Timing



Termination Circuits

Figure 9. LVPECL Termination



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Ordering Information

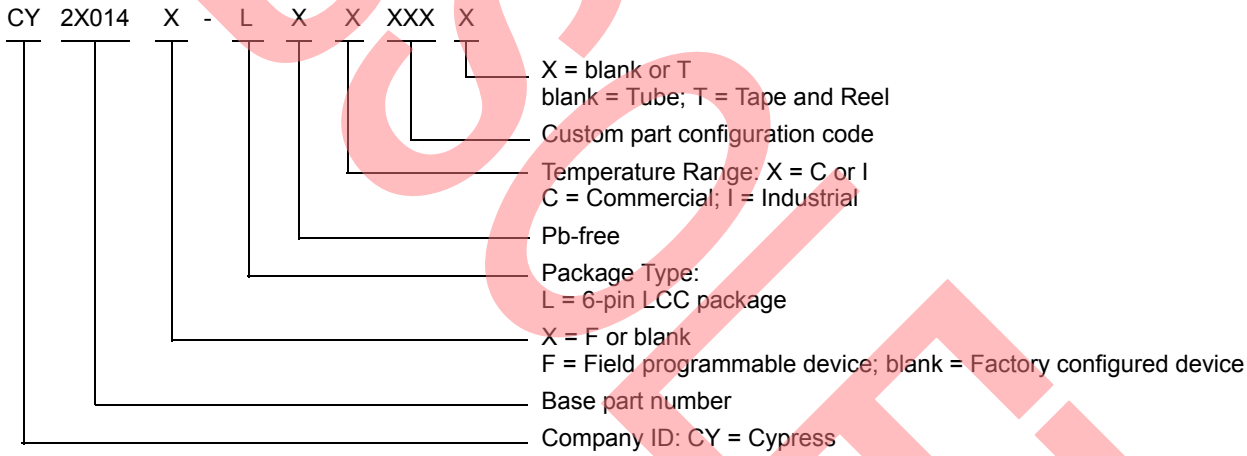
Part Number	Configuration	Package Description	Product Flow
Pb-free			
CY2X014FLXIT	Field-programmable	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C

Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

Part Number [7]	Configuration	Package Description	Product Flow
CY2X014LXCxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2X014LXIxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions

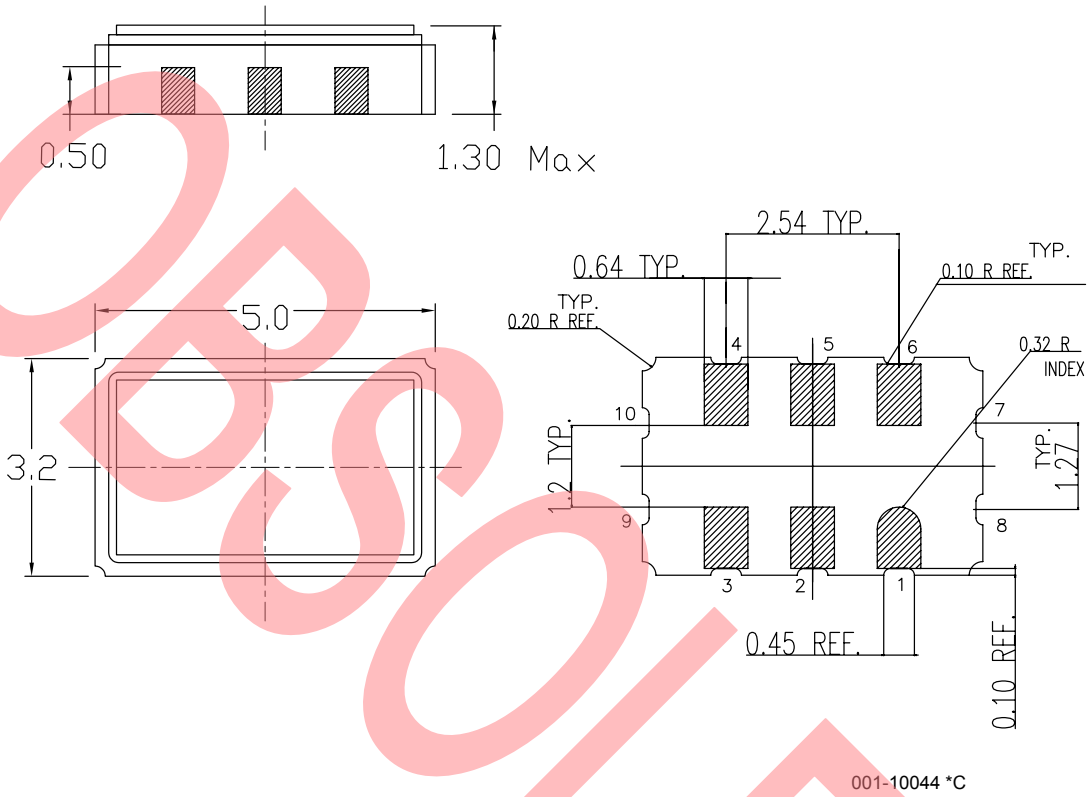


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Note
7. "xxx" indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or Sales Representative.

Package Diagrams

Figure 10. 6-pin Ceramic LCC (5.0 × 3.2 × 1.3 mm) LZ06A Package Outline, 001-10044



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Acronyms

Acronym	Description
ESD	electrostatic discharge
FAE	field application engineer
HBM	human body model
JEDEC	joint electron devices engineering council
LCC	leadless chip carrier
LVPECL	low-voltage positive-referenced emitter coupled logic
OE	output enable
OTP	one-time programmable
PCB	printed circuit board
PLL	phase-locked loop
RMS	root mean square
SMD	surface mount device
XO	crystal oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

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Document History Page

Document Title: CY2X014, Low Jitter LVPECL Crystal Oscillator Document Number: 001-10179				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	504478	RGL	See ECN	New datasheet
*A	1428603	JWK / SFV	See ECN	Removed pull up on pin 1 and related specifications, Added items to Programming Variables section, Added C_{IN} specification, Modified t_{J2}, I_{IH}, I_{IL}, I_{DD} and I_{SB} specifications, Changed to a single Frequency Stability specification, Removed Peak-to-peak Period Jitter specification, Changed pin 2 from NC to DNU, Changed max storage temperature, Title change, 2.5V supply tightened from ±10% to ±5%, 2.5V termination option changed from VDD-1.4V to VDD-1.5V, Added typical output characteristic curves
*B	2669117	KVM / AESA	03/05/09	Revised frequency stability and aging specs and conditions, Max frequency changed from 700 MHz to 690 MHz, Duty cycle changed from 45/55 to 40/60 for freq > 450 MHz, Removed reference to CY3672 programmer, Junction and storage temperatures changed from 125 to 135°C, IIH changed from 20 µA to 115 µA, IIL changed from 20 µA to 50 µA, Rise and fall times changed from 350 ps to 500 ps, Removed MSL spec, Changed Datasheet Status to Final.
*C	2701663	KVM / PYRS	05/06/09	General clean up Added explanation of gaps in the frequency range Added URL for software Removed frequency stability paragraph under Programming Variables Added programming variables table Added separate IDD spec for 2.5V supply Changed the amount of load current in IDD footnote Changed phase jitter parameter name Removed supply voltage as a programming variable Changed conditions for ESD spec Changed rise and fall times from 500 ps to 400 ps typ, added min and max
*D	2718433	WWZ / HMT	06/12/09	No change. Submit to ECN for product launch.
*E	2761943	KVM	09/10/09	Revised maximum output rise and fall times.
*F	2896548	KVM	03/19/10	Moved parts with 'xxx' into new table, Possible Configurations Updated package diagram
*G	2973338	CXQ	07/08/2010	Added Standard and Application-Specific Factory Configurations. Added phase jitter specs for pre-defined configurations in AC Electrical Characteristics (note 7 refers users to the new table on page 2 for typical specs). Added all new factory programmed devices from the Standard and Application-Specific Factory Configurations to Ordering Information. Added note 8 to reference the configuration descriptions for each new device. Changed all references to CyberClocksOnline software to CyClockWizard. Removed section on phase noise vs jitter SW optimization.
*H	3767932	PURU	10/05/2012	Updated Package Diagrams (spec 001-10044 (Changed revision from *A to *B)). Added Units of Measure. Updated to new template.
*I	3845087	PURU	12/20/2012	Removed references of "Standard and Application-Specific Factory Configurations" in Functional Description. Removed "Standard and Application-Specific Factory Configurations". Removed references of "Standard and Application-Specific Factory Configurations" in Factory-configured CY2X014 under Programming Description. Updated Ordering Information (Updated part numbers).

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Document History Page (continued)

Document Title: CY2X014, Low Jitter LVPECL Crystal Oscillator Document Number: 001-10179				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	4587303	PURU	12/05/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Ordering Information: Removed prune part number CY2X014FLXCT. Updated Package Diagrams: spec 001-10044 – Changed revision from *B to *C. Updated to new template.
*K	5003622	TAVA	11/06/2015	Obsolete document. Completing Sunset Review.

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