March 1999

National Semiconductor

54LVX4245
8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a TRI-STATE condition. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

The LVX4245 is suitable for mixed voltage applications such as systems using 3.3V memories which must interface with existing buses or other components operating at 5.0V.

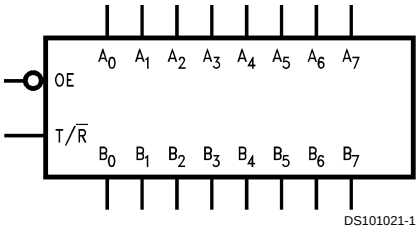
Features

- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A port and 3V data flow at B port
- Outputs source/sink 24 mA
- Available in Ceramic DIP and Flatpack packages
- Implements patented EMI reduction circuitry
- Functionally compatible with the 54 series 245
- Standard Microcircuit Drawing (SMD) 5962-9860601

Ordering Code

Order Number	Package Number	Package Description
54LVX4245J-QML	J24F	24-Lead Ceramic Dual-in-line
54LVX4245W-QML	W24C	24-Lead Cerpack

Logic Symbol



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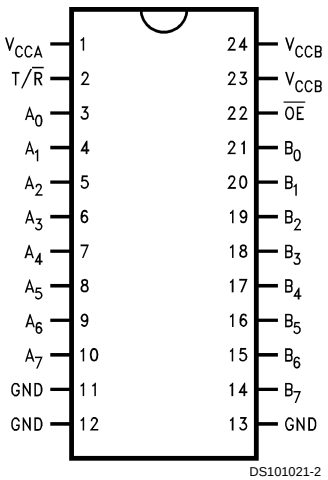
Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for CDIP and Cerpack



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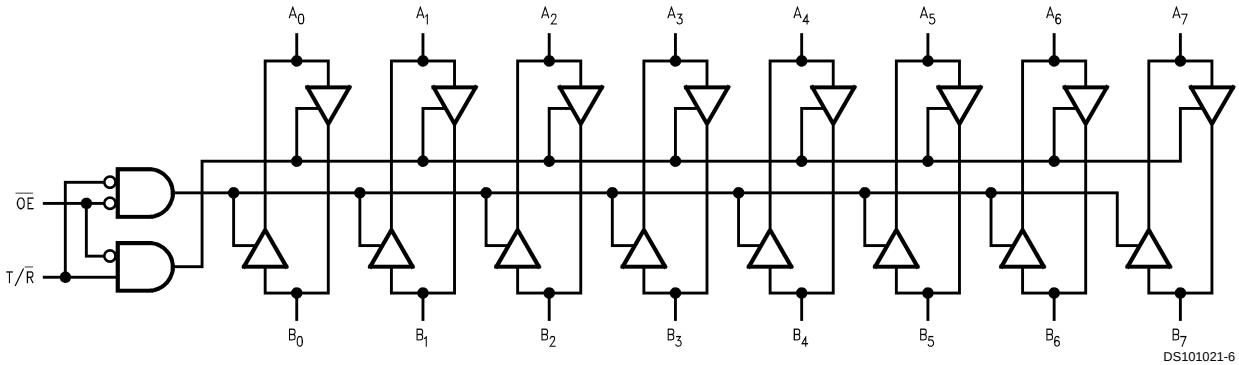
Connection Diagram (Continued)

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A(n)	−0.5V to V_{CCA} + 0.5V
@B(n)	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN})	
@ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current	
(I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±200 mA
@ I_{CCB}	±200 mA
Storage Temperature Range	
(T_{STG})	−65˚C to +150˚C

Recommended Operating Conditions (Note 2)

Supply Voltage	
V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 3.6V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@ A(n)	0V to V_{CCA}
@ B(n)	0V to V_{CCB}
Free Air Operating Temperature (T_A)	
54LVX	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must he held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A = −55˚C to +125˚C	Units	Conditions
					Guaranteed Limits		
V_{IHA}	Minimum	A(n), T/$\overline{R}$,	5.5	3.3	2.0	V	V_{OUT} ≤ 0.1V or
	High Level	$\overline{OE}$	4.5	3.3	2.0		≥ V_{CC} − 0.1V
V_{IHB}	Input Voltage	B(n)	5.0	3.6	2.0		
			5.0	2.7	2.0		
V_{ILA}	Maximum	A(n), T/$\overline{R}$,	5.5	3.3	0.8	V	V_{OUT} ≤ 0.1V or
	Low Level	$\overline{OE}$	4.5	3.3	0.8		≥ V_{CC} −0.1V
V_{ILB}	Input Voltage	B(n)	5.0	2.7	0.8		
			5.0	3.6	0.8		
V_{OHA}	Minimum High Level		4.5	2.7	4.4	V	I_{OH} = −100 µA
	Output Voltage		5.5	3.6	5.4		I_{OH} = −100 µA
			4.5	3.0	3.7		I_{OH} = −24 mA
V_{OHB}			4.5	2.7	2.6	V	I_{OH} = −100 µA
			5.5	3.6	3.5		I_{OH} = −100 µA
			4.5	2.7	2.2		I_{OH} = −12 mA
			4.5	3.0	2.4		I_{OH} = −12 mA
			4.5	3.0	2.2		I_{OH} = −24 mA
V_{OLA}	Maximum Low Level		4.5	2.7	0.1	V	I_{OL} =100 µA
	Output Voltage		5.5	3.6	0.1		I_{OL} =100 µA
			4.5	3.0	0.4		I_{OL} = 24 mA
V_{OLB}			4.5	2.7	0.1		I_{OL} = 100 µA
			5.5	3.6	0.1	V	I_{OL} = 100 µA
			4.5	2.7	0.4		I_{OL} = 12 mA
			4.5	3.0	0.3		I_{OL} = 12 mA
			4.5	3.0	0.4		I_{OL} = 24 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	T_A = −55°C to +125°C	Units	Conditions
				Guaranteed Limits		
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$	5.5	3.6	±1.0	µA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A(n)	5.5	3.6	±5.0	µA	T/$\overline{R}$ = 0.0V, $V_O = V_{CCA}$, GND
I_{OZB}	Maximum TRI-STATE Output Leakage @ B(n)	5.5	3.6	±5.0	µA	T/$\overline{R}$ = 5.5V, $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CCT}/Input @ A(n), T/$\overline{R}$, $\overline{OE}$	5.5	3.6	1.5	mA	$V_I = V_{CCA}$ − 2.1V, T/$\overline{R}$ = 5.5V
	Input @ B(n)	5.5	3.6	0.5	mA	$V_I = V_{CCB}$ − 0.6V, T/$\overline{R}$ = 0.0V
I_{CCA}	Quiescent V_{CCA} Supply Current	5.5	3.6	40	µA	B(n) = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = 0.0V
I_{CCB}	Quiescent V_{CCB} Supply Current	5.5	3.6	10	µA	A(n) = V_{CCA} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = 5.5V
V_{OLPA}	Quiet Output Maximum	5.0	3.3	1.5	V	(Notes 4, 5)
V_{OLPB}	Dynamic V_{OL}	5.0	3.3	0.8		
V_{OLVA}	Quiet Output Minimum	5.0	3.3	-1.1	V	(Notes 4, 5)
V_{OLVB}	Dynamic V_{OL}	5.0	3.3	-0.7		

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Worst case package.

Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

AC Electrical Characteristics

Symbol	Parameters	$T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF $V_{CCA} = 5V$ (Note 6) $V_{CCB} = 3.3V$ (Note 7)		$T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF $V_{CCA} = 5V$ (Note 6) $V_{CCB} = 2.7V$		Units
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	7.5 7.5	1.0 1.0	8.5 8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	8.5 8.5	1.0 1.0	9.0 9.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	8.0 8.0	1.0 1.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	7.5 7.5	1.0 1.0	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	0.5 0.5	7.0 7.0	0.5 0.5	7.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 8) Data to Output		1.5		1.5	ns

Note 6: Voltage Range 5.0V is 5.0V ±0.5V.

Note 7: Voltage Range 3.3V is 3.3V ±0.3V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

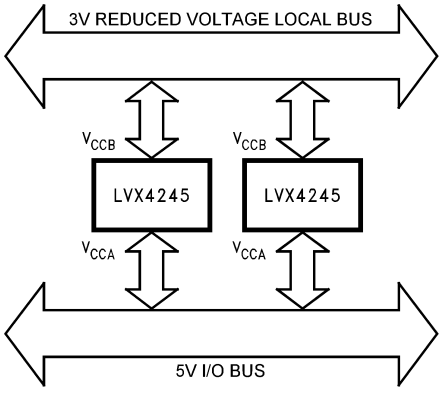
Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	10	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance	12	pF	V_{CCA} = 5.0V V_{CCB} = 3.3V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CCA} = 5.0V V_{CCB} = 3.3V

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications using 3.3V devices and 5V buses or IC's.



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Applications: Mixed Mode Dual Supply Interface Solution

LVX4245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latchup effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 5V port to interface 5V ICs. The "B" port is a dedicated port to interface 3V ICs. *Figure 2* shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

This device is also configured as an 8-bit 245 transceiver, giving the designer TRI-STATE capabilities and the ability to select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 54 series 245, as shown in *Figure 1*, the designer could use this device in either a 3V system or a 5V system without any further work to re-layout the board.

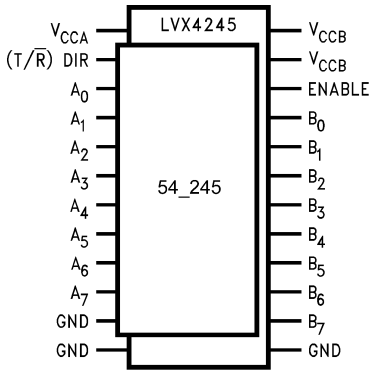


FIGURE 1. LVX4245 Pin Arrangement is Compatible to 20-Pin 54 Series 245

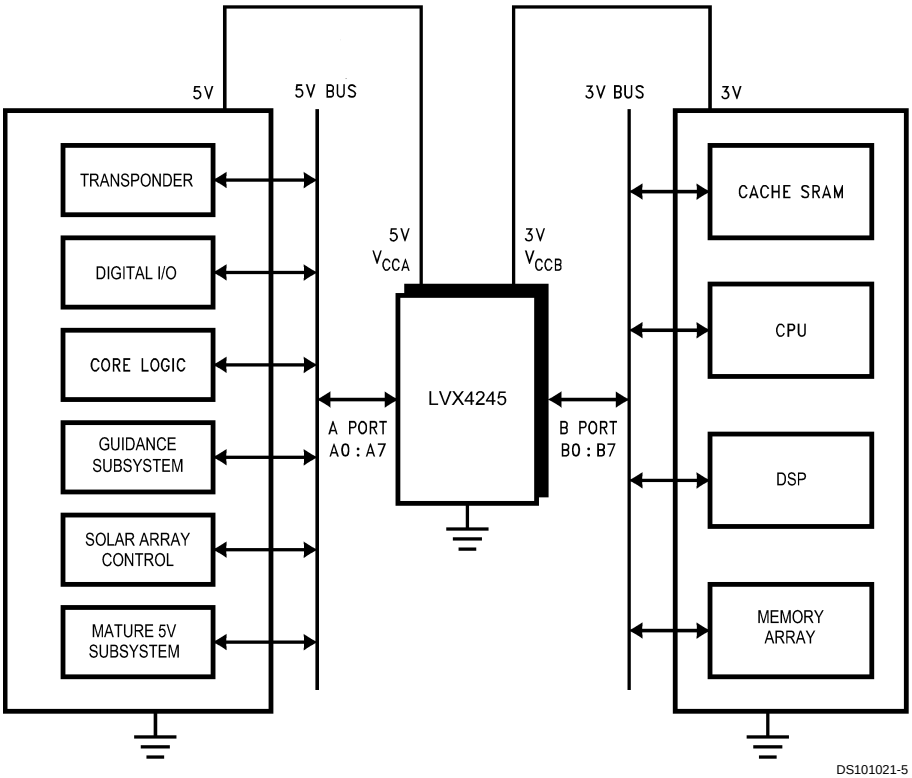
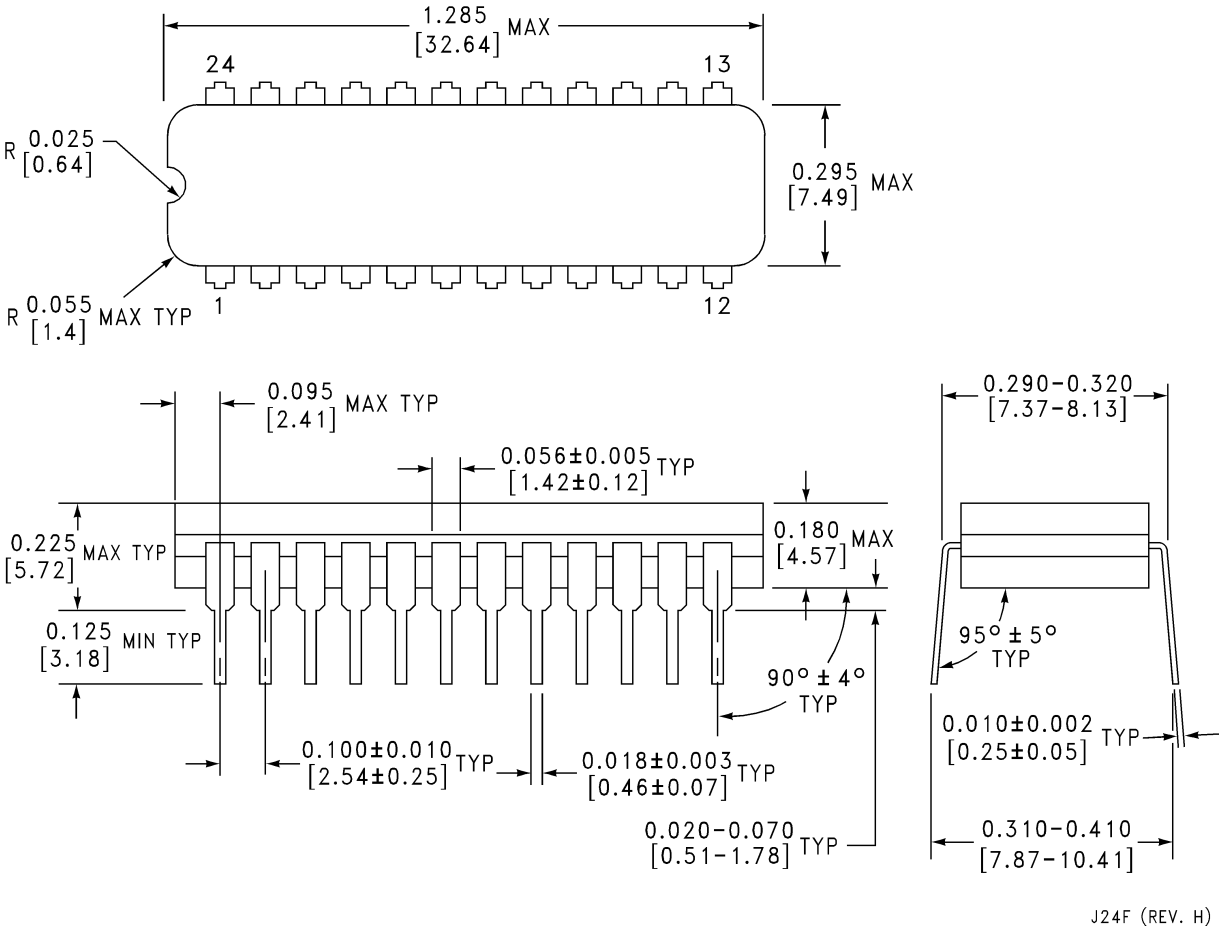
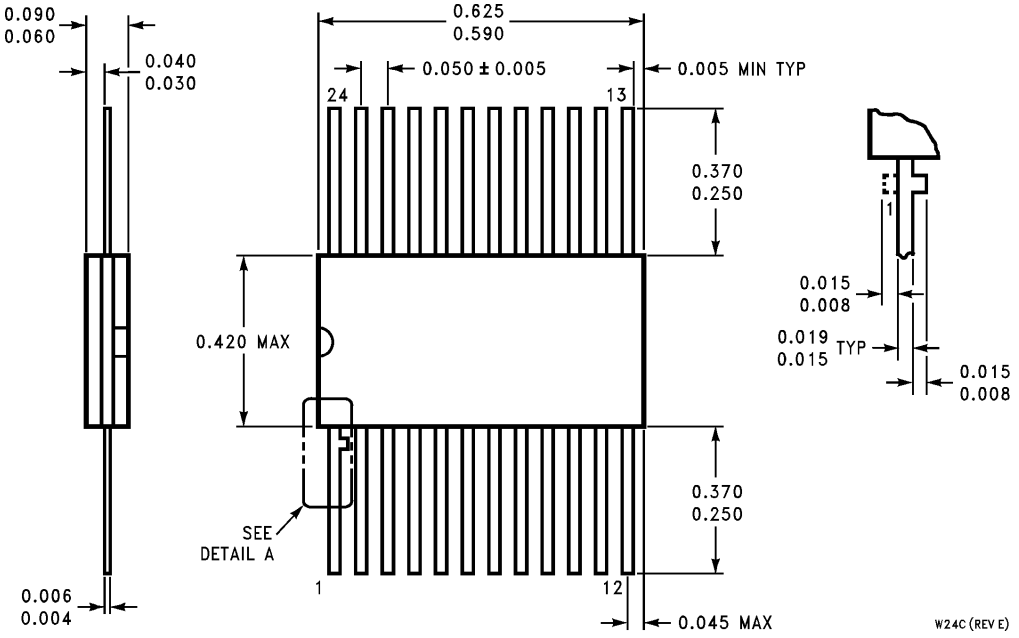


FIGURE 2. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-in-line
Package Number J24F



24-Lead Cerpack
Package Number W24C

Notes

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