Leiditech

LM0010-6L

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The LM0010-6L is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The PL0010-6L has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

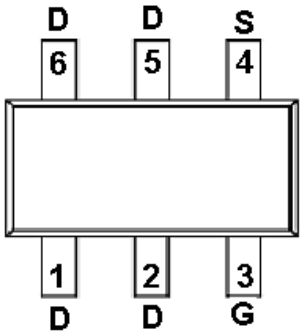
- Powered System
- DC/DC Converter
- Load Switch

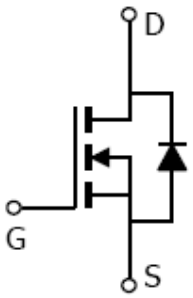
FEATURES

- 100V/3A,$R_{DS(ON)}$= 310mΩ@V_{GS}= 10V
- High density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)

PART MARKING





PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
LM0010-6L	SOT-23-6L	M10K MK

※ LM0010-6L : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	3.0	A
	T_A=70℃		2.0	
Pulsed Drain Current		I_{DM}	10	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1	2.0	2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=125℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V	3.0			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=3A		0.26	0.31	Ω
Forward Transconductance	gfs	V_{DS}=10V,I_D=3A		2.4		S
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=10V I_D= 5A		9	13	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	V_{DS}=25,V_{GS}=0V f=1MHz		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=10Ω I_D=3A,V_{GEN}=10V R_G=3.3Ω		2		nS
	t_r			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	t_f			18.8		

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