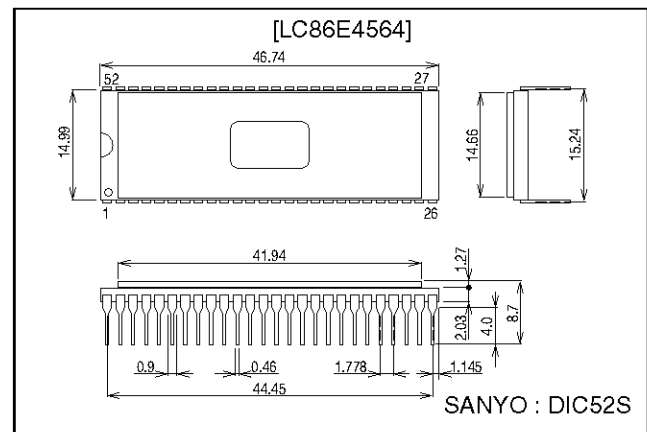


**LC86E4564****8-Bit Single-Chip Microcontroller****Preliminary****Overview**

The LC86E4564 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC864500 series. This microcontroller has the same function and the pin assignment as for the LC864500 series mask ROM version, and the 64K-byte EPROM. The program data is rewritable. It is suitable for developing programs.

Package Dimensions

unit : mm

3225-DIC52S**Features**

- (1) Option switching by EPROM data
The option function of the LC864500 series can be specified by the EPROM data.
The functions of the trial pieces can be evaluated using the mass production board.
- (2) Internal EPROM capacity : 65512 bytes (for program)
: 8192 × 12-bit (for character)
- (3) Internal RAM capacity : 256 bytes

Mask ROM version	EPROM capacity	RAM capacity
LC864532	32768 bytes	256 bytes
LC864528	28672 bytes	256 bytes
LC864524	24576 bytes	256 bytes
LC864520	20480 bytes	256 bytes
LC864516	16256 bytes	256 bytes
LC864512	12288 bytes	256 bytes
LC864508	8192 bytes	256 bytes

- (4) Operating voltage : 4.5 V to 5.5 V
- (5) Instruction cycle time : 1.0 μs to 366 μs
- (6) Operating temperature : +10°C to +40°C
- (7) The pin and the package compatible with the LC864500 series mask ROM devices
- (8) Applicable mask ROM version : LC864532, LC864528, LC864524, LC864520, LC864516, LC864512, LC864508
- (9) Factory shipment : DIC52S

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC86E4564

Usage Notes

When using, take notice of the followings.

(1) Differences between the LC86E4564 and the LC864500 series

Item	LC86E4564	LC864532/28/24/20/16/12/08
Operation after reset releasing	The option is specified by degrees until 3 ms after going to a 'H' level to the reset pin. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset pin.
Operating voltage range (V_{DD})	4.5 V to 6.0 V	2.5 V to 6.0 V
Operating temperature range (T_{opr})	+10 to +40°C	-30 to +70°C
Current drain	Refer to 'Electrical Characteristics' on the semiconductor news.	

The LC86E4564 uses the program memory area of 256 bytes from 0FF00H to 0FFFFH to select the options.

• The option types of the LC86E4564

Option types	Pins, Circuits	Contents of the option
Input/output form of input/output ports	Port 0	1. N-channel open drain output 2. CMOS output *1
		1. Pull-up MOS transistor provided 2. Pull-up MOS transistor not provided *2
	Port 1 *1	1. Input : Programmable pull-up MOS transistor Output : N-channel open drain 2. Input : Programmable pull-up MOS transistor Output : CMOS
Port 7 pull-up MOS transistor	Port 7 *1	1. Input : No Programmable pull-up MOS transistor 2. Input : Programmable pull-up MOS transistor

*1) Specified in bit

*2) Specified in nibble unit. Pull-up MOS transistor is not provided in N-channel open drain output port.

(2) Option

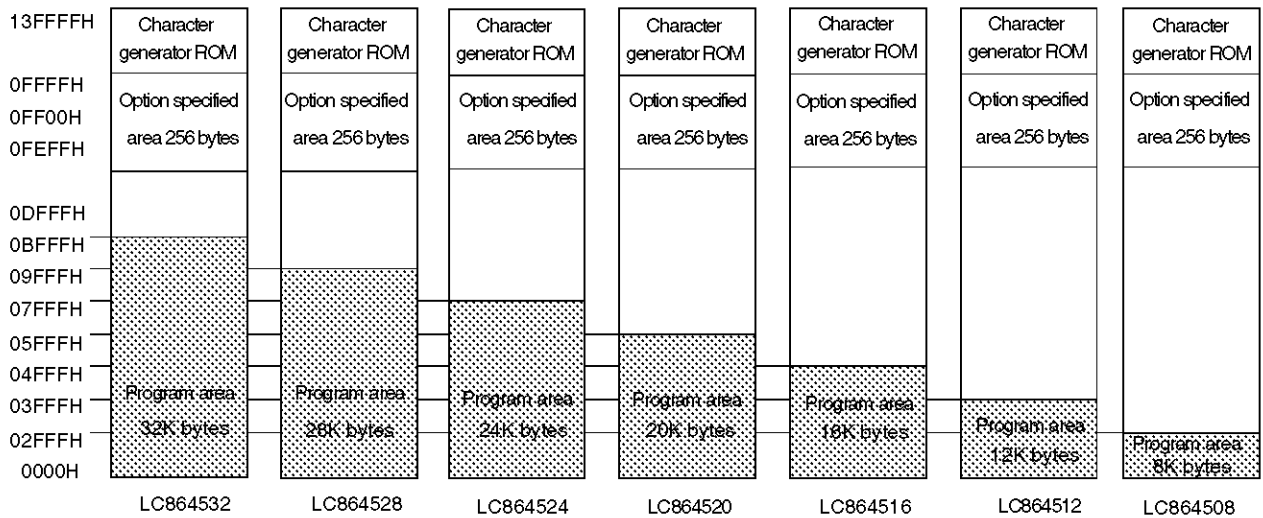
The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

LC86E4564

(3) ROM space

The LC86E4564 and LC864500 series use the program memory area of 256 bytes from 0FF00H to 0FFFFH to select the options. The program memory capacity of the series is 65280 bytes addressed on 0000H to 0FEFFH.

Note that the capacity of the LC86E4564 user-available EPROM is 32768 bytes addressed on 0000H to 7FFFH, although the LC86E4564 has 65536-byte EPROM.



Writing to EPROM

(1) Create programming data for LC86E4564

Programming data for EPROM of the LC86E4564 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program SU86K.EXE. The HEX file is used as the programming data for the LC86E4564.

(2) How to write data to EPROM

The LC86E4564 can be programmed by a general-purpose EPROM programmer with attachment W86EP4564D.

- Recommended EPROM programmer

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL1890A

- "27010 (Vp-p = 12.5 V) Intel high-speed programming" mode should be adopted. The address must be set to "0 to 13FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the function reading to disable the EPROM data from being read out.

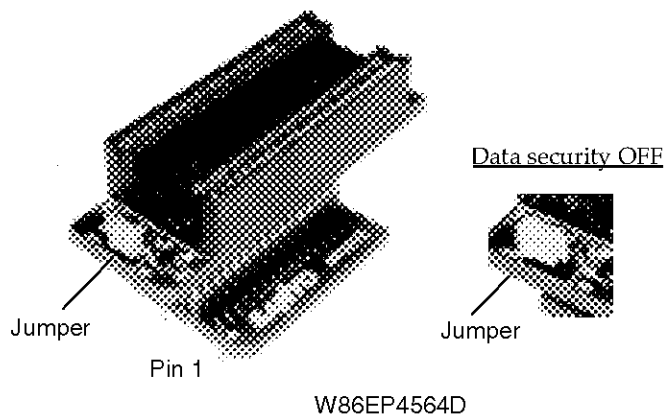
The following is the process in order to execute data security function.

- Set the jumper of attachment 'ON'.
- Program again. The EPROM programmer will display an error. The error means that the data security functions normally. It is not a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all addresses have 'FF' at sequence 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" cannot be executed data security at procedure 2 above.
- Set the jumper to 'OFF' after executing data security.

Data security



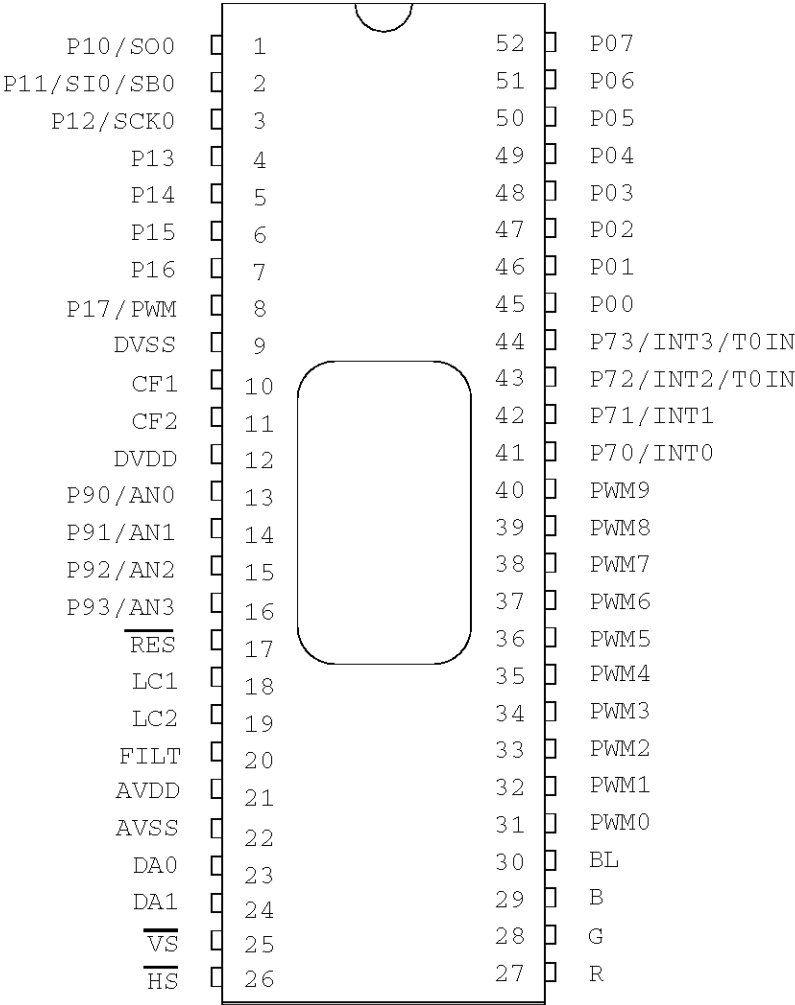
(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

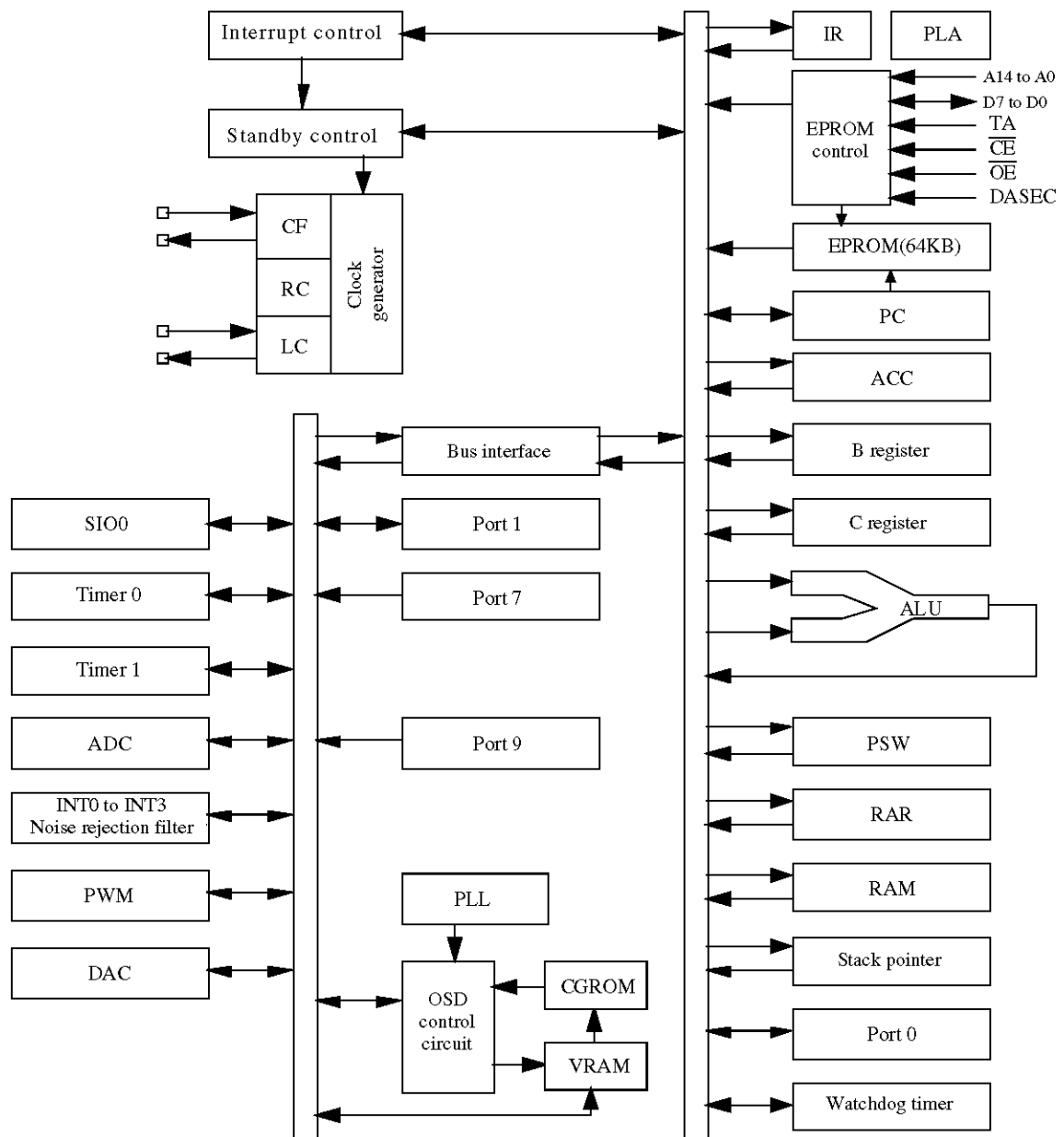
Because the UVEPROM (ultraviolet erasable programmable ROM) is incorporated in LC86E4564, put the seal on the window in use.

Pin Assignment



Top view

System Block Diagram



Pin Description

- Port option can be specified by bit units except the pull-up resistor selection of port 0.

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option	PROM mode								
DVSS	9	—	Negative power supply for digital circuit										
CF1	10	I	Input for ceramic resonator										
CF2	11	O	Output for ceramic resonator										
DVDD	12	—	Positive power supply for digital circuit										
$\overline{\text{RES}}$	17	I	Reset										
LC1	18	I	LC oscillation circuit input										
LC2	19	O	LC oscillation circuit output										
FILT	20	O	Filter for PLL										
AVDD	21	—	Positive power supply for analog circuit										
AVSS	22	—	Negative power supply for analog circuit										
DA0	23	I/O	DA0 output / General I/O port										
DA1	24	I/O	DA1 output / General I/O port										
$\overline{\text{VS}}$	25	I	Vertical synchronization signal input										
$\overline{\text{HS}}$	26	I	Horizontal synchronization signal input										
R	27	O	Red (R) output of RGB image output		A4 (*1)								
G	28	O	Green (G) output of RGB image output		A5 (*1)								
B	29	O	Blue (B) output of RGB image output		A6 (*1)								
BL	30	O	Fast blanking control signal Switch TV image signal and OSD image signal		A7 (*1)								
PWM0 to PWM9	31 to 40	O	PWM0 to 9 output 15 V withstand		PWM 0 to 8 : A8 to A16 (*1) PWM 9 : "L" fixed								
Port 0	45 to 52	I/O	8-bit Input / output port Input / output can be specified in nibble units HOLD release input Interrupt input	Pull-up resistor Provided/not provided (in bit units) Output Format CMOS/Nch-OD (in bit units)									
P00 to P07													
Port 1	1 to 8	I/O	8-bit Input/output port Input/output can be specified in bit units. Other function <table><tr><td>P10</td><td>SIO0 data output</td></tr><tr><td>P11</td><td>SIO0 data input / bus input / output</td></tr><tr><td>P12</td><td>SIO0 clock input / output</td></tr><tr><td>P17</td><td>Timer 1 (PWM) output</td></tr></table>	P10	SIO0 data output	P11	SIO0 data input / bus input / output	P12	SIO0 clock input / output	P17	Timer 1 (PWM) output	Output format CMOS/Nch-OD (in bit units)	D0 to D7 (*2)
P10				SIO0 data output									
P11	SIO0 data input / bus input / output												
P12	SIO0 clock input / output												
P17	Timer 1 (PWM) output												
P10 to P17													

LC86E4564

Pin name	Pin No.	I/O	Function Description				Option	PROM mode																																																											
Port 7 P70 P71 to P73	41 42 to 44	I/O I	4-bit input port Other function <table><tr><td>P70</td><td colspan="3">INT0 input/HOLD release input/ Nch-transistor output for watchdog timer</td><td colspan="2"></td></tr><tr><td>P71</td><td colspan="3">INT1 input/HOLD release input</td><td colspan="2"></td></tr><tr><td>P72</td><td colspan="3">INT2 input/timer 0 event input</td><td colspan="2"></td></tr><tr><td>P73</td><td colspan="3">INT3 input (noise rejection filter attached input/timer 0 event input)</td><td colspan="2"></td></tr></table> Interrupt receiver format vector address <table><tr><td></td><td>Rise</td><td>Fall</td><td>Rise/Fall</td><td>H level</td><td>L level</td><td>Vector</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr></table>				P70	INT0 input/HOLD release input/ Nch-transistor output for watchdog timer					P71	INT1 input/HOLD release input					P72	INT2 input/timer 0 event input					P73	INT3 input (noise rejection filter attached input/timer 0 event input)						Rise	Fall	Rise/Fall	H level	L level	Vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	Pull-up resistor provided/ not provided (in bit units)	P70 : VPP (*3) P71 : DASEC (*4) P72 : $\overline{OE}$ (*5) P73 : $\overline{CE}$ (*6)
P70	INT0 input/HOLD release input/ Nch-transistor output for watchdog timer																																																																		
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	Rise	Fall	Rise/Fall	H level	L level	Vector																																																													
INT0	enable	enable	disable	enable	enable	03H																																																													
INT1	enable	enable	disable	enable	enable	0BH																																																													
INT2	enable	enable	enable	disable	disable	13H																																																													
INT3	enable	enable	enable	disable	disable	1BH																																																													
Port 9 P90 to P93	13 to 16	I	4-bit input port Other function A/D converter input port (4 lines)					A0 to A3 (*1)																																																											

*1 An → Address input

*2 Data I/O

*3 Power for programming

*4 Memory select input/output for data security

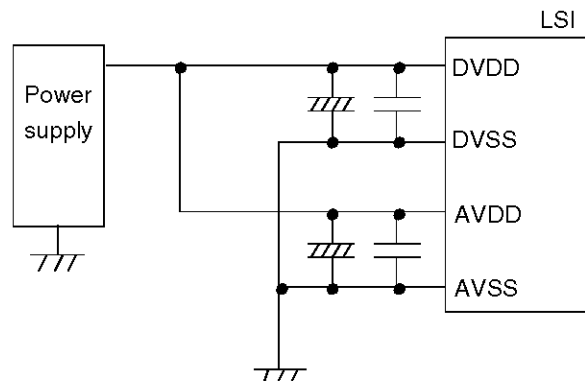
*5 Output Enable input

*6 Chip Enable input

- All of port options except the pull-up resistor option of Port 0 can be specified in a bit unit.
- Port status in reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the noise influence.



Specifications

1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter		Symbol	Pins	Conditions	Ratings			Unit	
					V _{DD} [V]	min	typ		max
Supply voltage		V _{DD} max	DVDD, AVDD	DVDD = AVDD		−0.3		+7.0	V
Input voltage		V _I (1)	• P71, 72, 73 • Port 9 • $\overline{\text{RES}}$, $\overline{\text{HS}}$, $\overline{\text{VS}}$			−0.3		V _{DD} +0.3	
Output voltage		V _O (1)	R, G, B, BL, FILT			−0.3		V _{DD} +0.3	
		V _O (2)	PWM0 to PWM9			−0.3		+15	
Input/output voltage		V _{IO} (1)	Ports 0, 1, P70 DA0, 1			−0.3		V _{DD} +0.3	
High-level output current	Peak output current	I _{OPH} (1)	Ports 0, 1	•Pull-up MOS transistor output •At each pin		−2			mA
		I _{OPH} (2)	Ports 0, 1 DA0, 1	•CMOS output •At each pin		−4			
		I _{OPH} (3)	R, G, B, BL	•CMOS output •At each pin		−5			
	Total output current	ΣI _{OA} H(1)	Port 1	The total of all pins		−10			
		ΣI _{OA} H(2)	Port 0	The total of all pins		−10			
		ΣI _{OA} H(3)	R, G, B, BL	The total of all pins		−15			
Low-level output current	Peak output current	I _{OPL} (1)	Ports 0, 1 DA0, 1	At each pin				20	
		I _{OPL} (2)	P70	At each pin				30	
		I _{OPL} (3)	• R, G, B, BL • PWM0 to PWM9	At each pin				5	
	Total output current	ΣI _{OA} L(1)	Port 0	The total of all pins				40	
		ΣI _{OA} L(2)	Port 1, P70	The total of all pins				40	
		ΣI _{OA} L(3)	R, G, B, BL	The total of all pins				15	
		ΣI _{OA} L(4)	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIC52S	Ta = +10 to +40°C				600	mW
Operating temperature range		Topr				10		+40	°C
Storage temperature range		Tstg				−55		+150	

- * DVSS and AVSS must be supplied the same voltage, VSS. VSS = DVSS = AVSS
 DVDD and AVDD must be supplied the same voltage, VDD. VDD = DVDD = AVDD

2. Recommended Operating Range at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V _{DD} [V]	min	typ	max	
Operating supply voltage range	V _{DD}	DVDD, AVDD	0.98 μs ≤ tCYC tCYC ≤ 1.02 μs		4.5		5.5	V
Hold voltage	V _{HD}	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high voltage	V _{IH} (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V _{DD}		V _{DD}	
	V _{IH} (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS	Output disable	4.5 to 5.5	0.75V _{DD}		V _{DD}	
	V _{IH} (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V _{DD}		V _{DD}	
	V _{IH} (4)	P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V _{DD} −0.5		V _{DD}	
	V _{IH} (5)	Port 9 DA0, 1 port input		4.5 to 5.5	0.7V _{DD}		V _{DD}	
Input low voltage	V _{IL} (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V _{SS}		0.2V _{DD}	
	V _{IL} (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS • Port 9	Output disable	4.5 to 5.5	V _{SS}		0.25V _{DD}	
	V _{IL} (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V _{SS}		0.25V _{DD}	
	V _{IL} (4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V _{SS}		0.6V _{DD}	
	V _{IL} (5)	Port 9 DA0, 1 port input		4.5 to 5.5	V _{SS}		0.3V _{DD}	
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.98	1	1.02	μs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.98		30	
Oscillation frequency range (Note 1)	FmCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5	14.11			
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	3.0	
Oscillation stable time period (Note 2)	tmsCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms

Note 1: Refer to Table 1 and Table 2 for oscillation constant.

Note 2: The oscillation stable time period refers to the time it takes to oscillate stably after the following conditions.

1. Applying the first supply voltage.
2. Release of the HOLD mode.
3. Release of the stopping of the main-clock oscillation.

3. Electrical Characteristics at Ta= +10°C to +40°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Ratings			Unit
					min	typ	max	
Input high-level current	I _{IH} (1)	<ul style="list-style-type: none"> Port 1 DA0, 1 Port 0 without pull-up MOS transistor 	<ul style="list-style-type: none"> Output disable Pull-up MOS transistor OFF V_{IN} = V_{DD} (including the off-leak current of the output transistor) 	4.5 to 5.5			1	μA
	I _{IH} (2)	<ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 9 $\overline{\text{RES}}$ $\overline{\text{HS}}$, $\overline{\text{VS}}$ 	V _{IN} = V _{DD}	4.5 to 5.5			1	
Input low-level current	I _{IL} (1)	<ul style="list-style-type: none"> Port 1 DA0, 1 Port 0 without pull-up MOS transistor 	<ul style="list-style-type: none"> Output disable Pull-up MOS transistor OFF V_{IN} = V_{SS} (including the off-leak current of the output transistor) 	4.5 to 5.5	-1			
	I _{IL} (2)	<ul style="list-style-type: none"> Port 7 without pull-up MOS transistor Port 9 	V _{IN} = V _{SS}	4.5 to 5.5	-1			
	I _{IL} (3)	<ul style="list-style-type: none"> $\overline{\text{RES}}$ $\overline{\text{HS}}$, $\overline{\text{VS}}$ 	V _{IN} = V _{SS}	4.5 to 5.5	-1			
Output high-level voltage	V _{OH} (1)	CMOS output of ports 0, 1 DA0, 1	I _{OH} = -1.0 mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)	R, G, B, BL	I _{OH} = -0.1 mA	4.5 to 5.5	V _{DD} -0.5			
Output low-level voltage	V _{OL} (1)	Ports 0, 1	I _{OL} = 10 mA	4.5 to 5.5			1.5	
	V _{OL} (2)	Ports 0, 1 DA0, 1	<ul style="list-style-type: none"> I_{OL} = 1.6 mA The total current of the ports 0, 1 is 40 mA or less. 	4.5 to 5.5			0.4	0.4
	V _{OL} (3)	<ul style="list-style-type: none"> R, G, B, BL PWM0 to PWM9 	<ul style="list-style-type: none"> I_{OL} = 3.0 mA The current of any unmeasured pin is 3 mA or less. 	4.5 to 5.5			0.4	
	V _{OL} (4)	P70	I _{OL} = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	R _{pu}	<ul style="list-style-type: none"> Ports 0, 1 Port 7 	V _{OH} = 0.9V _{DD}	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I _{OFF}	PWM0 to PWM9	V _{OUT} = 13.5 V	4.5 to 5.5			5	μA
Hysteresis voltage	V _{HIS}	<ul style="list-style-type: none"> Ports 0, 1 Port 7 $\overline{\text{RES}}$ $\overline{\text{HS}}$, $\overline{\text{VS}}$ 	Output disable	4.5 to 5.5		0.1V _{DD}		V
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> f = 1 MHz Unmeasured input pins are set to V_{SS} level. Ta = 25°C 	4.5 to 5.5		10		pF

4. Serial Input/Output Characteristics at Ta = +10°C to +40°C , VSS = 0 V

Parameter		Symbol	Pins	Conditions	VDD [V]	Ratings			Unit
						min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0 • SCLK0	Refer to Figure 5.	4.5 to 5.5	2		tCYC
		Low-level pulse width	tCKL(1)			4.5 to 5.5	1		
		High-level pulse width	tCKH(1)			4.5 to 5.5	1		
	Output clock	Cycle	tCKCY(2)	• SCK0 • SCLK0	• Use a pull-up resistor (1 kΩ) during open drain output • Refer to Figure 5.	4.5 to 5.5	2		
		Low-level pulse width	tCKL(2)			4.5 to 5.5		1/2tCKCY	
		High-level pulse width	tCKH(2)			4.5 to 5.5		1/2tCKCY	
Serial input	Data setup time	tICK	SI0	• Data setup to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 5.	4.5 to 5.5	0.1			μs
	Data hold time	tCKI			4.5 to 5.5	0.1			
Serial output	Output delay time (External serial clock)	tCKO(1)	SO0	• Use a pull-up resistor (1 kΩ) during open drain output. • Data setup to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5.	4.5 to 5.5			7/12tCYC +0.2	μs
	Output delay time (Internal serial clock)	tCKO(2)			4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Ratings			Unit
					min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is set to 1/1)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is set to 1/16)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 5.5	32			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 5.5	200			μs
	tPIH(5) tPIL(5)	$\overline{\text{HS}}$, $\overline{\text{VS}}$	Display position controllable Each active edge of $\overline{\text{HS}}$, $\overline{\text{VS}}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10			tCYC
Rise/fall time	tTHL tTLH	$\overline{\text{HS}}$	Refer to Figure 7.	4.5 to 5.5			500	ns
Horizontal pull-in range	FH	$\overline{\text{HS}}$	The monitor point in Figure 10 is 1/2 V _{DD} .	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	V _{DD} [V]	Ratings			Unit
					min	typ	max	
Resolution	N			4.5 to 5.5		4		bit
Absolute precision	ET		Note 3	4.5 to 5.5		±1/4	±1/2	LSB
Conversion time	tCAD	From Vref selection to when the result is produced	1 bit conversion time = 2tCYC	4.5 to 5.5			1.96	μs
Reference current	I _{REF}		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V _{AIN}	AN0 to AN3		4.5 to 5.5	V _{SS}		V _{DD}	V
Analog port input current	I _{AINH}		V _{AIN} = V _{DD}	4.5 to 5.5			1	μA
	I _{AINL}		V _{AIN} = V _{SS}	4.5 to 5.5	-1			

Note 3: Absolute precision excepts quantizing error (±1/2 LSB).

7. D/A Converter Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				V _{DD} [V]	min	typ	max
Resolution	NDA			4.5 to 5.5		7	bit
Absolute precision	ETDA		7 bits mode (Note 4)	4.5 to 5.5		±2.0	LSB
Settling time	tSDA		(Note 5)	4.5 to 5.5		1.0	μs
Analog input voltage range	V _{AOUT}	DA0 to DA1		4.5 to 5.5	V _{SS}		V _{DD}
Output register	RODA		(Note 6)	4.5 to 5.5		8	kΩ

Note 4 : Absolute precision excepts quantizing error (±1/2 LSB).

Note 5 : Settling time refers to the time from when the DA conversion instruction is executed to when the analog voltage output corresponding to the digital on the specific port is generated.

Note 6 : DA data = 80H

8. Current Drain Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V _{DD} [V]	min	typ		max
Current drain during basic operation (Note 7)	I _{DDOP} (1)	DV _{DD} , AV _{DD}	<ul style="list-style-type: none">FmCF = 12 MHz for ceramic resonator oscillationFmLC = 14.11 MHz for LC oscillationSystem clock: CF oscillationInternal RC oscillation stops	4.5 to 5.5		21	32	mA
Current drain in HALT mode (Note 7)	I _{DDHALT} (1)	DV _{DD} , AV _{DD}	<ul style="list-style-type: none">HALT modeFmCF = 12 MHz for ceramic resonator oscillationFmLC = 0 Hz (when oscillation stops)System clock : CF oscillationInternal RC oscillation stops.	4.5 to 5.5		5	10	mA
	I _{DDHALT} (2)	DV _{DD} , AV _{DD}	<ul style="list-style-type: none">HALT modeFmCF = 0 MHz (when oscillation stops)FmLC = 0 Hz (when oscillation stops)System clock : Internal RC	4.5 to 5.5		400	800	μA
Current drain in HOLD mode (Note 7)	I _{DDHOLD} (1)	DV _{DD} , AV _{DD}	<ul style="list-style-type: none">HOLD modeAll oscillation stop.	4.5 to 5.5		0.05	20	μA
	I _{DDHOLD} (2)							

Note 7 : The currents to the output transistors and the pull-up MOS transistors are ignored.

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Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	47 pF	47 pF

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

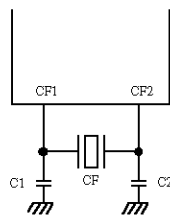
Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main clock)

Oscillation type	L	C3	C4
14.11 MHz LC oscillation	4.7 μ H	33 pF	45 pF (Trimmer)
	4.7 μ H $\pm 10\%$ (Variable)	33 pF	33 pF

* See Figures 11 and 12 for the LC oscillation frequency characteristics.

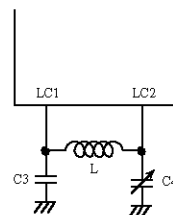
Table 2. LC oscillation Guaranteed Constants (OSD clock)

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 - If you use other oscillators herein, we provide no guarantee for the characteristics.
 - Adjust the voltage of monitor point in Figure 10 to $1/2V_{DD} \pm 10\%$ by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



main clock

Figure 1 Ceramic resonator oscillation



OSD clock

Figure 2 LC resonator oscillation

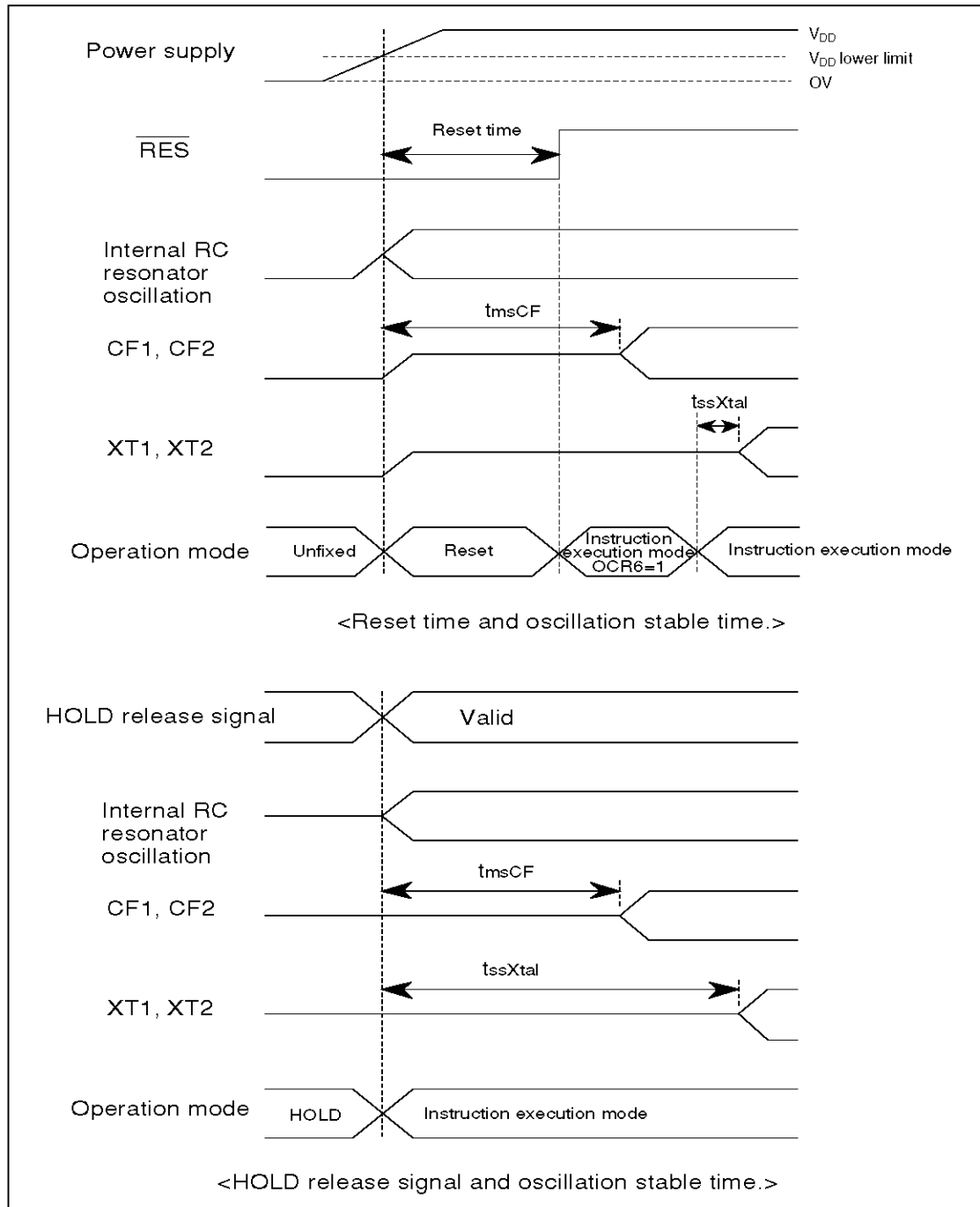
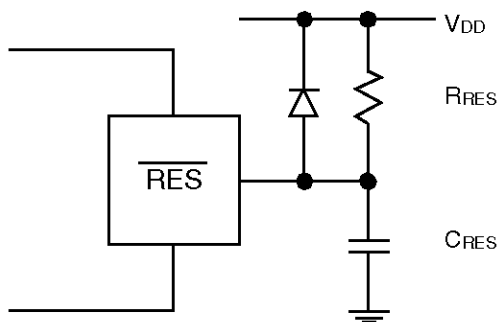


Figure 3 Oscillation Stable Time



(Note) Set the values of C_{RES} , R_{RES} so that the reset time is 200 μs or longer.

Figure 4 Reset Circuit

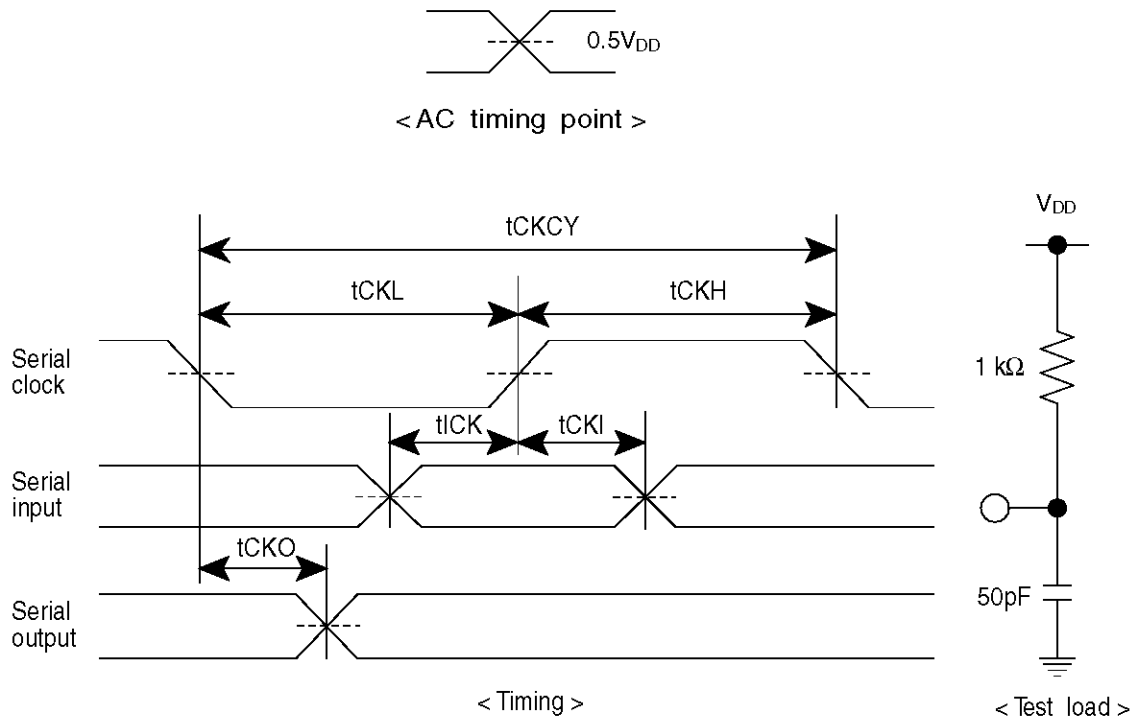


Figure 5 Serial Input/output Test Condition

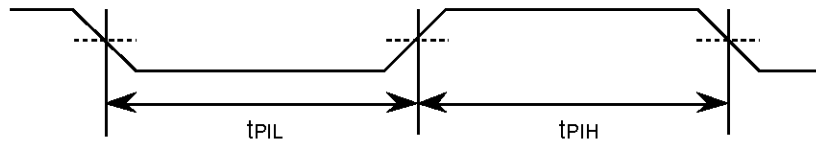


Figure 6 Pulse Input Timing Condition - 1

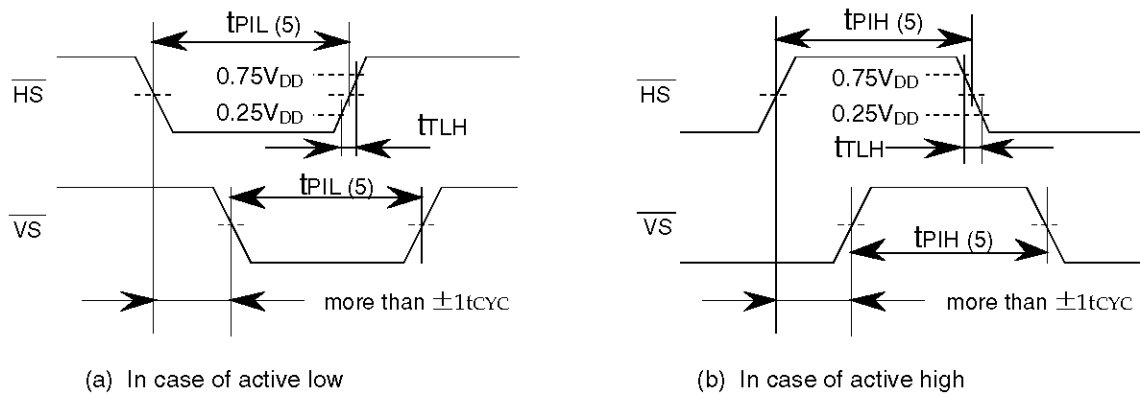


Figure 7 Pulse Input Timing Condition - 2

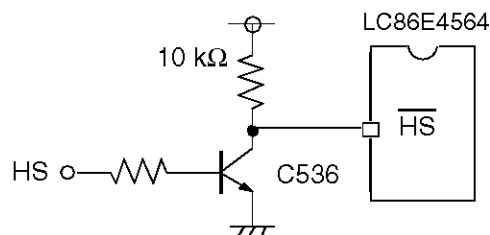


Figure 8 Recommended Interface Circuit

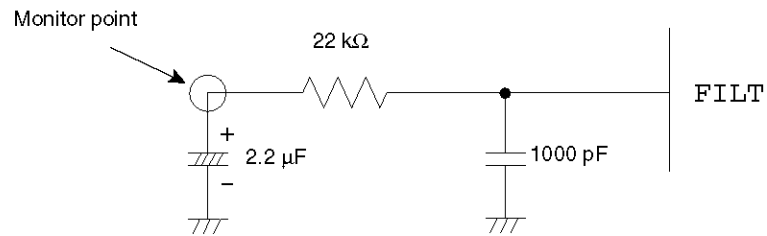


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

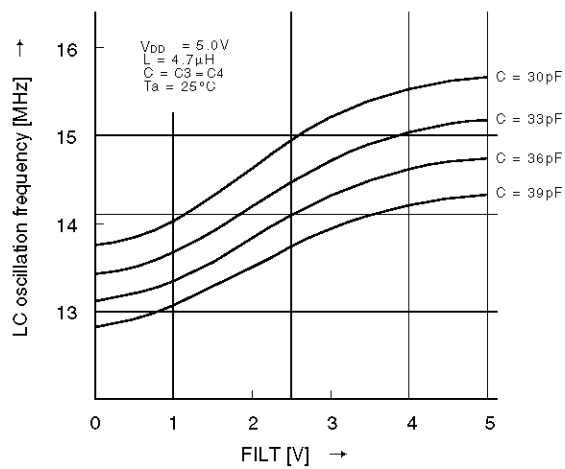


Figure 11 FILT-LC Oscillation Frequency (1)

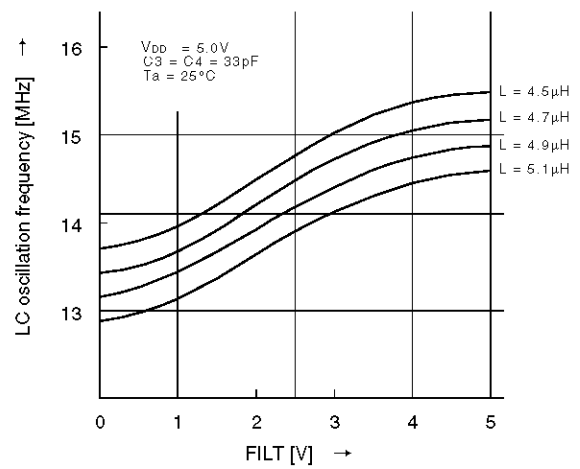


Figure 12 FILT-LC Oscillation Frequency (2)

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